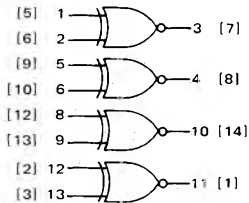


QUAD EXCLUSIVE
"NOR" GATE
(Open Collector)

MC8200/MC7200 series

MC8242F, L*
MC7242F, L, P*

ADVANCE INFORMATION/NEW PRODUCT



$$3 = \bar{1} \cdot \bar{2} + 1 \cdot 2$$

V_{CC} = Pin 14 [4]
GND = Pin 7 [11]

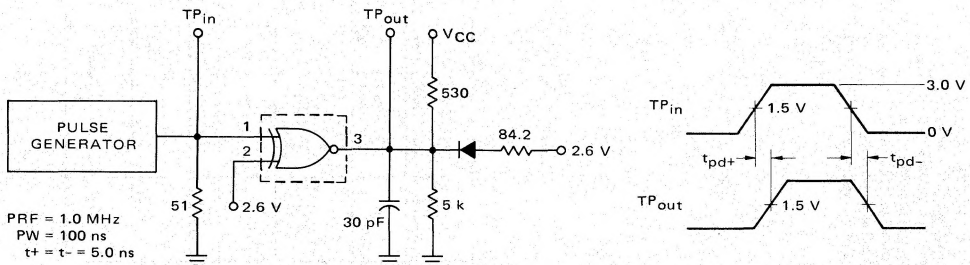
Numbers at ends of terminals represent pin numbers for devices in the dual in-line package.

Numbers in brackets represent pin numbers for devices in the flat package.

This device contains four independent Exclusive NOR gates with open collector outputs which may be used to implement digital comparison functions. A four-bit comparison may be made by connecting the outputs together.

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 170 mW typ/pkg

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



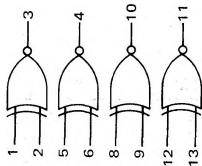
5 kΩ and 30 pF include jig and scope.

*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

MC8242F,L, MC7242F,L,P (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Pin numbers indicated are for devices in dual in-line packages only. To test devices in the flat package, substitute pin numbers shown in brackets on the logic diagram on the first page of this data sheet.



Characteristic	Symbol	Pin Under Test	MC8242 Test Limits												MC7242 Test Limits												TEST CURRENT/VOLTAGE VALUE											
			-55°C			+25°C			+125°C			0°C			+25°C			+75°C			-55°C			+25°C			+125°C			0°C			+25°C			+75°C		
			Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit	Min	Max	Unit			
Input	Forward Current	1	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc			
		2	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc	-0.1	-3.2	mAdc			
		Leakage Current	1	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc	-	50	µAdc		
Breakdown Voltage	BV _{in}	1	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc			
	2	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc	-	6.0	Vdc				
Output	Output Voltage	3	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc	-	0.4	Vdc			
		Leakage Current	3	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc	-	25	µAdc		
Power Requirements (Total Device)	Power Supply Drain	14	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc	-	-	mAdc			
		Switching Parameters	3	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns		
Turn-On Delay	t _{pd-}	3	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns			
	Turn-Off Delay	3	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns	-	-	ns			
TEST CURRENT/VOLTAGE VALUE	mA	I _{OL}	I _{in}	V _{I/L}	V _{I/H}	V _F	V _R	V _{CC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}		
																																					25	10
TEST CURRENT/VOLTAGE VALUE	Volts	I _{OL}	I _{in}	V _{I/L}	V _{I/H}	V _F	V _R	V _{CC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	V _{VCC}	
																																						25