# MC5420 · MC7420

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7420 only.

**CIRCUIT SCHEMATIC**
1/2 OF CIRCUIT SHOWN
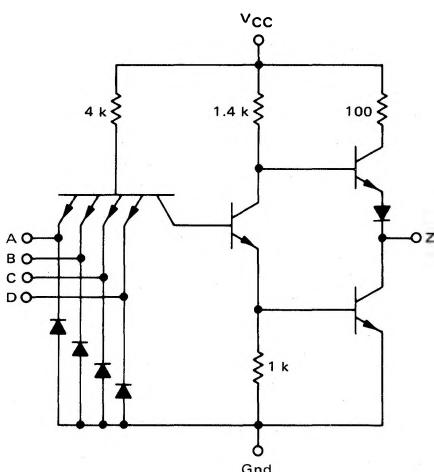
V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

FLAT Pkg Pin / DIL Pkg Pin

Positive Logic: $Z = \overline{A \cdot B \cdot C \cdot D}$
Negative Logic: $Z = \overline{A + B + C + D}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 20 mW typ/pkg
Propagation Delay Time = 10 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

V_{CC} +5.0 Vdc

Coax
950 ±1.0%
950 ±1.0%
400
TP_{in}
TP_{out}
MMD6150 or Equiv
MMD7000 or Equiv
PULSE GENERATOR
V_{IH}
50
C_T

t+ = 12 ns
t− = 6.0 ns } 10% to 90% points
PRF = 1.0 MHz
Duty Cycle = 50%
PW = 0.5 μs
$Z_{out} \approx 50\ \Omega$

TP_{in} — 3.0 V min / 1.5 V / 0 V max
TP_{out} — 2.4 V min / 1.5 V / 0.4 V max / Gnd
t_{pd-} t_{pd+}
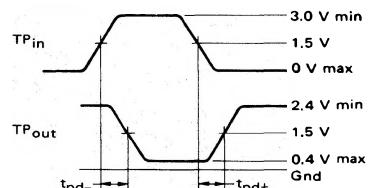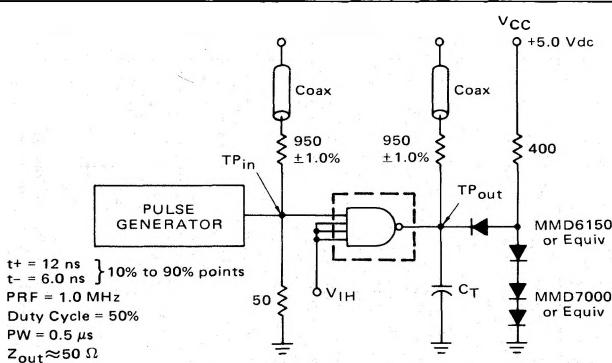
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.
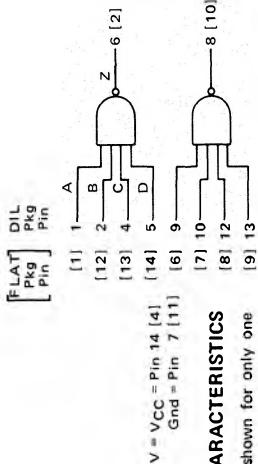
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

Pin assignments:

	F LAT Pkg Pin	DIL Pkg Pin
A	[11]	1
B	[12]	2
C	[13]	4
D	[14]	5
	[6]	9
Z	[7] [11]	10
	[8]	12
	[9]	13

V = VCC = Pin 14 [4]
Gnd = Pin 7 [11]

Z 6 [2]
8 [10]

Pin 7 [11] is grounded for all tests in addition to the pins listed below.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)

		mA		Volts									
		IOL	IOH	VIL	VIH	VIHH	VR1	VR2	Vth1	Vth0	VCC	VCCL	VCCH
MC5420		16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
MC7420		16	-0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC5420 Test Limits −55 to +125°C Min	Max	Unit	MC7420 Test Limits 0 to +70°C Min	Max	Unit
Input Forward Current	I_F	A	-	-1.6	mAdc	-	-1.6	mAdc
Leakage Current	I_{R1}	A	-	40	μAdc	-	40	μAdc
	I_{R2}	A	-	1.0	mAdc	-	1.0	mAdc
Output Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc
Short-Circuit Current	I_{SC}†	Z	-20	-55	mAdc	-18	-55	mAdc
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	V	-	11	mAdc	-	11	mAdc
	I_{PDL}	V	-	4.0	mAdc	-	4.0	mAdc
Switching Parameters Turn-On Delay	t_{pd-}	A,Z	-	15**	ns	-	15**	ns
Turn-Off Delay	t_{pd+}	A,Z	-	22**	ns	-	22**	ns

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

Symbol	IOL	IOH	VIL	VIH	VIHH	VR1	VR2	Vth1	Vth0	VCC	VCCL	VCCH	Gnd
I_F	-	-	A	-	-	B,C,D	-	-	-	-	-	-	*
I_{R1}	-	-	-	A	-	-	-	-	-	-	-	-	B,C,D*
I_{R2}	-	-	-	-	A	-	-	-	-	-	-	-	B,C,D*
V_{OL}	Z	-	-	-	-	-	-	A,B,C,D	-	-	-	-	*
V_{OH}	-	Z	-	-	-	B,C,D	-	-	A	-	V	-	*
I_{SC}	-	-	-	-	-	-	-	-	-	V	-	V	All Inputs
I_{PDH}	-	-	-	-	-	-	All Inputs	-	-	-	-	V	-
I_{PDL}	-	-	-	-	-	-		-	-	-	-	V	-
t_{pd-}	Pulse In: A	Pulse Out: Z	-	B,C,D	-	-	-	-	-	V	-	V	A,B,C,D*
t_{pd+}	Pulse In: A	Pulse Out: Z	-	B,C,D	-	-	-	-	-	V	-	V	*

* Ground inputs to gate not under test.
** Tested only at 25°C.
† Only one output should be shorted at a time.