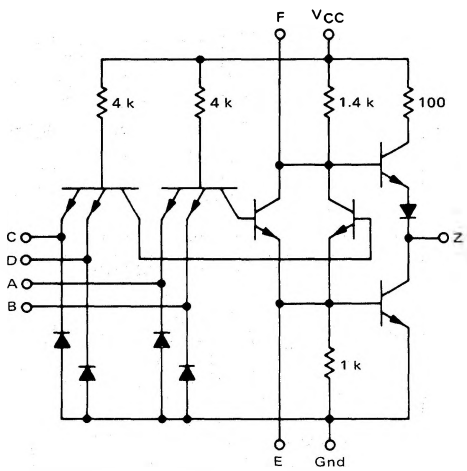
EXPANDABLE DUAL
2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

MC5450 • MC7450

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC7450 only.

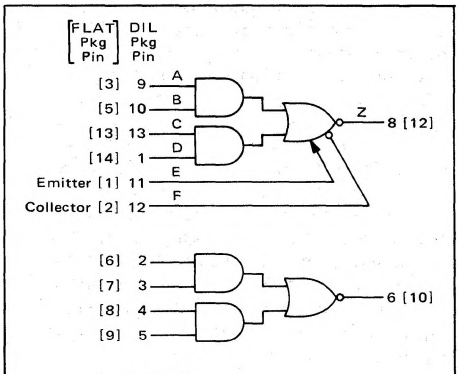
CIRCUIT SCHEMATIC
1/2 OF CIRCUIT SHOWN†



V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

†Other half of circuit omits expander inputs.

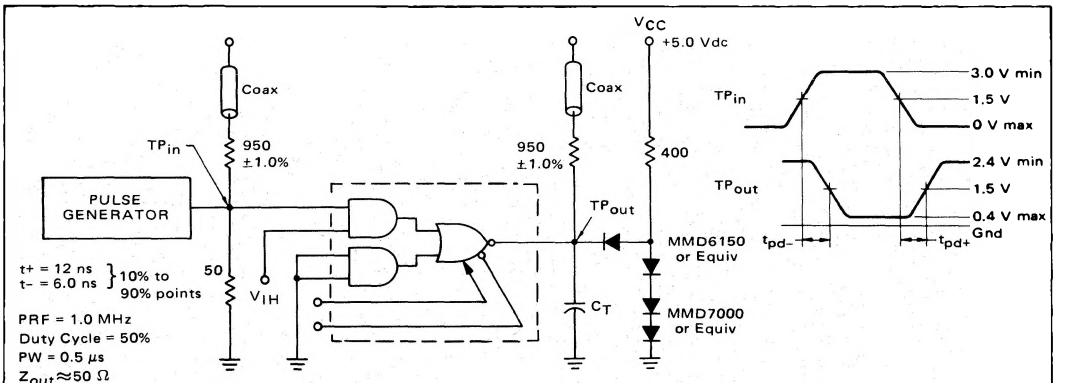
This device consists of two AND-OR-INVERT gates, one of which OR expandable. Up to four MC5460/7460 expander gates may be ORed with the device at the expander points.



Positive Logic:
$Z = \overline{(A \bullet B) + (C \bullet D) + (\text{Expanders})}$
Negative Logic:
$Z = \overline{(A + B) \bullet (C + D) \bullet (\text{Expanders})}$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 28 mW typ/pkg
Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

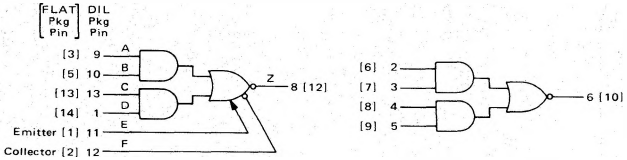


C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



V= V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]

Pin 7[11] is grounded for all tests in addition to the pins listed below: Gnd

Characteristic	Symbol	Pin Under Test	MC5450 Test Limits −55 to +125°C Min	MC5450 Test Limits −55 to +125°C Max	MC5450 Test Limits −55 to +125°C Unit	MC7450 Test Limits 0 to +70°C Min	MC7450 Test Limits 0 to +70°C Max	MC7450 Test Limits 0 to +70°C Unit	I_{OL} (mA)	I_{OH} (mA)	I_{X1} (mA)	I_{X2} (mA)	I_{X3} (mA)	I_{X4} (mA)	R_{EX} ③ (Ohms)	V_{EX} ① (Volts)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_{R1} (Volts)	V_{R2} (Volts)	$V_{th\,1}$ (Volts)	$V_{th\,0}$ (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
									TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																	
	MC5450								16	-0.4	0.41	0.15	-0.15	0.3	138	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.50	5.50
	MC7450								16	-0.4	0.62	0.27	-0.27	0.43	130	0.4	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.0	4.75	5.25
Input																										
Forward Current	I_F	D	-	-1.6	mAdc	-	-1.6	mAdc	-	-	-	-	-	-	-	-	D	-	-	C	-	-	-	-	-	V
Leakage Current	I_{R1}	D	-	40	μAdc	-	40	μAdc	-	-	-	-	-	-	-	-	-	D	-	-	-	-	-	-	-	V
	I_{R2}	D	-	1.0	mAdc	-	1.0	mAdc	-	-	-	-	-	-	-	-	-	-	D	-	-	-	-	-	-	V
Expander Input Current	I_{EX}	F ①	-	-2.9#	mAdc	-	-3.1#	mAdc	Z	-	-	-	-	-	-	E,F	-	-	-	-	-	-	-	-	V	-
Base-Emitter Voltage	V_{BE}	E ②	-	1.0#	Vdc	-	1.0#	Vdc	Z	-	E,F	-	-	-	-	-	-	-	-	-	-	-	-	-	V	-
Output																										
Output Voltage	V_{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	-	-	-	-	-	-	-	-	C,D	-	-	V	-
		Z ③	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	E	F	-	-	-	-	-	-	C,D	-	-	V	-
	V_{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	-	-	-	-	-	C	-	-	D	-	V	-
		Z	2.4#	-	Vdc	2.4#	-	Vdc	-	Z	-	E	F	-	-	-	-	-	-	-	-	-	-	-	V	-
Short-Circuit Current	I_{SC} †	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	V	-	14	mAdc	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	All Inputs	-	-	-	-	V
	I_{PDL}	V	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	V
Switching Parameters									Pulse In	Pulse Out																
Turn-On Delay	t_{pd-}	D,Z	-	15**	ns	-	15**	ns	D	Z	-	-	-	-	-	-	-	C	-	-	-	-	-	V	-	-
Turn-Off Delay	t_{pd+}	D,Z	-	29**	ns	-	29**	ns	D	Z	-	-	-	-	-	-	-	C	-	-	-	-	-	V	-	-

*Ground inputs to gate not under test. †Only one output should be shorted at a time. #Tested only at low temperature limit.
** Tested only at 25°C.

① See Figure 1.
② See Figure 2.
③ See Figure 3.

FIGURE 1 – I_{EX} TEST CIRCUIT

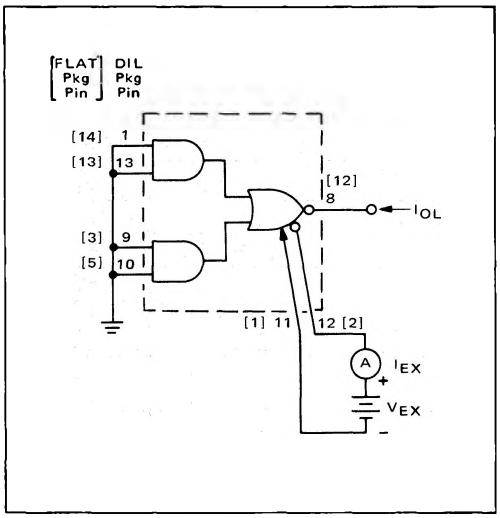


FIGURE 2 – V_{BE} TEST CIRCUIT

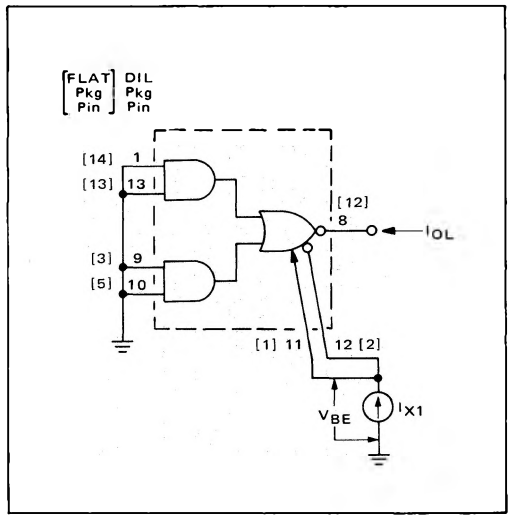


FIGURE 3 – V_{OL} TEST CIRCUIT