5-BIT SHIFT REGISTER

MC5496
MC7496

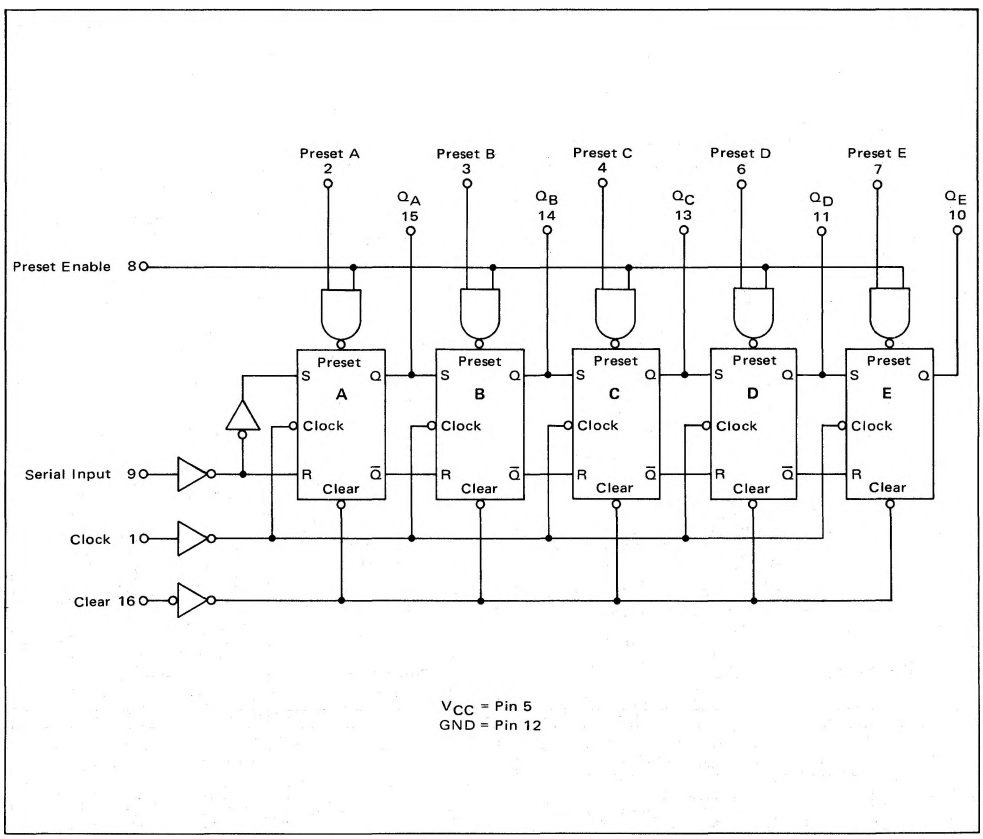
ADVANCE INFORMATION

Soon to be announced, the MC5496/7496 5-bit shift register is constructed of five R-S master-slave flip-flops plus internal gating to accomplish serial-to-parallel or parallel-to-serial conversion, and parallel-in/parallel-out or serial-in/serial-out operation.

Right-shift operation is accomplished by entering serial data at the serial input prior to the positive transition of clock pulse.

The common clear input is independent of the clock, and the separate preset inputs are independent of the clock or clear inputs.

The clear input must be at a logic "1" level and the preset input must be at a logic "0" level when clocking occurs.



Total Power Dissipation = 240 mW typ/pkg
Propagation Delay Time (Clock to Output) = 25 ns typ
Maximum Toggle Frequency = 10 MHz