

MC7524L MC7525L

DUAL SENSE AMPLIFIERS

Advance Information

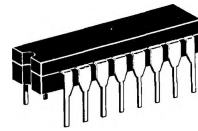
MONOLITHIC DUAL SENSE AMPLIFIERS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and M TTL circuits.

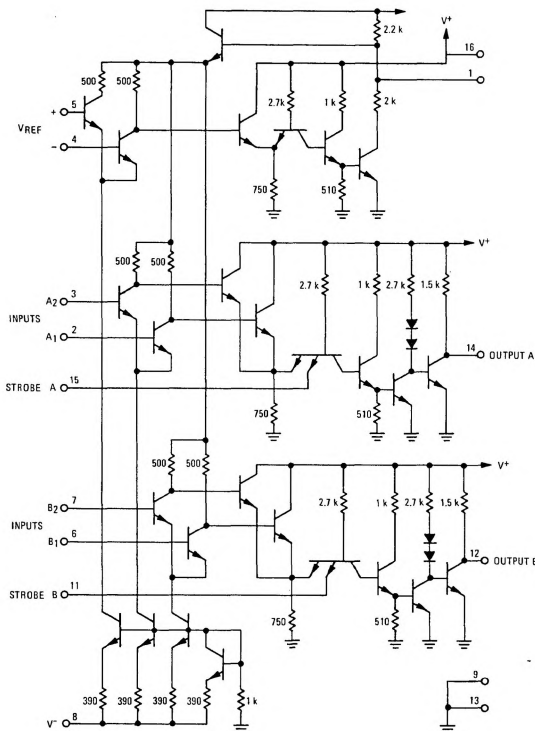
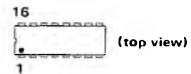
Features:

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs

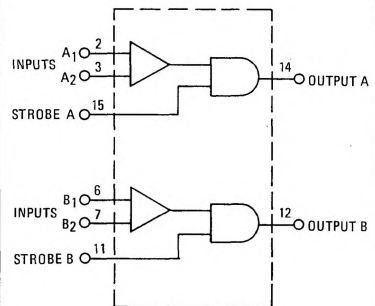
DUAL HIGH-SPEED
SENSE AMPLIFIER
INTEGRATED CIRCUIT
MONOLITHIC SILICON
EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 620



Equivalent Circuit



MC7524L, MC7525L (continued)

MAXIMUM RATINGS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Units
Power Supply Voltage	V^+	+7.0	Vdc
	V^-	-7.0	Vdc
Differential Input Voltages	V_{in} or V_{ref}	± 5.0	Vdc
Power Dissipation Derate above $T_A = +25^{\circ}\text{C}$	P_D	575	mW
		3.85	$\text{mW}^{\circ}\text{C}$
Operating Temperature Range	T_A	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = 0$ to $+70^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
Input Threshold Voltage $V_{ref} = 15\text{ mV}$ $V_{ref} = 40\text{ mV}$	V_{th}	11	15	19	mV	
		8.0	15	22		
		36	40	44		
		33	40	47		
Common-Mode Input Firing Voltage	V_{CMF}	-	± 3.0	-	Volts	
Input Bias Current	I_{in}	-	30	75	μA	
Input Offset Current	I_{io}	-	0.5	-	μA	
Input Impedance ($f = 1.0\text{ kHz}$)	$Z_{in(D)}$	-	2.0	-	k ohms	
Input Voltage Logic "1" Level (Strobe Inputs)	$V_{in(0)} = 0.8\text{ V}$	$V_{in(1)}$	2.0	-	Volts	
Input Voltage Logic "0" Level (Strobe Inputs)	$V_{in(1)} = 2.0\text{ V}$	$V_{in(0)}$	-	-	Volt	
Input Current Logic "0" Level (Strobe Inputs)	$V_{in(0)} = 0.4\text{ V}$	$I_{in(0)}$	-	-1.0	-1.6	mA
Input Current Logic "1" Level (Strobe Inputs)	$V_{in(1)} = 2.4\text{ V}$ $V_{in(1)} = V^+$	$I_{in(1)}$	-	-	40	μA
			-	-	1.0	mA
Output Voltage Logic "1" Level	$V_{in(1)} = 2.0\text{ V}$, $V_{in(0)} = 0.8\text{ V}$	$V_{out(1)}$	2.4	3.9	-	Volts
Output Voltage Logic "0" Level	$V_{in(0)} = 0.8\text{ V}$	$V_{out(0)}$	-	0.25	0.4	Volt
Short-Circuit Output Current	$I_{sc(out)}$	2.1	-	3.5	mA	
V^+ Supply Current @ $T_A = +25^{\circ}\text{C}$	I^+	-	25	-	mA	
V^- Supply Current @ $T_A = +25^{\circ}\text{C}$	I^-	-	-15	-	mA	

SWITCHING CHARACTERISTICS ($V^+ = 5.0\text{ V}$, $V^- = -5.0\text{ V}$, $T_A = +25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (Differential Input to Output)	$t_{pd(1)D}$	-	15	40	ns
	$t_{pd(0)D}$	-	40	-	
Propagation Delay Time (Strobe Input to Output)	$t_{pd(1)S}$	-	15	30	ns
	$t_{pd(0)S}$	-	35	-	
Differential-Mode Input Overload Recovery Time	$t_{OR DM}$	-	20	-	ns
Common-Mode Input Overload Recovery Time	$t_{OR CM}$	-	20	-	ns
Minimum Cycle Time	$t_c(\text{min})$	-	200	-	ns