Low Skew CMOS PLL Clock Driver
With Power-Down/Power-Up Feature

MC88920

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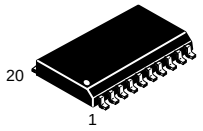


DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04

The MC88920 Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The RST_IN/RST_OUT(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040 microprocessor family.

The PLL allows the the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88920 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

- 2X_Q Output Meets All Requirements of the 20 and 25MHz 68040 Microprocessor PCLK Input Specifications
- Three Outputs (Q0–Q2) With Output–Output Skew <500ps and Six Outputs Total (Q0–Q2, Q3, 2X_Q,) With <1ns Skew Each Being Phase and Frequency Locked to the SYNC Input
- The Phase Variation From Part–to–Part Between SYNC and the 'Q' Outputs Is Less Than 600ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5MHZ to 2X_Q $F_{Max}/4$
- Additional Outputs Available at 2X and ÷2 the System 'Q' Frequency. Also a Q (180° Phase Shift) Output Available.
- All Outputs Have ±36mA Drive (Equal High and Low) CMOS Levels. Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL–Level Compatible
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing
- Special Power–Down Mode With 2X_Q, Q0, and Q1 Being Reset (With $\overline{MR}$), and Other Outputs Remain Running. 2X_Q, Q0 and Q1 Are Guaranteed to Be in Lock 3 Clock Cycles After MR Is Negated

Three 'Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. The $\overline{Q3}$ output is inverted (180° phase shift) from the 'Q' outputs. A 2X_Q output runs at twice the 'Q' output frequency. The 2X_Q output is ideal for 68040 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 20 and 25MHz 68040. The Q/2 output runs at 1/2 the 'Q' frequency. This output is fed back internally, providing a fixed 2X multiplication from the 'Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88920 in a static 'test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The $\overline{RST}\_\overline{OUT}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{RST}\_IN$ pin is held high, the open drain $\overline{RST}\_\overline{OUT}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{RST}\_\overline{OUT}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the RST_IN pin is toggled low, and the $\overline{RST}\_\overline{OUT}$(LOCK) pin will stay low for 1024 cycles of the 'Q' output frequency after the RST_IN pin is brought back high.

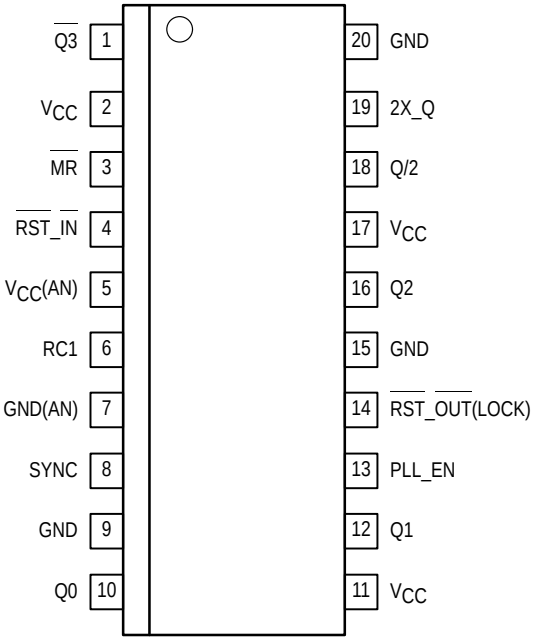
Description of the $\overline{RST}$_IN/$\overline{RST}$_$\overline{OUT}$(LOCK) Functionality

The $\overline{RST}\_IN$ and $\overline{RST}\_\overline{OUT}$(LOCK) pins provide a 68030/040 processor reset function, with the $\overline{RST}\_\overline{OUT}$ pin also acting as a lock indicator. If the RST_IN pin is held high during system power–up, the RST_OUT pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 'Q' output cycles after phase–lock is achieved the RST_OUT(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the RST_OUT(LOCK) pin). If the RST_IN pin is held low during power–up, the RST_OUT(LOCK) pin will remain low.

Power–Down Mode Functionality

The MC88920 has a special feature designed in to allow the processor clock inputs to be reset for total processor power–down, and then to return to phase–locked operation very quickly when the processor is powered–up again.

The MR pin resets outputs 2X_Q, Q0 and Q1 only leaving the other outputs operational for other system activity. When MR is negated, all outputs will be operating normally within 3 clock cycles.



Pinout: 20–Lead Wide SOIC Package (Top View)

Description of the RST_IN/RST_OUT(LOCK) Functionality (continued)

After the system start–up is complete and the 88920 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88920 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start–up

Because the RST_OUT(LOCK) pin is an indicator of phase–lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start–up (power–up). With the recommended loop filter values (see Figure 7) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when VCC reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88920 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power–up, the V_{CC} ramp rate must be less than 10mS for proper '030/040 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start–up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

CAPACITANCE AND POWER SPECIFICATIONS

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	5.0 ±10%	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	4.75 5.25	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	4.75 5.25	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	4.75 5.25	4.01 4.51	V	V_{IN} = V_{IH} or V_{IL} I_{OH} –36mA –36mA
V_{OL}	Minimum Low Level Output Voltage	4.75 5.25	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH} +36mA[1] +36mA
I_{IN}	Maximum Input Leakage Current	5.25	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.25	2.0 [2]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	5.25	88	mA	V_{OLD} = 1.0V Max
I_{OHD}		5.25	–88	mA	V_{OHD} = 3.85 Min
I_{CC}	Maximum Quiescent Supply Current	5.25	750	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

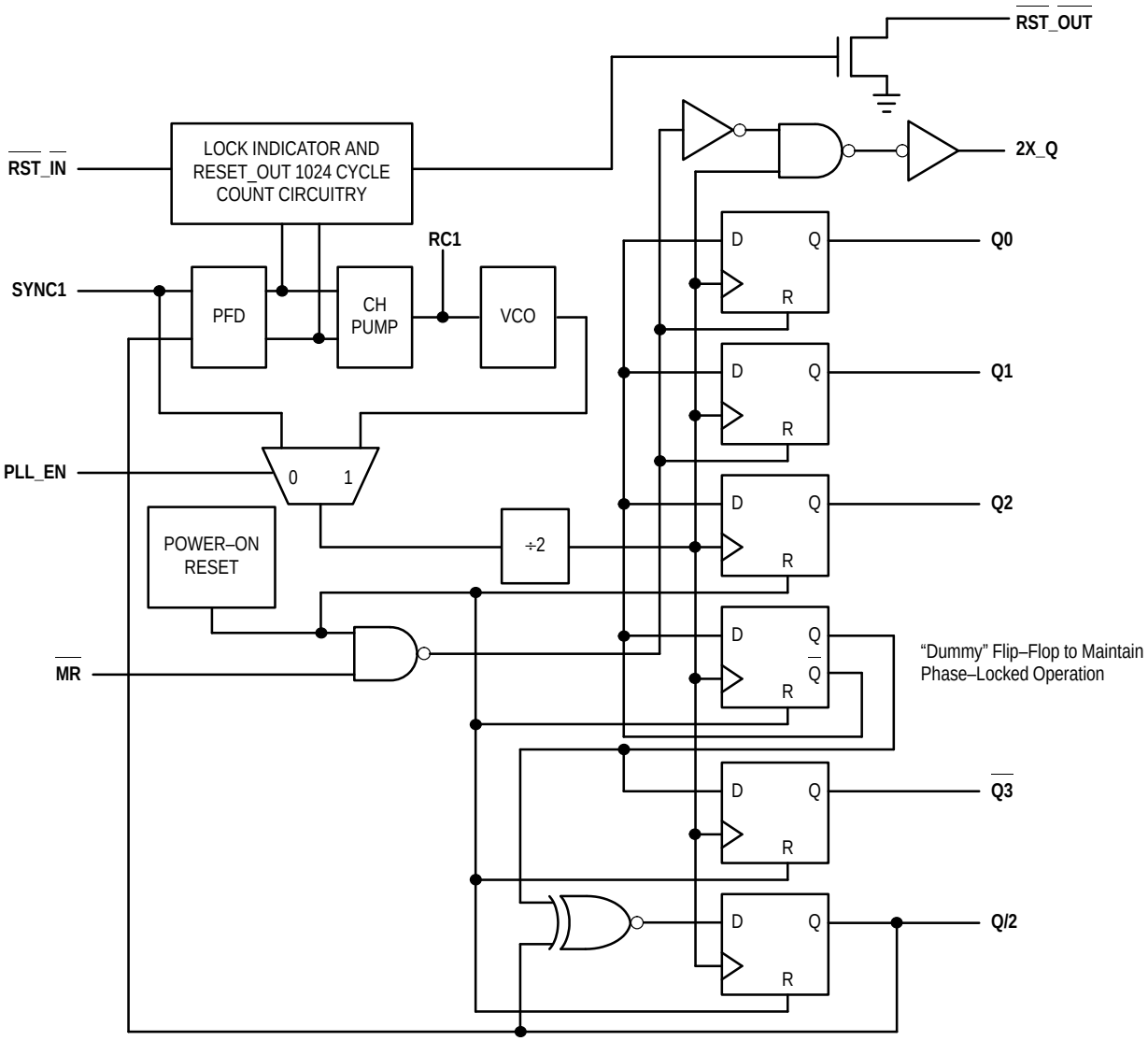


Figure 1. MC88920 Logic Block Diagram

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q}/4}$	200	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	50	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q2, Q3 Outputs	25	MHz

1. Maximum Operating Frequency is guaranteed with the 88920 in a phase–locked condition, and all outputs loaded at 50pF.

AC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Mimimum	Maximum	Unit	Condition
$t_{RISE/FALL}$[1] All Outputs	Rise/Fall Time, All Outputs into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20pF Load, With Termination Specified in AppNote 3	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, Q3)	Output Pulse Width Q0, Q1, Q2, Q3 at $V_{CC}/2$	$0.5t_{cycle} - 0.5$[5]	$0.5t_{cycle} + 0.5$[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at $V_{CC}/2$	$0.5t_{cycle} - 0.5$[5]	$0.5t_{cycle} + 0.5$[5]	ns	50Ω Load Terminated to $V_{CC}/2$ (See Application Note 3)
t_{PD}[1,4] SYNC – Q/2	SYNC Input to Q/2 Output Delay (Measured at SYNC and Q/2 Pins)	–0.75	–0.15	ns	With 1MΩ From RC1 to An V_{CC} (See Application Note 2)
		+1.25 [7]	+3.25 [7]	ns	With 1MΩ From RC1 to An GND (See Application Note 2)
t_{SKEWr}[1,2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2, Q/2 (Rising Edge Only)	—	500	ps	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{SKEWf}[1,2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
$t_{SKEWall}$[1,2]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q2 Rising Q3 Falling	—	1.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$ (See Timing Diagram in Figure 6)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q	Propagation Delay, MR to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{REC}, $\overline{MR}$ to SYNC[6]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	—	ns	
t_{REC}, $\overline{MR}$ to Normal Operation	Recovery Time for Outputs 2X_Q, Q0, Q1 to Return to Normal PLL Operation	—	3 Clock Cycles (Q Frequency)	ns	
t_W, $\overline{MR}$ LOW[6]	Minimum Pulse Width, $\overline{MR}$ input Low	5	—	ns	
t_W, $\overline{RST\_IN}$ LOW	Minimum Pulse Width, $\overline{RST\_IN}$ Low	10	—	ns	When in Phase–Lock
t_{PZL}	Output Enable Time $\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}	Output Enable Time $\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z	1016 ‘Q’ Cycles (508 Q/2 Cycles)	1024 ‘Q’ Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1µF; t_{LOCK} Min is with C1 = 0.01µF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Refer to Application Note 3 to translate signals to a 1.5V threshold.
6. Specification is valid only when the PLL_EN pin is low.
7. This is a typical specification only, worst case guarantees are not provided.

Application Notes

1. Several specifications can only be measured when the MC88920 is in phase–locked operation. It is not possible to have the part in phase–lock on ATE (automated test equipment). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88920 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. IC performance to each specification and fab variation were used to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 1MΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 2, is required to ensure no jitter is present on the MC88920 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 2 for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88920 meets the 20MHz and 25MHz 68040 P–Clock input specification (at 40MHz and 50MHz). For these two specs to be guaranteed by Motorola, the termination scheme shown in Figure 3 must be used. For applications which require 1.5V thresholds, but do not require a tight duty cycle the R_P resistor can be ignored.
4. The t_{PD} spec (SYNC to Q/2) guarantees how close the Q/2 output will be locked to the reference input connected to the SYNC input (including temperature and voltage variation). This also tells what the skew from the Q/2 output on one part connected to a given reference input, to the Q/2 output on one or more parts connected to that reference input (assuming equal delay from the referenceinput to the SYNC input of each part). Therefore the t_{PD} spec is equivalent to a part–to–part specification. However, to correctly predict the skew from a given output on one part to any other output on one or more other parts, the distribution of each output in relation to the SYNC input must be known. This distribution for the MC88920 is provided in Table 1.

TABLE 1. Distribution of Each Output versus SYNC

Output	–(ps)	+(ps)
2X_Q	TBD	TBD
Q0	TBD	TBD
Q1	TBD	TBD
Q2	TBD	TBD
Q3	TBD	TBD
Q/2	TBD	TBD

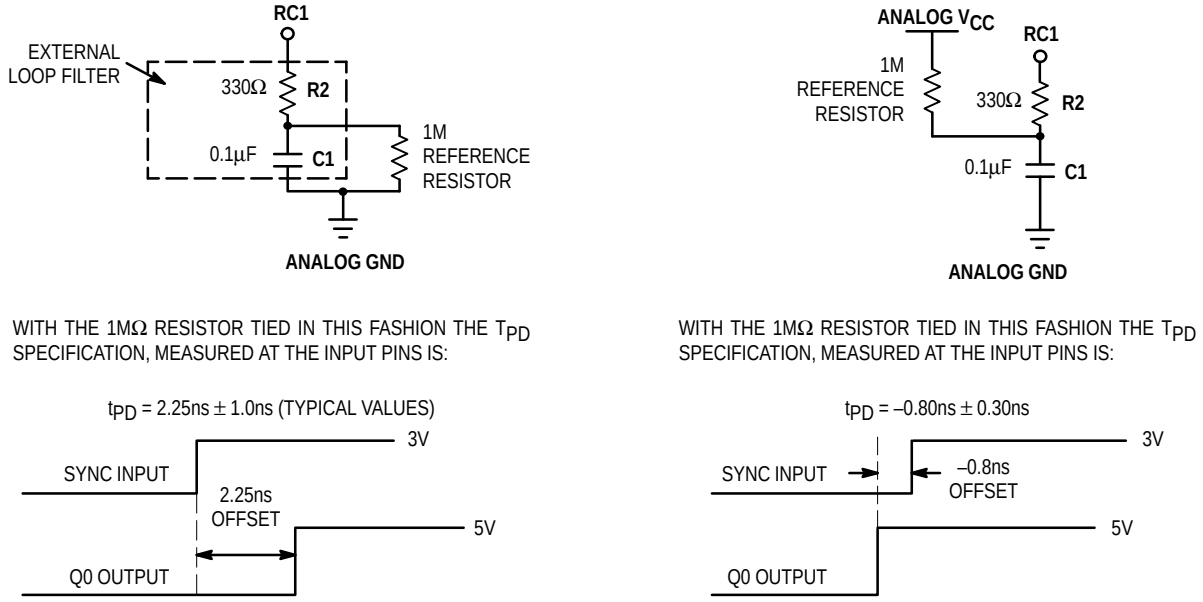


Figure 2. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 1MΩ Resistor Is Tied to V_{CC} or Ground

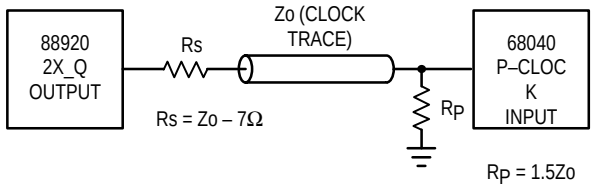


Figure 3. MC68040 P–Clock Input Termination Scheme

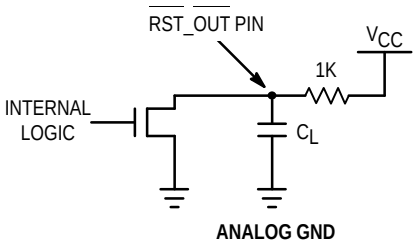


Figure 4. RST_OUT Test Circuit

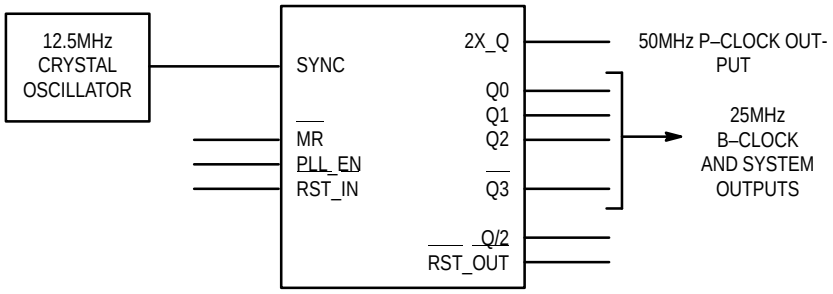


Figure 5. Logical Representation of the MC88920 With Input/Output Frequency Relationships

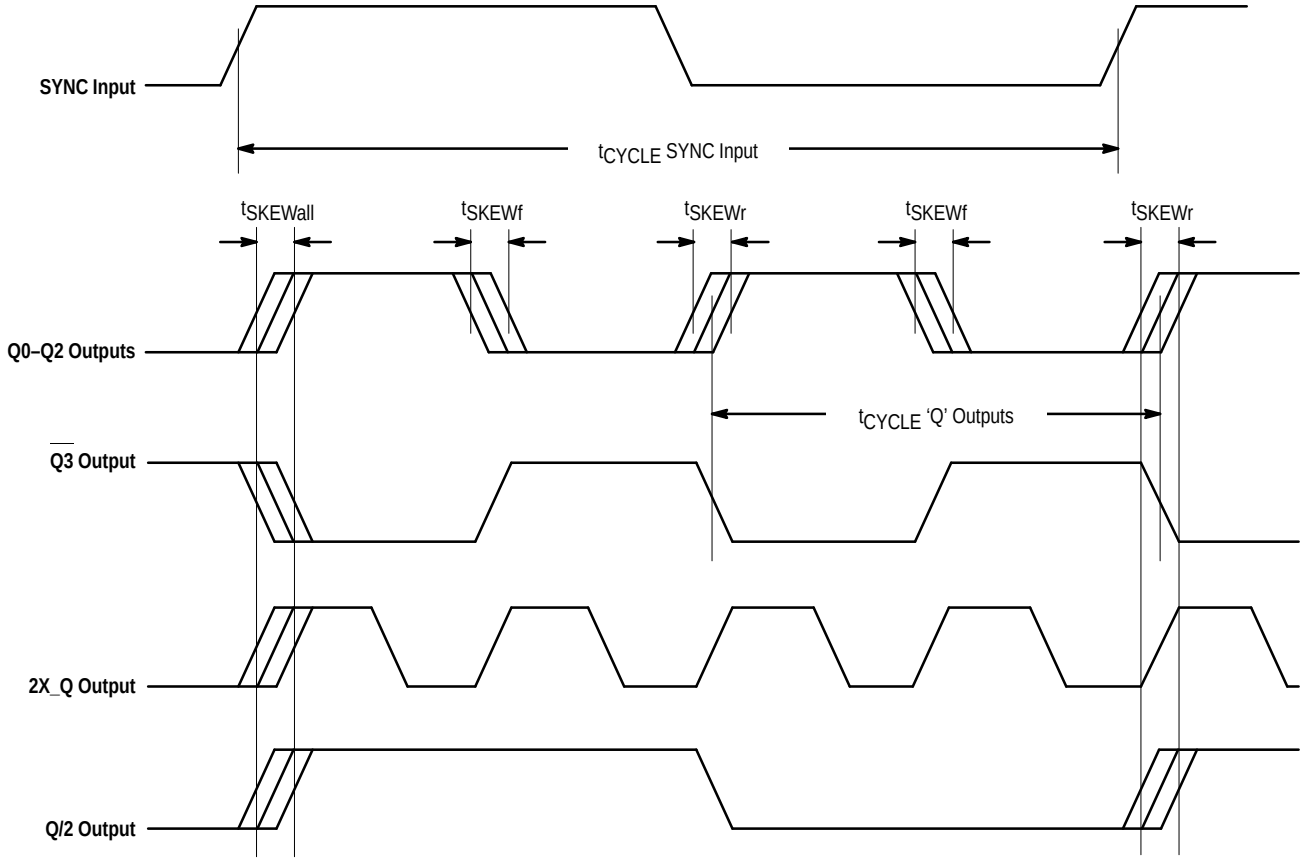


Figure 6. Output/Input Switching Waveforms and Timing Relationships

Timing Notes

1. The MC88920 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 4.75V to 5.25V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{RST}$_$\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the RST_OUT pin when it goes into the high impedance state (after the MC88920 is phase–locked to the reference input with RST_IN held high or 1024 'Q' cycles after the RST_IN pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 4.

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 7 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88920 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88920 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88920's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 7 is to give the 88920 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1M and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1M resistor provides the correct amount of current injection into the charge pump (2–3μA).

2. In addition to the bypass capacitors used in the analog filter of Figure 7, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88920 outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88920 package as possible.

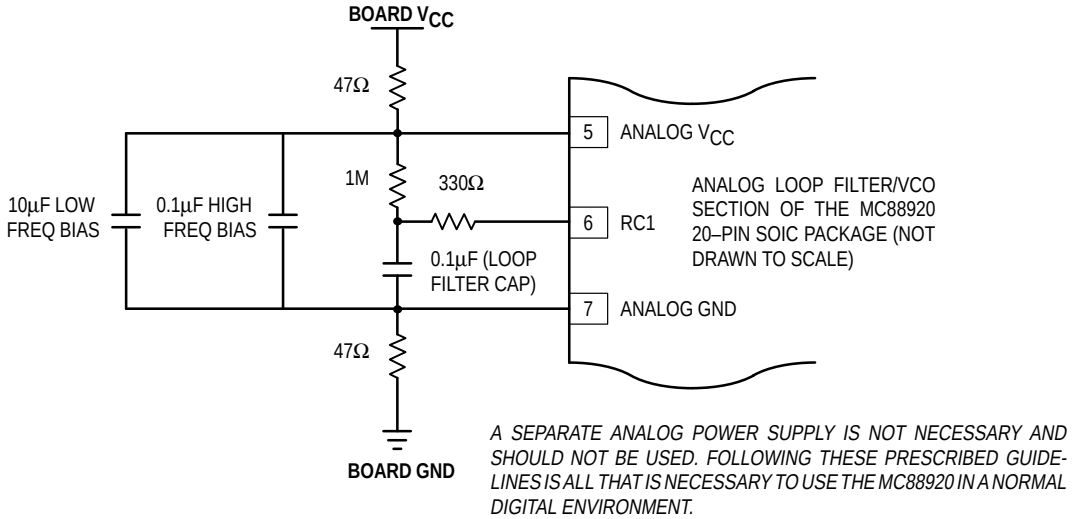


Figure 7. Recommended Loop Filter and Analog Isolation Scheme for the MC88920

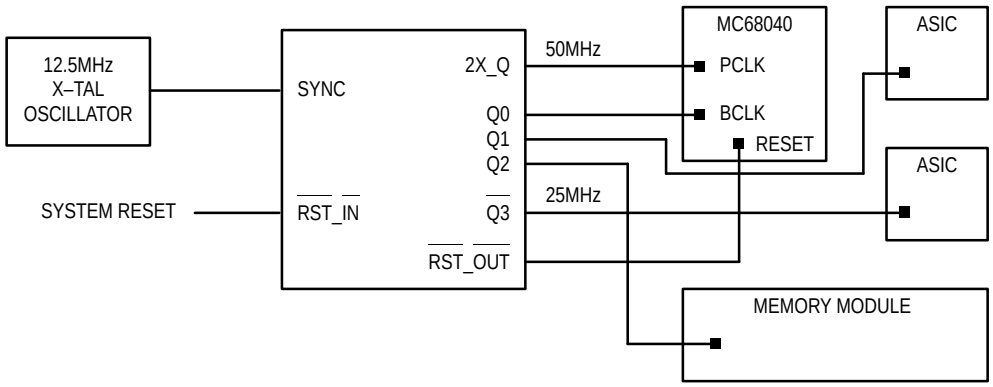
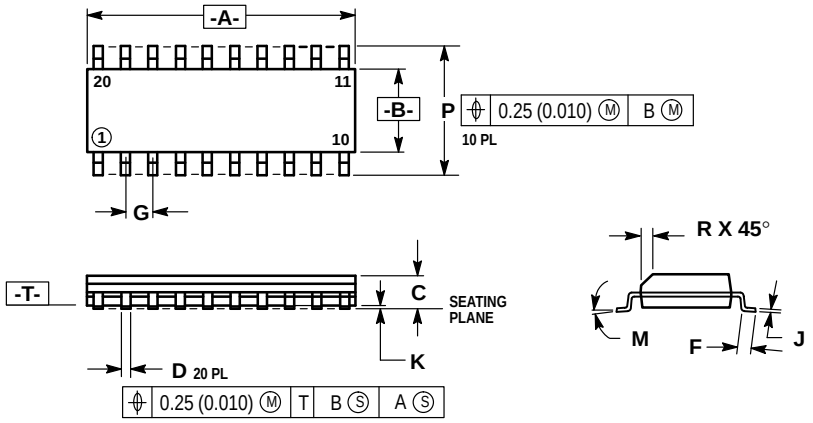


Figure 8. Typical MC88920/MC68040 System Configuration

OUTLINE DIMENSIONS

DW SUFFIX
SOIC PACKAGE
CASE 751D-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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