

# MC92314

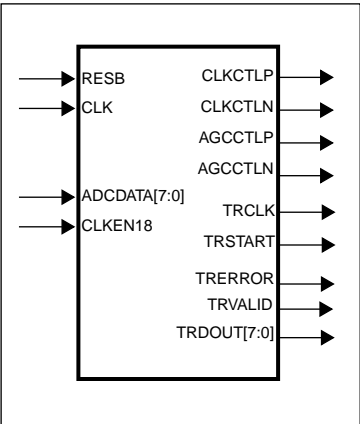
## Advance Information

# 2K Integrated DVB-T Demodulator

The MC92314 is a DVB-T compliant demodulator for 2K transmission mode according to the ETSI specification for digital terrestrial broadcasting (ETS 300744). The MC92314 contains all the functionality required to demodulate and decode DVB-T compliant broadcast signals.

### Feature Summary

- Usable for 8MHz/7MHz/6MHz channels by adjusting the clock rate
- Digital I/Q separation on-chip
- Digital AFC on chip
- Supports QPSK, 16-QAM and 64-QAM (non-hierarchical)
- Supports all guard interval lengths (1/32, 1/16, 1/8, 1/4)
- Automatic locking to any DVB-T guard interval
- Accepts 8-bit TTL-compatible twos-complement and offset-binary data input
- Provides control signals for AGC and ADC clock frequency control
- Viterbi Decoder for DVB convolutional code rates 1/2, 2/3, 3/4, 5/6 and 7/8
- Reed/Solomon Decoder for DVB Reed-Solomon code (204,188,8)
- I<sup>2</sup>C serial bus compatible interface (M-Bus) for external programming and control
- Operating voltage 3.3V
- Power requirement 1.7W
- Package 160PQFP



### Ordering Information

Device	Package
MC92314DH	160PQFP

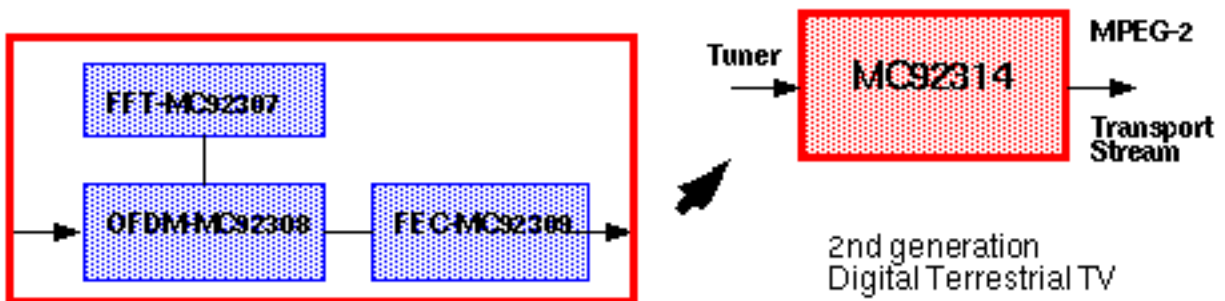


Figure 1. DVB-T Demodulator Block Diagram



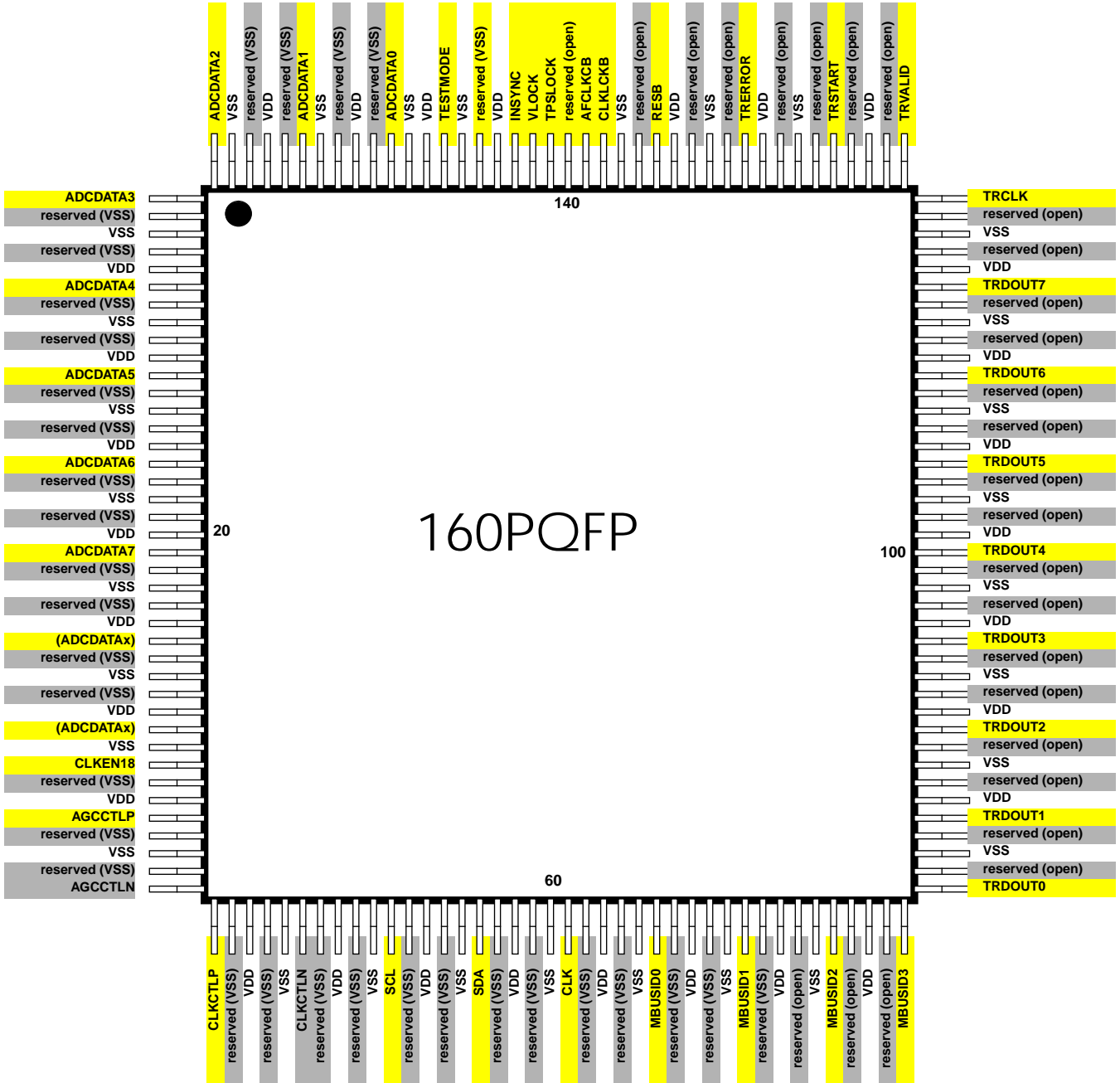


Figure 2. Pinout of the MC92314

**Table 1. MC92314 Pin List**

SIGNAL	FUNCTIONALITY	TYPE	POLTY
CLK	Common clock input (36.57 MHz)	TTL - IN	high
RESB	Reset (asynchronous)	TTL - IN	low
CLKEN18	ADC data strobe	TTL - IN	high
ADCDATA[7:0]	Input for samples from ADC	TTL - IN	high
CLKCTLP	ADC clock synchronization loop (+)	TTL - OUT	high
CLKCTLN	ADC clock synchronization loop (-)	TTL - OUT	low
AGCCTLP	Analog AGC loop (+)	TTL - OUT	high
AGCCTLN	Analog AGC loop (-)	TTL - OUT	low
MSDA	I <sup>2</sup> C compatible control bus, data pin	TTL - OD	-
MSCL	I <sup>2</sup> C compatible control bus, clock pin	TTL - IN	high
MBUSID[3:0]	I <sup>2</sup> C compatible control bus, variable ID selector	TTL - IN	high
TRERROR	MPEG2 Frame Error Indicator	TTL - OUT	high
TRVALID	MPEG2 Byte Valid Indicator	TTL - OUT	high
TRSTART	MPEG2 Sync Byte Indicator	TTL - OUT	high
TRCLK	MPEG2 Byte Clock	TTL - OUT	high
TRDOUT[7:0]	MPEG2 Transport Stream Byte Output	TTL - OUT	high
INSYNC	FEC Frame Synchronization Status	TTL - OUT	high
VLOCK	Viterbi Decoder Synchronization Status	TTL - OUT	high
TPSLOCKB	TPS Data Valid indicator (inverted)	TTL - OUT	high
AFCLCK	AFC lock indicator	TTL - OUT	high
CLKLCK	Time Synchronization lock indicator	TTL - OUT	high

**Table 2. FEC I<sup>2</sup>C Register Map:**

Addr	Name	Type	Def	b7	b6	b5	b4	b3	b2	b1	b0		
0	CONFIG_VIT	R/W		DAP	DLT	DDEC	DTHR	IFS	VSYNC[2:0]				
1	THRESHOLD	R/W					THRES[4:0]						
2	DECREMENT	R/W					DEC[4:0]						
3	TIMEOUT	R/W						TIM[3:0]					
4	AVG_PERIOD	R/W						PERIOD[3:0]					
8	QVALLSB	R		QVAL[7:0]									
9	QVALMSB	R			QVAL[14:8]								
\$A	SYNC_VIT	R						VLCK					
\$B	SELECTEDRATE	R								SR[2:0]			
\$C	FIFO_STATE	R									VFF	VEF	
\$11	AQ_THRESH	R/W		SYNC[2:0]			REF[4:0]						
\$12	TR_THRESH	R/W		SYNC[2:0]			REF[4:0]						
\$13	TIME_COUNT	R/W		TC[7:0]									
\$18	BER_COUNT	R		BER[7:0]									
\$19	BAD_COUNT	R						BAD[3:0]					
\$1A	SYNC_RS	R		0	0	0	0	0	RERRU	DEINT	INSYNC		
\$1F	SOFT_RESET	R/W		GP3	GP2	GP1	GP0		FFT	RS	VIT		

**Table 3. OFDM I<sup>2</sup>C Registers**

Addr	Name	Type	Def	b7	b6	b5	b4	b3	b2	b1	b0	
0	TPS R0	R	-	S[7:0]								
1	TPS R1	R	-	S[15:8]								
2	TPS R2	R	-	S[23:16]								
3	TPS R3	R	-	S[31:24]								
4	TPS R4	R	-	S[39:32]								
5	TPS R5	R	-	S[47:40]								
6	TPS R 6	R	-	S[55:48]								
7	TPS R7	R	-	S[63:56]								
8	TPS R 8	R	-	AFCL	CLKL	TPSV	TPSL	S[67:64]				
9	TPS Idx	W	-	IDX[7:0]								
\$A	Reset	W	-									SRES
\$B	OFDM R0	W	-	CODERATE				GUARD		CONST		
\$C	OFDM R1	W	\$1F	00	0	FROT	ASYN	ATPS	AFC	TSM		
\$D	OFDM R2	W	\$B4	1	AFCS	AGCS	10	UHFI	ADCM	CLKS		

**I<sup>2</sup>C Programming:**

The MC92314 2K Integrated DVB-T Demodulator can be programmed serially over an I<sup>2</sup>C bus protocol. It contains two independent I<sup>2</sup>C controllers (one for the FEC and one for the OFDM), each with a distinct slave address in the I<sup>2</sup>C address space. The primary pins MBUSID[3:0] can be used to resolve potential slave address conflicts in an I<sup>2</sup>C based system. The addressing convention is such that an I<sup>2</sup>C slave address is given by

Module selected	ADR[6:4]	ADR[3:0]
FEC	001	MBUSID[3:0]
OFDM	010	MBUSID[3:0]

The Register Address space under each I<sup>2</sup>C slave address is defined for the FEC in Table 2 and for the OFDM in Table 3. Please note that to access any register, the procedure requires that this register number has to be written into a symbolic address \$0 in the first slave access; a second slave access can then proceed with the read or write of the desired register(s). Please note, that for the FEC a soft reset is only possible in normal operation of the OFDM, i.e. with the TPSLOCKB signal active.

**Operation:**

The MC92314 2K Integrated DVB-T Demodulator is preconfigured such that only minimal setup programming is required. The rate selection of the FEC is automatic. If an ADC with 'offset-binary' coding is used, OFDM register 2 (\$D) must be set accordingly. No further programming is necessary.

The locking process of the MC92314 2K Integrated DVB-T Demodulator during startup can be observed externally by monitoring the pins TPSLOCKB, VLOCK and INSYNC. For error free operation TPSLOCKB should be low, VLOCK should be high and INSYNC should be high.

**Home Page:**

[www.freescale.com](http://www.freescale.com)

**email:**

[support@freescale.com](mailto:support@freescale.com)

**USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
 Technical Information Center, CH370  
 1300 N. Alma School Road  
 Chandler, Arizona 85224  
 (800) 521-6274  
 480-768-2130

[support@freescale.com](mailto:support@freescale.com)

**Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
 Technical Information Center  
 Schatzbogen 7  
 81829 Muenchen, Germany  
 +44 1296 380 456 (English)  
 +46 8 52200080 (English)  
 +49 89 92103 559 (German)  
 +33 1 69 35 48 48 (French)

[support@freescale.com](mailto:support@freescale.com)

**Japan:**

Freescale Semiconductor Japan Ltd.  
 Headquarters  
 ARCO Tower 15F  
 1-8-1, Shimo-Meguro, Meguro-ku  
 Tokyo 153-0064, Japan  
 0120 191014  
 +81 2666 8080

[support.japan@freescale.com](mailto:support.japan@freescale.com)

**Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
 Technical Information Center  
 2 Dai King Street  
 Tai Po Industrial Estate,  
 Tai Po, N.T., Hong Kong  
 +800 2666 8080

[support.asia@freescale.com](mailto:support.asia@freescale.com)

**For Literature Requests Only:**

Freescale Semiconductor  
 Literature Distribution Center  
 P.O. Box 5405  
 Denver, Colorado 80217  
 (800) 441-2447  
 303-675-2140  
 Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document. Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

