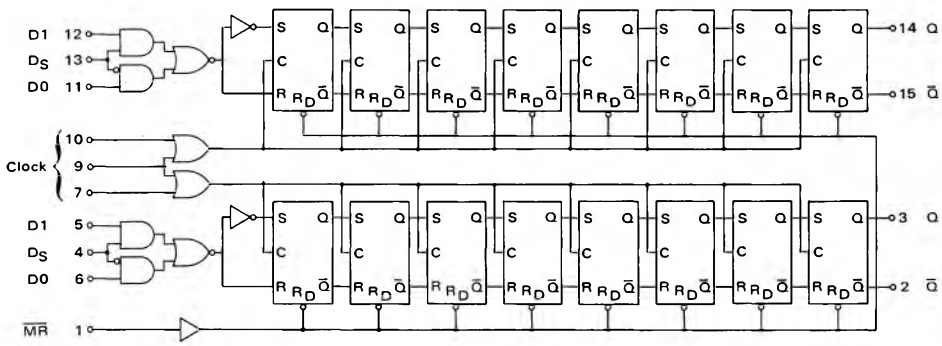
MC9328L*
MC8328L,P*

Input Loading Factors:
$\overline{MR}$, D0, D1 = 1
D_S = 2
Clock – Pins 7, 10 = 1.5
Pin 9 = 3
Output Loading Factor = 6

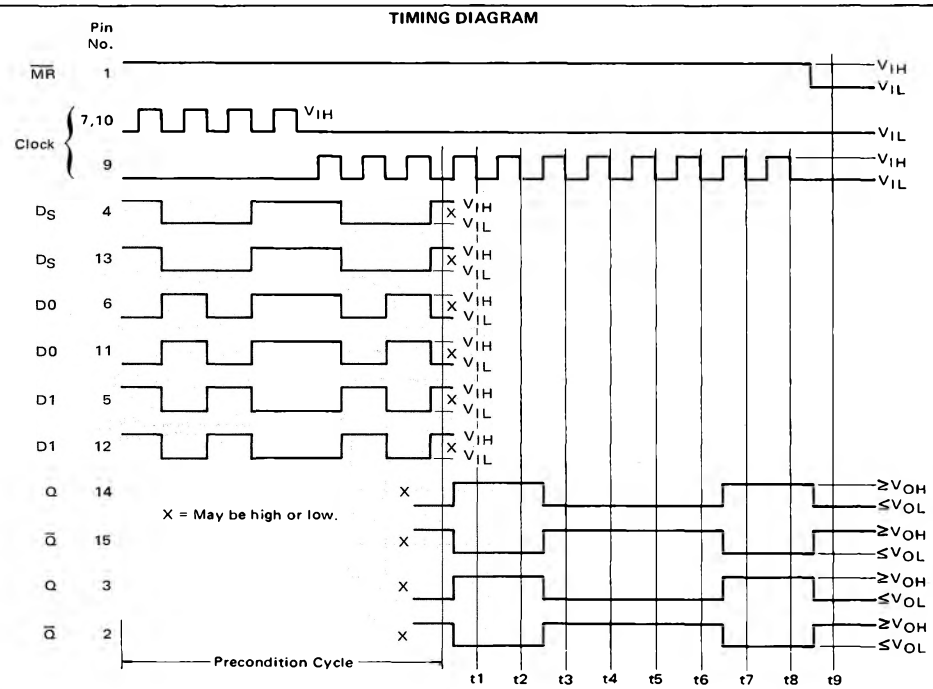
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = :
Clock to Output, t_{pd-} = 22 ns typ
t_{pd+} = 13 ns typ
$\overline{MR}$ to Output, t_{pd-} or t_{pd+} = 35 ns typ

The MC9328/8328 is a monolithic dual 8-bit serial shift register. Each 8-bit register is provided with a 2-input multiplexer circuit and complementary serial outputs. The two registers can be clocked together with a common line, or clocked separately with separate lines. A common Master Reset input is active in the low level and overrides all other inputs.

V_{CC} = Pin 16
GND = Pin 8



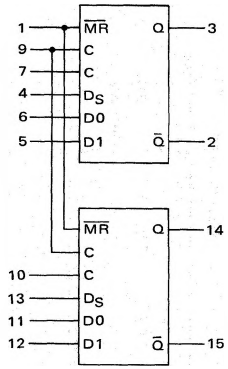
TIMING DIAGRAM



*L suffix = 16-pin dual in-line ceramic package (Case 620).
P suffix = 16-pin dual in-line plastic package (Case 612).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output of one half of the device. To complete testing, sequence through other inputs and outputs in the same manner

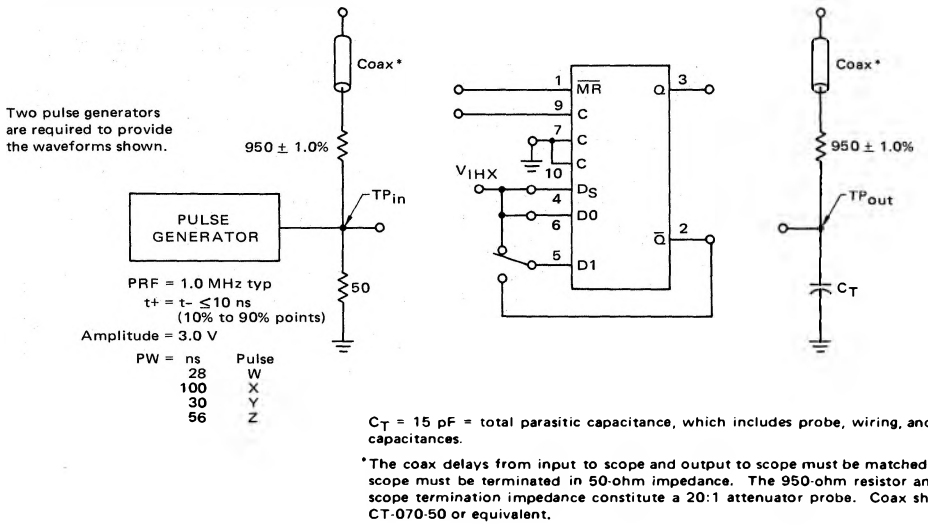


@ Test Temperature		I_{OL1} mA	I_{OL2} mA	I_{OH} mA	I_D mA	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts
MC9328	-55°C	7.44	9.6	-0.36	–	0.80	2.0	0.4	4.5	–	4.5	5.5
	+25°C	7.44	9.6	-0.36	-10	0.90	1.7	0.4	4.5	5.0	4.5	5.5
	+125°C	7.44	9.6	-0.36	–	0.80	1.4	0.4	4.5	–	4.5	5.5
MC8328	0°C	8.5	9.6	-0.36	–	0.85	1.9	0.45	4.5	–	4.75	5.25
	+25°C	8.5	9.6	-0.36	-10	0.85	1.8	0.45	4.5	5.0	4.75	5.25
	+75°C	8.5	9.6	-0.36	–	0.85	1.6	0.45	4.5	–	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9328 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8328 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																											
Forward Current	I_F	1	–	-1.6	–	-1.6	–	-1.6	mAdc	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	–	1	–	–	–	16	8
		4	–	-3.2	–	-3.2	–	-3.2	↓	–	-3.2	–	-3.2	–	-3.2	↓	–	–	–	–	–	–	4	–	–	–	↓	↓
		7	–	-2.4	–	-2.4	–	-2.4		–	-2.4	–	-2.4	–	-2.4		–	–	–	–	–	–	7	–	–	–		
		9	–	-4.8	–	-4.8	–	-4.8		–	-4.8	–	-4.8	–	-4.8		–	–	–	–	–	–	9	–	–	–		
Leakage Current	I_R	1	–	60	–	60	–	60	µAdc	–	60	–	60	–	60	µAdc	–	–	–	–	–	–	–	1	–	–	16	8
		4	–	120	–	120	–	120	↓	–	120	–	120	–	120	↓	–	–	–	–	–	–	–	4	–	–	↓	↓
		7	–	90	–	90	–	90		–	90	–	90	–	90		–	–	–	–	–	–	–	7	–	–		
		9	–	180	–	180	–	180		–	180	–	180	–	180		–	–	–	–	–	–	–	9	–	–		
Clamp Voltage	V_D	1	–	–	–	-1.5	–	–	Vdc	–	–	–	-1.5	–	–	Vdc	–	–	–	1	–	–	–	–	–	16	–	8
Output																											
Output Voltage	V_{OL1}	3	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	3	–	–	See Timing Diagram						16	–	7,8,10
	V_{OL2}	3	–	0.40	–	0.40	–	0.40	Vdc	–	0.45	–	0.45	–	0.45	Vdc	–	3	–	See Timing Diagram						–	16	7,8,10
	V_{OH}	3	2.4	–	2.4	–	2.4	–	Vdc	2.4	–	2.4	–	2.4	–	Vdc	–	–	3	See Timing Diagram						16	–	7,8,10
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	16	–	–	–	73	–	–	mAdc	–	–	–	73	–	–	mAdc	–	–	–	–	–	–	–	–	16	–	–	8
Switching Parameters																	Pulse In*		Pulse Out	V_{IHX} = 2.4 Vdc						#	##	
Turn-On Delay C to Q	t_{pd-}	3	–	–	–	44	–	–	ns	–	–	–	44	–	–	ns	9 (W)		3	1, 4, 6, 11, 13					16	2, 5	12, 15	7,8,10
Turn-Off Delay C to Q	t_{pd+}	3	–	–	–	26	–	–	ns	–	–	–	26	–	–	ns	9 (W)		3	1, 4, 6, 11, 13					16	2, 5	12, 15	7,8,10
Turn-On Delay $\overline{MR}$ to Q	t_{pd-}	3	–	–	–	70	–	–	ns	–	–	–	70	–	–	ns	1 (Y), 9 (X)		3	4, 5, 6, 11, 12, 13					16	–	–	7,8,10
Turn-On Delay $\overline{MR}$ to Q	t_{pd-}	3	–	–	–	70	–	–	ns	–	–	–	70	–	–	ns	1 (Z), 9 (X)		3	4, 5, 6, 11, 12, 13					16	–	–	7,8,10

*Letters in parenthesis refer to waveform.
#These pins tied together
##These pins tied together

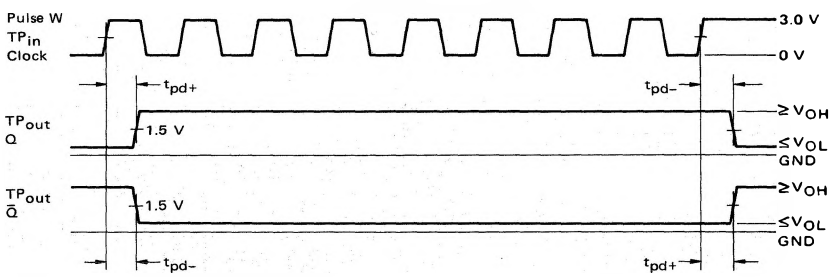
SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

CLOCK PROPAGATION DELAY



MASTER RESET PROPAGATION DELAY