MC9S12XF512PB
Rev. 1, 06-Dec-2006

16-bit S12X Microcontroller Family with Integrated FlexRay Interface

Covers MC9S12XF512, MC9S12XF384, MC9S12XF256 and MC9S12XF128

Introduction

Targeted at actuators, sensors and other distributed nodes in the FlexRay network for Chassis and Body Electronics, the MC9S12XF-Family will deliver 32-bit performance with all the advantages and efficiencies of a 16-bit MCU. The design goal is to retain the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Freescale Semiconductor's existing 16-bit MC9S12 MCU families.

Based around an enhanced S12X core, the MC9S12XF-Family will run 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12XF-Family also features a new flexible interrupt handler, which allows multilevel nested interrupts.

The MC9S12XF-Family features the performance boosting enhanced XGATE co-processor. The XGATE is programmable in “C” language and runs at twice the bus frequency of the S12. Its instruction set is optimized for data movement, logic and bit manipulation instructions. Any peripheral module can be serviced by the XGATE.

The MC9S12XF-Family features a FlexRay module for high speed serial communication supporting various bit rates up to 10 Mbit/s. The FlexRay clock can be derived from crystals ranging from 4MHz to 40MHz for cost and EMC optimization using an Internal PLL (IPLL). The 64-pin LQFP allows interfacing to a single FlexRay channel. The 64-pin LQFP (10mm x 10mm) is intended for those applications challenged by the size constraint of some satellite FlexRay modules. The 112-pin LQFP offer increase number of I/Os as well as 16 A/D channels, in addition to that the 144-pin LQFP provides a full 16-bit wide non-multiplexed external bus interface with the pins usable in single-chip mode as general purpose I/O.

NOTE

The 144-Pin LQFP version will not be qualified for production and is intended to be used for emulation (development tools) only.

The MC9S12XF-Family features the MSCAN module with a FIFO receiver buffer arrangement, and input filters optimized for Gateway applications handling numerous message identifiers.

The MCU9S12XF Family provides Flash memory sizes from 128K throughout 512K non volatile memory together with enhanced EEPROM functionality (EE-Emulation) with built in Error Correcting Code (ECC).The memory uses Freescale Semiconductor's industry-leading, full automotive qualified SG-Flash.

The inclusion of a frequency modulated PLL circuit allows power consumption and performance to be adjusted to suit operational requirements and allows optimization of the radiated emissions (EMC).

The ADC now offers 12 Bit resolution at a conversion rate down to 3µs per channel.

The Enhanced Programmable Interrupt Timer offers the possibility to schedule up to 3 ADC trigger events after an initial PMF or PIT sync event. Additional trigger events can be scheduled via software.

In addition to the I/O ports available in each module, up to eleven further I/O ports are available with interrupt capability allowing wake-up from STOP or WAIT mode.

Features

Features of the MC9S12XF-Family are listed here. Please see Table 1 for memory options and Table 2 for the peripheral features that are available on the different family members.

16-Bit CPU12X	• Upward compatible with MC9S12 instruction set • Enhanced indexed addressing • Additional (superset) instructions to improve 32-bit calculations and semaphore handling • Access large data segments independent of PPAGE • **Note:** Five Fuzzy instructions are removed (MEM, WAV,WAVR, REV, REVW)
Enhanced Interrupt Module	• Eight levels of nested interrupt • Flexible assignment of interrupt sources to each interrupt level. • One non-maskable high priority interrupt (XIRQ) • Wake-up Interrupt Inputs – IRQ and non-maskable XIRQ
XGATE	• Programmable, high performance I/O coprocessor module – up to 100 MIPS RISC performance • Transfers data to or from all peripherals and RAM without CPU intervention or CPU wait states • Performs logical, shifts, arithmetic, and bit operations on data • Can interrupt the HCS12X CPU signalling transfer completion • Triggers from any hardware module as well as from the CPU possible • **NEW!** Two interrupt levels to service high priority tasks • Enables Full CAN capability when used in conjunction with MSCAN module • Full LIN master or slave capability when used in conjunction with the integrated LIN SCI module
System Integrity Support	• Power-on reset (POR) • Illegal address detection with reset • Low-voltage detection with interrupt or reset • Computer Operating Properly (COP) watchdog – configurable as window COP for enhanced failure detection – Can be initialized out of reset using option bits located in Flash • Clock monitor supervising the correct function of the oscillator

Memory Options	• Crossbar architecture for efficient data flow • 128K, 256k, 384K and 512K byte Flash • 2K, 4K byte Emulated EEPROM • 16K, 24K and 32K Byte RAM • Flash General Features – **NEW!** 64 data bits plus 8 syndrome ECC (Error Correction Code) bits allow single bit error correction and double fault detection – Erase sector size 1024 bytes – Automated program and erase algorithm – Security option to prevent unauthorized access – Sense-amp margin level setting for reads • **NEW!** Data Flash General Features – Up to 32K bytes of D-Flash memory with 256-byte sectors for user access. – Dedicated commands to access D-Flash memory over EEE operation – Single bit fault correction and double fault detection within a word during read operations – Automated program and erase algorithm with verify and generation of ECC parity bits – Fast sector erase and word program operation – Ability to program up to four words in a burst sequence • **NEW!** Emulated EEPROM General Features – Automatic EEE file handling using internal Memory Controller – Automatic transfer of valid EEE data from D-Flash memory to buffer RAM on reset – Ability to monitor the number of outstanding EEE related buffer RAM words left to be programmed into D-Flash memory – Ability to disable EEE operation and allow priority access to the D-Flash memory – Ability to cancel all pending EEE operations to allow priority access to the D-Flash memory
Oscillator (OSC_LCP)	• Loop Control Pierce oscillator utilizing a 4MHz to 16MHz crystal • Good noise immunity • Full-swing Pierce option utilizing a 2MHz to 40MHz crystal • Transconductance sized for optimum start-up margin for typical crystals

Clock and Reset Generator (CRG)	• Phase-locked-loop (IPLL) clock frequency multiplier – **NEW!** Internally filtered. No external components required – Configurable option to spread spectrum for reduced EMC radiation (frequency modulation) • Fast wake up from STOP in self clock mode for power saving and immediate program execution
Non-Multiplexed External Bus (144 Pin package only)	• 16 data wide • Support for external WAIT input or internal wait cycles to adapt MCU speed to peripheral speed requirements • Up to four chip select outputs to select 16K, 768K, 2M and 4MByte address spaces • Supports glue less interface to popular asynchronous RAMs and Flash devices • External address space 4MByte for Data and Program space
FlexRay Module (FR)	• FlexRay protocol implementation according to FlexRay V2.1 Protocol Implementation document • Optimized programmers model to fit small address footprint • **NEW!** Supports Data Rates of 2.5, 5, 8 and 10MBit/s on each of the two channels • **NEW!** The FlexRay clock can be derived from crystals ranging from 4MHz to 40MHz for cost and EMC optimization using a PLL. • FlexRay clocking independent from the CPU and XGATE bus frequency • Up to two channels for fault tolerant systems (see Table 2 Peripheral Feature Summary of MC9S12XF-Family Members) • Single channel operation on channel A, configurable to run FlexRay channel A or channel B protocol • 32 configurable message buffers – Message buffers can be configured as Receive, single buffered Transmit or double buffer Transmit message buffer – Message buffer header, status and payload data stored in System RAM – 2 independent message buffer segments with configurable size of payload data section – Size of message buffer payload data section configurable from 0 up to 254 bytes • 2 independent receive FIFOs, 1 per channel • Six separate interrupt channels for Receive, receive FIFO channel A, receive FIFO channel B, Transmit, Error and Wake-up • Internal signals can be routed to I/O pins to ease debugging

Analog-to-Digital Converter (ADC)	• **NEW!** 8/10/12 Bit resolution • Multiplexer for 16 analog input channels • **NEW!** 3µs, 12-bit single conversion time • Left or right justified result data • External and internal conversion trigger capability • Internal oscillator for conversion in Stop Modes • Wake-up from low power modes on analog comparison > or <= match
Enhanced Capture Timer (ECT)	• 8 x 16-bit channels for input capture or output compare • 16-bit free-running counter with 8-bit precision prescaler • 16-bit modulus down counter with 8-bit precision prescaler • 4 x 8-bit or 2 x 16-bit pulse accumulators • Four channels have enhanced input capture capabilities: – Delay counter for noise immunity – 16-bit capture buffer – 8-bit pulse accumulator buffer
NEW! Enhanced Programmable Interrupt Timer (EPIT)	• Up to 8 timers with independent time-out periods • Time-out periods selectable between 1 and 2^{24} bus clock cycles • Time-out interrupt and peripheral triggers • 3 Sync sources (e.g. PMF) to select. • Eight time-out trigger output signals available to trigger peripheral modules. • Start of timer channels can be aligned to each other. • Start of timer channels can be aligned to an external trigger event.
Real Time Interrupt (RTI)	• Real Time Interrupt for task scheduling purposes or cyclic wake-up • Can be active in Pseudo Stop mode for low power precision timing tasks
NEW! Asynchronous Periodic Interrupt (API)	• Available in all modes including Full Stop mode • Trimmable to +-10% accuracy • Time-out periods range from 0.2ms to ~13s with a 0.2ms resolution

Pulse Width Modulator with Fault detection (PMF)	• Six channel Pulse width Modulator with Fault protection (PMF) optimized for electrical motor control • Three independent 15-bit counters with synchronous mode • Complementary channel operation • Edge and center aligned PWM signals • Programmable dead time insertion • Integral reload rates from 1 to 16 • Up to four fault protection shut down input pins depending on the package option • Up to three current sense input pins depending on the package option (see Table 3 Port and Peripheral Availability by Package Option)
Multi-scalable Controller Area Networks (MSCAN)	• CAN 2.0 A, B software compatible – Standard and extended data frames – 0 - 8 bytes data length – Programmable bit rate up to 1 Mbps • Five receive buffers with FIFO storage scheme • Three transmit buffers with internal prioritization • Flexible identifier acceptance filter programmable as: – 2 x 32-bit – 4 x 16-bit – 8 x 8-bit • Wake-up with integrated low pass filter option • Loop back for self test • Listen-only mode to monitor CAN bus • Bus-off recovery by software intervention or automatically • 16-bit time stamp of transmitted/received messages
Serial Peripheral Interface (SPI)	• Up to two SPI modules (see Table 2 Peripheral Feature Summary of MC9S12XF-Family Members) • **NEW!** configurable 8 or 16-bit data size • Full-duplex or single-wire bidirectional • Double-buffered transmit and receive • Master or Slave mode • MSB-first or LSB-first shifting • Serial clock phase and polarity options

Serial Communication Interfaces (SCI)	• Up to two SCI modules (see Table 2 Peripheral Feature Summary of MC9S12XF-Family Members) • Full-duplex or single wire operation • Standard mark/space non-return-to-zero (NRZ) format • Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths • 13-bit baud rate selection • Programmable character length • Programmable polarity for transmitter and receiver • Receive wakeup on active edge • Break detect and transmit collision detect supporting LIN
Background Debug (BDM)	• Background debug controller (BDM) with single-wire interface – Non-intrusive memory access commands – Supports in-circuit programming of on-chip non-volatile memory – Supports security
Debugger (DBG)	• Four comparators A, B, C and D – Each can monitor CPU or XGATE busses – A and C compares 23-bit address bus and 16-bit data bus with mask register – B and D compares 23-bit address bus only – Three modes: simple address/data match, inside address range or outside address range • 64 x 64-bit circular trace buffer to capture change-of-flow addresses or address and data of every access • Tag-type or force-type hardware breakpoint requests
On-Chip Voltage Regulator (VREG)	• Two parallel, linear voltage regulators with bandgap reference • Low-voltage detect (LVD) with low-voltage interrupt (LVI) • Power-on reset (POR) circuit • 3V to 5V range operation • Low-voltage reset (LVR)
Input/Output	• up to 110 general-purpose input/output (I/O) pins depending on the package option and 2 input-only pins • Hysteresis and configurable pull up/pull down device on all input pins • Configurable drive strength on all output pins
Package Options	• 144-pin low-profile quad flat-pack (LQFP) • 112-pin low-profile quad flat-pack (LQFP) • 64-pin low-profile exposed quad flat-pack (LQFP)

Operating Conditions	• Ambient temperature range –40°C to 85°C • Temperature Options: – –40°C to 105°C – –40°C to 125°C • Supply voltage range from 3.15V to 5.5V • Internal Voltage Regulator providing 1.8V logic and 3.0V Flash supply • MCU9S12XF-Family: – 40MHz maximum CPU bus frequency – 80MHz maximum XGATE bus frequency

Block Diagram

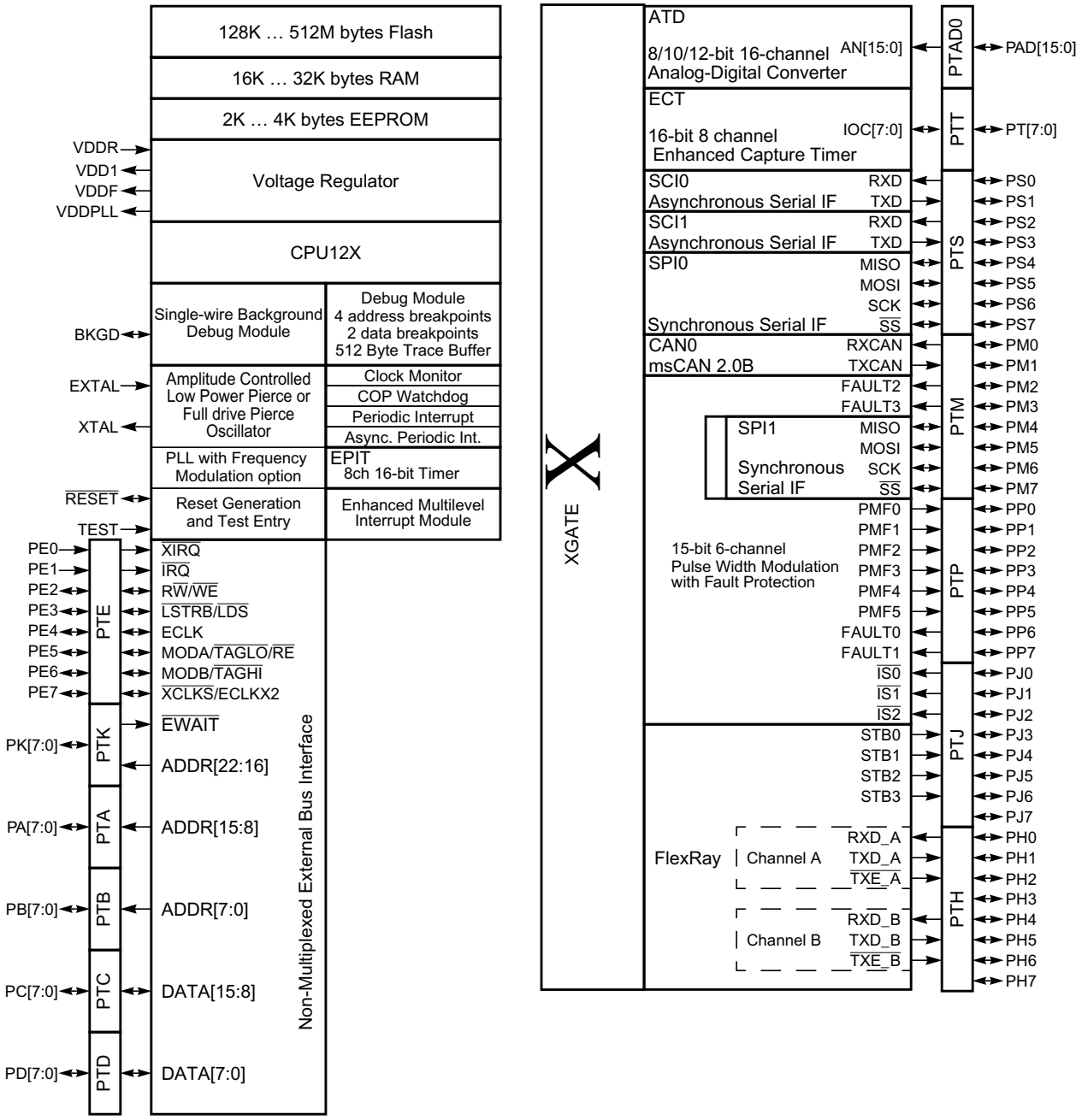


Table 1 Package and Memory Options of MC9S12XF-Family Members

Device	Package	Flash	RAM	EEPROM
9S12XF512	144 LQFP(1)	512K	32K	4K
	112 LQFP			
	64 LQFP			
9S12XF384	144 LQFP(1)	384K	24K	4K
	112 LQFP			
	64 QFP			
9S12XF256	144 LQFP(1)	256K	20K	2K
	112 LQFP			
	64 QFP			
9S12XF128	144 LQFP(1)	128K	16K	2K
	112 LQFP			
	64 QFP			

NOTES:
1. The 144-Pin LQFP version will not be qualified for production and is intended to be used for emulation (development tools) only.

Table 2 Peripheral Feature Summary of MC9S12XF-Family Members

Package	FlexRay	ECT	EPIT	CAN	SCI	SPI	A/D	PMF
144 LQFP(1)	2-ch	8ch	8ch	1	2	2	16-ch	6-ch 4 Fault Inputs 3 Current Sense
112 LQFP	2-ch	8ch	8ch	1	2	2	16-ch	6-ch 4 Fault Inputs 3 Current Sense
64 LQFP	1-ch	8ch	8ch	1	1	1	8-ch	6-ch 0 Fault Inputs 0 Current Sense

NOTES:
1. The 144-Pin LQFP version will not be qualified for production and is intended to be used for emulation (development tools) only.

Pin Assignments

Table 3 Port and Peripheral Availability by Package Option

Port	144 LQFP	112 LQFP	64 LQFP
Port AD/ADC Channels	16/16	16/16	8/8
Port A pins	8	8	0
Port B pins	8	2	0
Port C pins	8	0	0
Port D pins	8	6	0
Port E pins inc. IRQ/XIRQ input only	8	8	4
Port H/FlexRay Channels	8/A+B	8/A+B	4/A
Port J/PMF Current Sense	8/3	8/3	4/0
Port K pins	8	0	0
Port M/CAN/PMF Fault Inputs/SPI	8/1/2/1	8/1/2/1	2/1/0/0
Port P/PMF channels/PMF Fault Inputs	8/6/2	8/6/2	6/6/0
Port S/SCI/SPI	8/2/1	8/2/1	6/1/1
Port T/Timer Channels	8/8	8/8	8/8
VDDX/VSSX	4/4	3/3	2/2

Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
1	1	1	PP1	PMF1		
2	2	2	PP0	PMF0		
3	3		PD3	DATA3		
4	4		PD2	DATA2		
5	5		PD1	DATA1		
6	6		PD0	DATA0		
7	7	3	PT0	IOC0		

Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
8	8	4	PT1	IOC1		
9	9	5	PT2	IOC2		
10	10	6	PT3	IOC3	STB0[2]	
11	11		PJ0	$\overline{IS0}$		
12	12		PJ1	$\overline{IS1}$		
13	13		PJ2	$\overline{IS2}$		
14	14	7	VDDF			
15	15	8	VSS1			
16	16		VSSX3			
17	17		VDDX3			
18	18	9	PT4	IOC4	STB1	
19	19	10	PT5	IOC5	STB2	
20	20	11	PT6	IOC6	STB3	
21	21	12	PT7	IOC7		
22			PC0	DATA8		
23			PC1	DATA9		
24			PC2	DATA10		
25			PC3	DATA11		
26			PC4	DATA12		
27			PC5	DATA13		
28			PC6	DATA14		
29			PC7	DATA15		
30	22	13	PJ3	STB0		
31	23	14	PJ4	STB1		
32	24	15	PJ5	STB2		
33	25	16	PJ6	STB3		
34	26		PJ7			
35	27		PB0	ADDR0	$\overline{UDS}$	
36	28		PB1	ADDR1		

Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
37			PB2	ADDR2		
38			PB3	ADDR3		
39	29	17	BKGD	MODC		
40	30	18	PE7	$\overline{\text{XCLKS}}$	ECLKX2	
41	31		PE6	MODB	$\overline{\text{TAGHI}}$	
42	32		PE5	MODA	$\overline{\text{TAGLO}}$	$\overline{\text{RE}}$
43	33	19	PE4	ECLK		
44	34		PE3	$\overline{\text{LSTRB}}$	$\overline{\text{LDS}}$	EROMCTL
45	35		PE2	R$\overline{\text{W}}$	$\overline{\text{WE}}$	
46	36		PH4	RXD_B		
47	37		PH5	TXD_B		
48	38		PH6	$\overline{\text{TXE\_B}}$		
49	39		PH7			
50	40	20	VDDX2			
51	41	21	VSSX2			
52	42	22	VSS3			
53	43	23	VDDR			
54	44	24	$\overline{\text{RESET}}$			
55	45	25	VDDPLL			
56	46	26	NC	No internal connection. Don’t connect!		
57	47	27	VSSPLL			
58	48	28	EXTAL			
59	49	29	XTAL			
60	50	30	TEST			
61			PB4	ADDR4		
62			PB5	ADDR5		
63			PB6	ADDR6		
64			PB7	ADDR7		
65	51		PA0	ADDR8		

Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
66	52		PA1	ADDR9		
67	53		PA2	ADDR10		
68	54		PA3	ADDR11		
69			VDDX4			
70			VSSX4			
71	55	31	PE1	$\overline{\text{IRQ}}$		
72	56	32	PE0	$\overline{\text{XIRQ}}$		
73	57	33	PH0	RXD_A		
74	58	34	PH1	TXD_A		
75	59	35	PH2	$\overline{\text{TXE\_A}}$		
76	60	36	PH3			
77			PK0	ADDR16	IQSTAT0	
78			PK1	ADDR17	IQSTAT1	
79			PK2	ADDR18	IQSTAT2	
80			PK3	ADDR19	IQSTAT3	
81			PK4	ADDR20	ACC0	
82			PK5	ADDR21	ACC1	
83			PK6	ADDR22	ACC2	
84			PK7	$\overline{\text{EWAIT}}$	ROMCTL	
85	61		PA4	ADDR12		
86	62		PA5	ADDR13		
87	63		PA6	ADDR14		
88	64		PA7	ADDR15		
89	65	37	VDD			
90	66	38	VSS2			
91	67	39	PAD00	AN0		
92	68		PAD08	AN8		
93	69	40	PAD01	AN1		
94	70		PAD09	AN9		

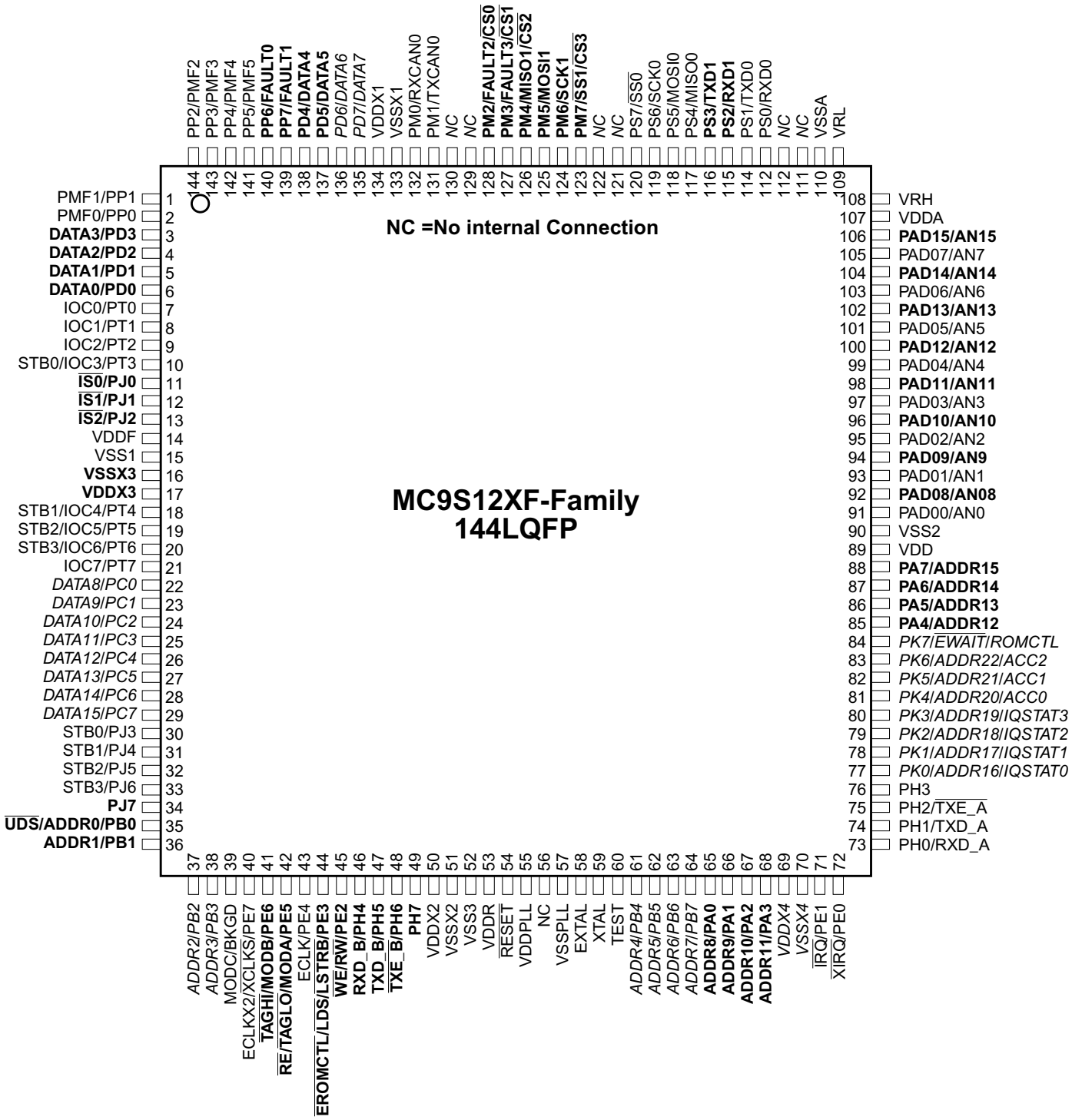
Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
95	71	41	PAD02	AN2		
96	72		PAD10	AN8		
97	73	42	PAD03	AN3		
98	74		PAD11	AN11		
99	75	43	PAD04	AN4		
100	76		PAD12	AN12		
101	77	44	PAD05	AN5		
102	78		PAD13	AN13		
103	79	45	PAD06	AN6		
104	80		PAD14	AN14		
105	81	46	PAD07	AN7		
106	82		PAD15	AN15		
107	83	47	VDDA			
108	84	48	VRH			
109	85	49	VRL			
110	86	50	VSSA			
111			NC			
112			NC			
113	87	51	PS0	RXD0		
114	88	52	PS1	TXD0		
115	89		PS2	RXD1		
116	90		PS3	TXD1		
117	91	53	PS4	MISO0		
118	92	54	PS5	MOSI0		
119	93	55	PS6	SCK0		
120	94	56	PS7	$\overline{SS0}$		
121			NC			
122			NC			
123	95		PM7	$\overline{SS1}$	$\overline{CS3}$	

Table 4 Pin-Out Summary

LQFP-144[1]	LQFP-112	LQFP-64	Pin	2nd Func.	3rd Func.	4th Func.
124	96		PM6	SCK1		
125	97		PM5	MOSI1		
126	98		PM4	MISO1	$\overline{CS2}$	
127	99		PM3	FAULT3	$\overline{CS1}$	
128	100		PM2	FAULT2	$\overline{CS0}$	
129			NC			
130			NC			
131	101	57	PM1	TXCAN0		
132	102	58	PM0	RXCAN0		
133	103	59	VSSX1			
134	104	60	VDDX1			
135			PD7	DATA7		
136			PD6	DATA6		
137	105		PD5	DATA5		
138	106		PD4	DATA4		
139	107		PP7	FAULT1		
140	108		PP6	FAULT0		
141	109	61	PP5	PMF5		
142	110	62	PP4	PMF4		
143	111	63	PP3	PMF3		
144	112	64	PP2	PMF2		

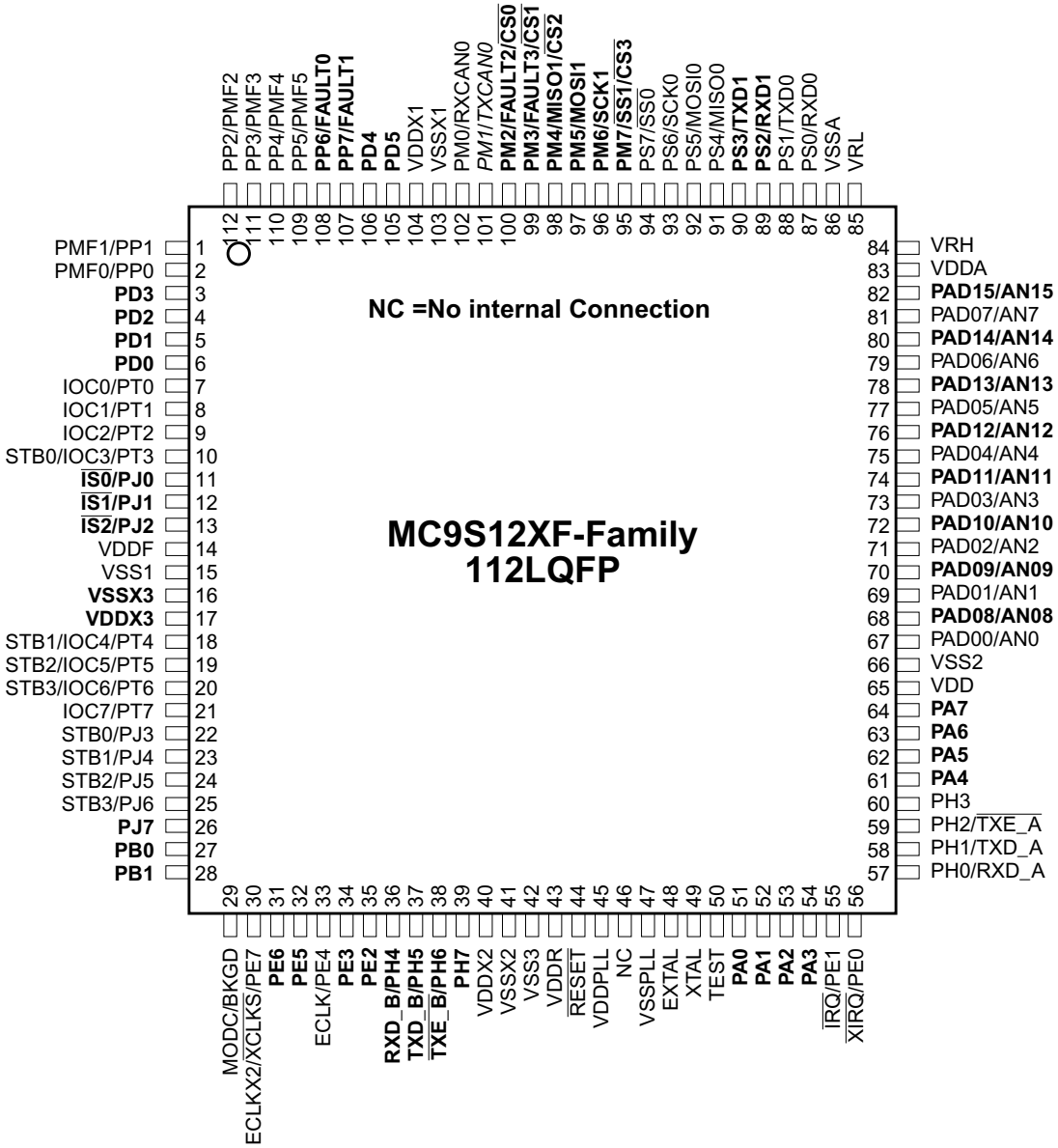
NOTES:
1. The 144-Pin LQFP version will not be qualified for production and is intended to be used for emulation (development tools) only.
2. STB3-0 on PT3-6 are equivalent to STB3-0 on PJ3-6



Pins shown in BOLD are not available on the 64-pin package option

Pins shown in *ITALICS* are not available on the 112-pin and 64-pin package options

Figure 1. MC9S12XF-Family Pin Assignments 144-pin LQFP Package



Pins shown in BOLD are not available on the 64-pin package option

Figure 2. MC9S12XF-Family Pin Assignments 112-pin LQFP Package

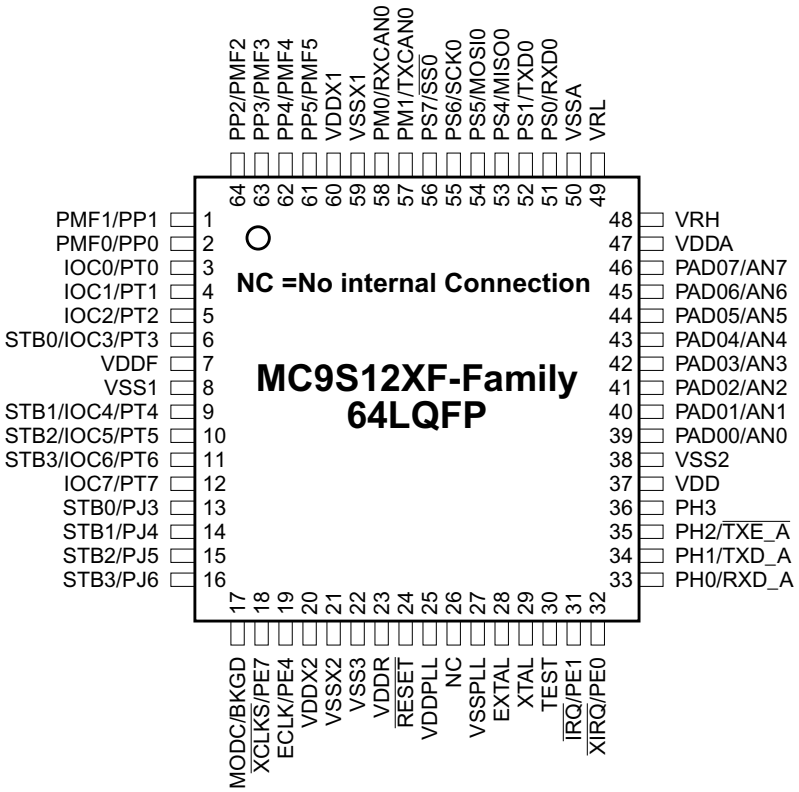


Figure 3. MC9S12XF-Family Pin Assignments 64-pin LQFP Package

NOTE

Pin 56 on the 114-pin LQFP, Pin 46 on the 112-pin LQFP and pin 26 on the 64-pin LQFP don't have to be connected.

Memory Maps

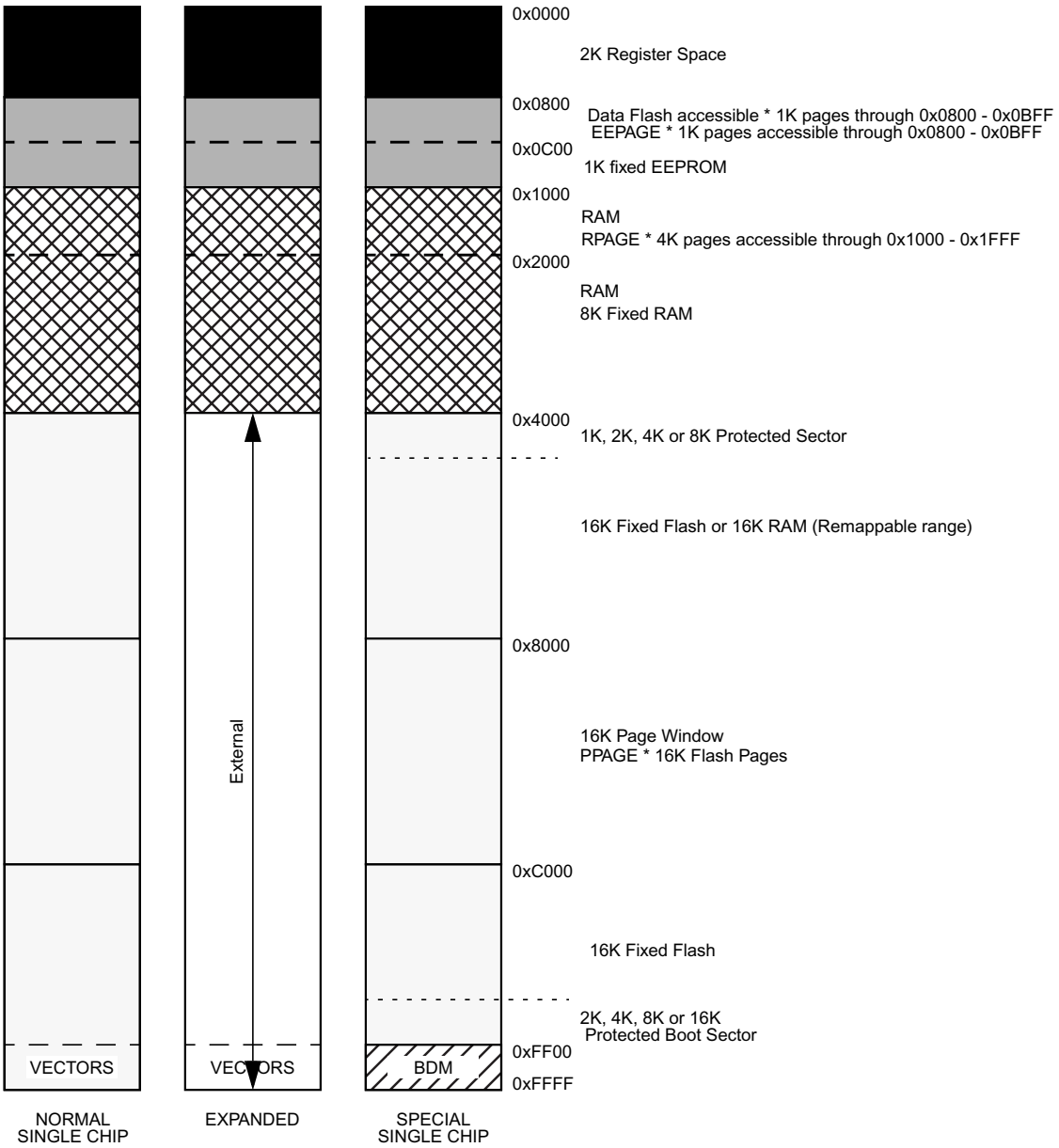


Figure 4. MC9S12XF-Family Memory Map

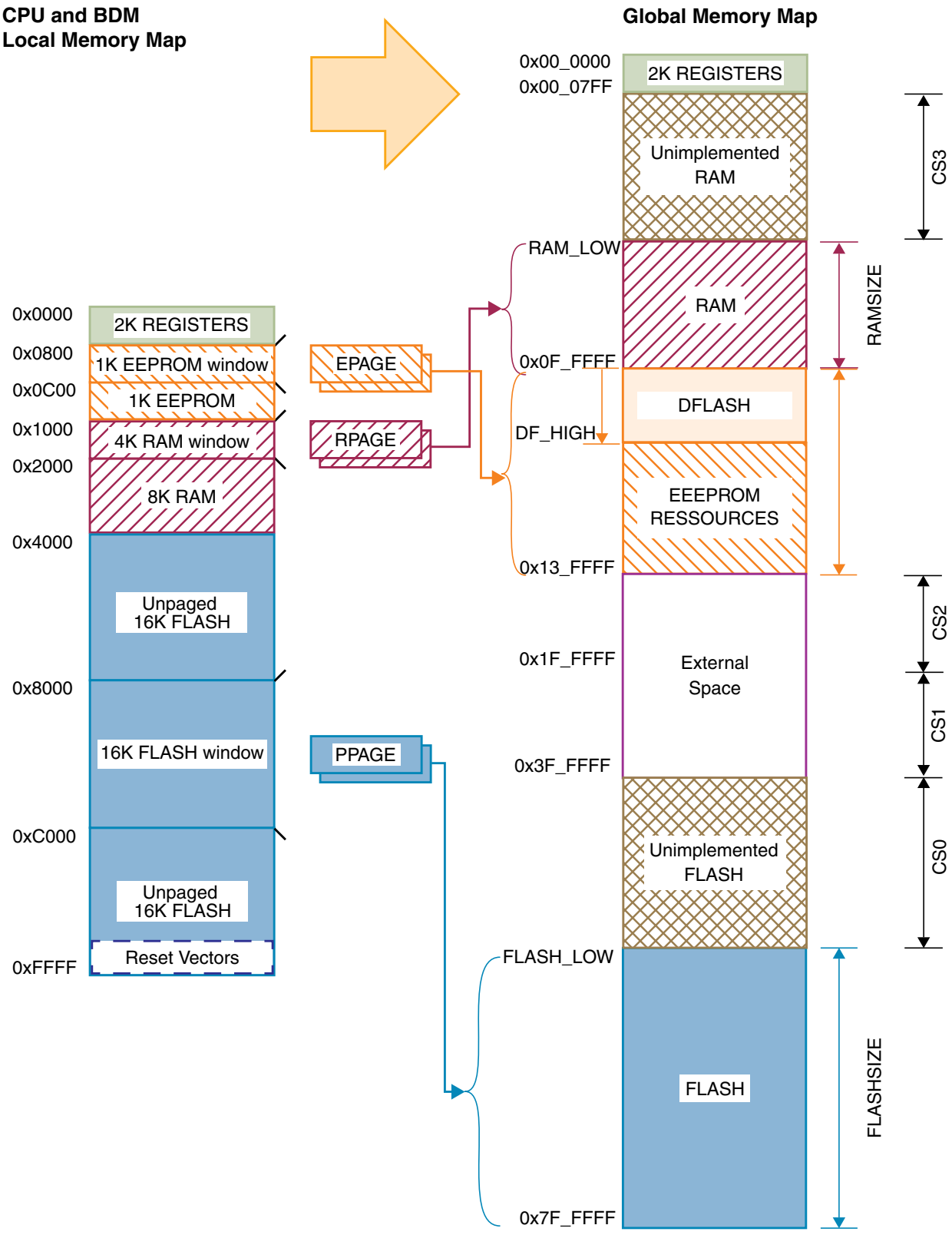


Figure 5 MC9S12XF512 Global Memory Map

Table 5 9S12XF512 Dependent Memory Parameters

Device	FLASH_LOW	PPAGE(1)	RAM_LOW	RPAGE(2)	DF_HIGH	EPAGE
9S12XF512	0x78_0000	32	0x0F_8000	8	0x10_7FFF	32

NOTES:
1. Number of 16K pages addressable via PPAGE register
2. Number of 4K pages addressing the RAM. RAM can also be mapped to 0x4000 - 0x7FFF

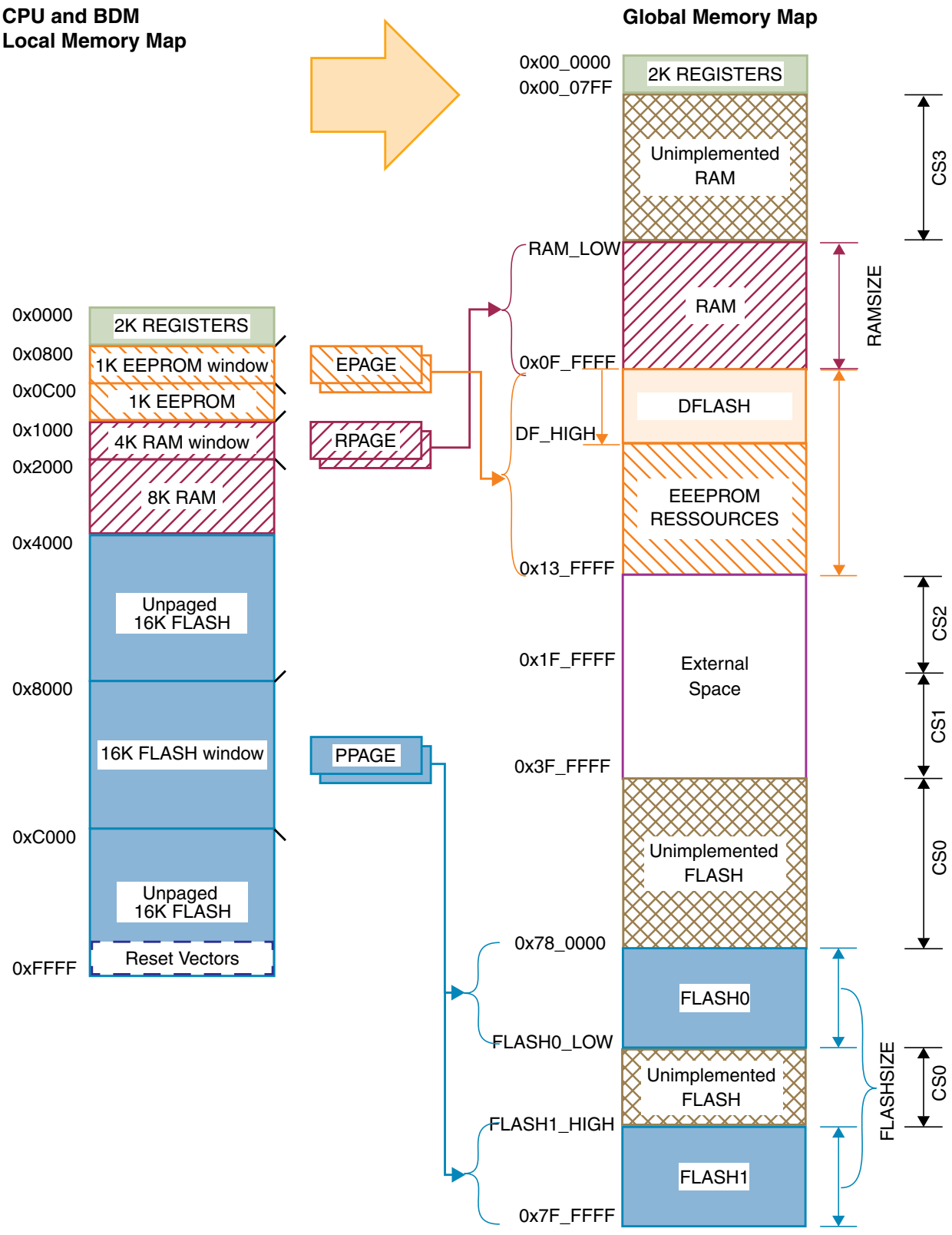


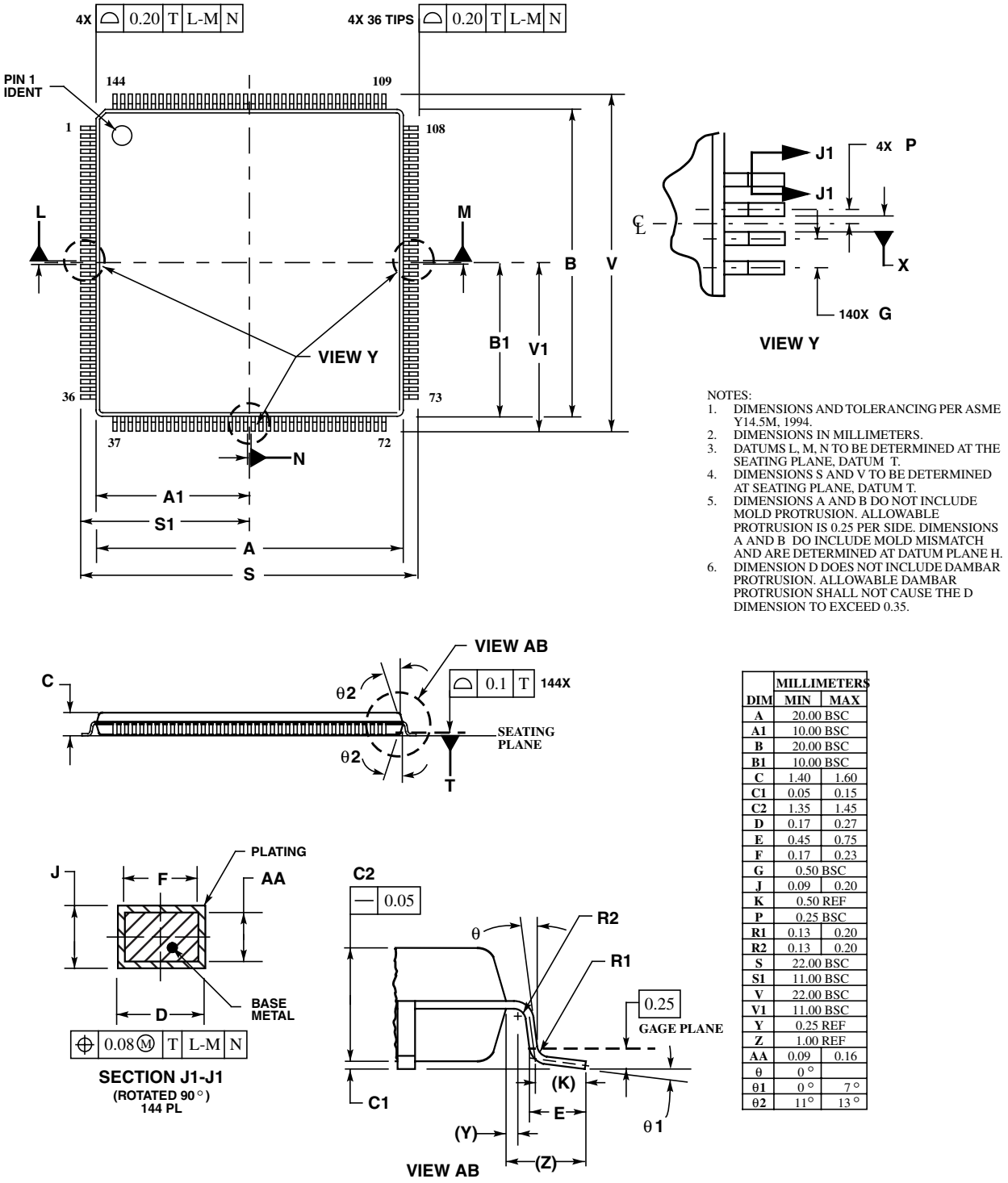
Figure 6 MC9S12XF384 , MC9S12XF256 and MC9S12XF128 Global Memory Map

Table 6 Derivative Dependent Memory Parameters

Device	FLASH0_LOW	FLASH1_HIGH	PPAGE(1)	RAM_LOW	RPAGE(2)	DF_HIGH	EPAGE
9S12XF384	0x79_FFFF	0x7C_0000	24	0x0F_A000	6	0x10_7FFF	32
9S12XF256	0x79_FFFF	0x7E_0000	16	0x0F_6000	5	0x10_7FFF	32
9S12XF128	0x78_FFFF	0x7F_0000	8	0x0F_C000	4	0x10_3FFF	16

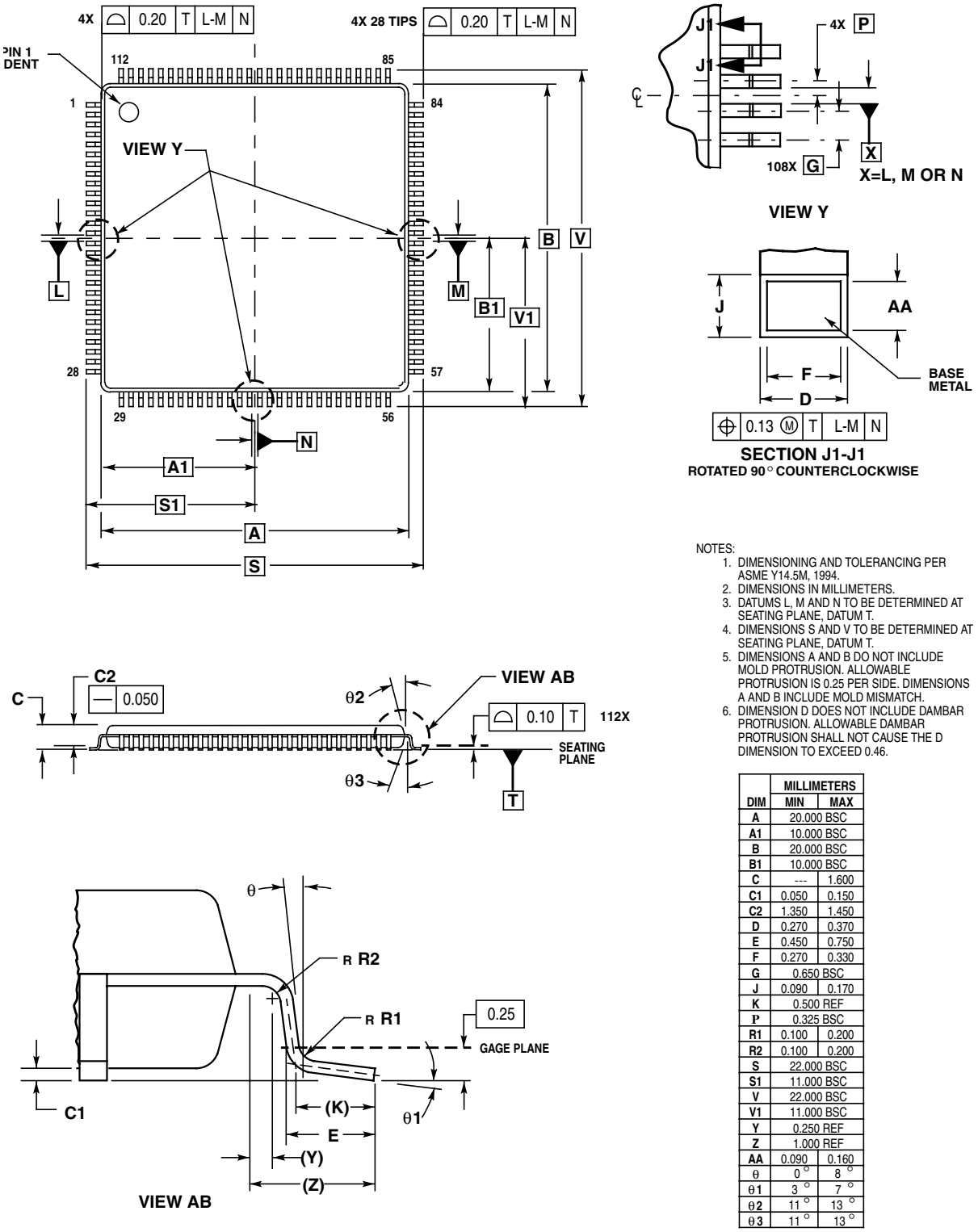
NOTES:
1. Number of 16K pages addressable via PPAGE register
2. Number of 4K pages addressing the RAM. RAM can also be mapped to 0x4000 - 0x7FFF

Mechanical Package Dimensions



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0 °	
θ1	0 °	7 °
θ2	11°	13 °

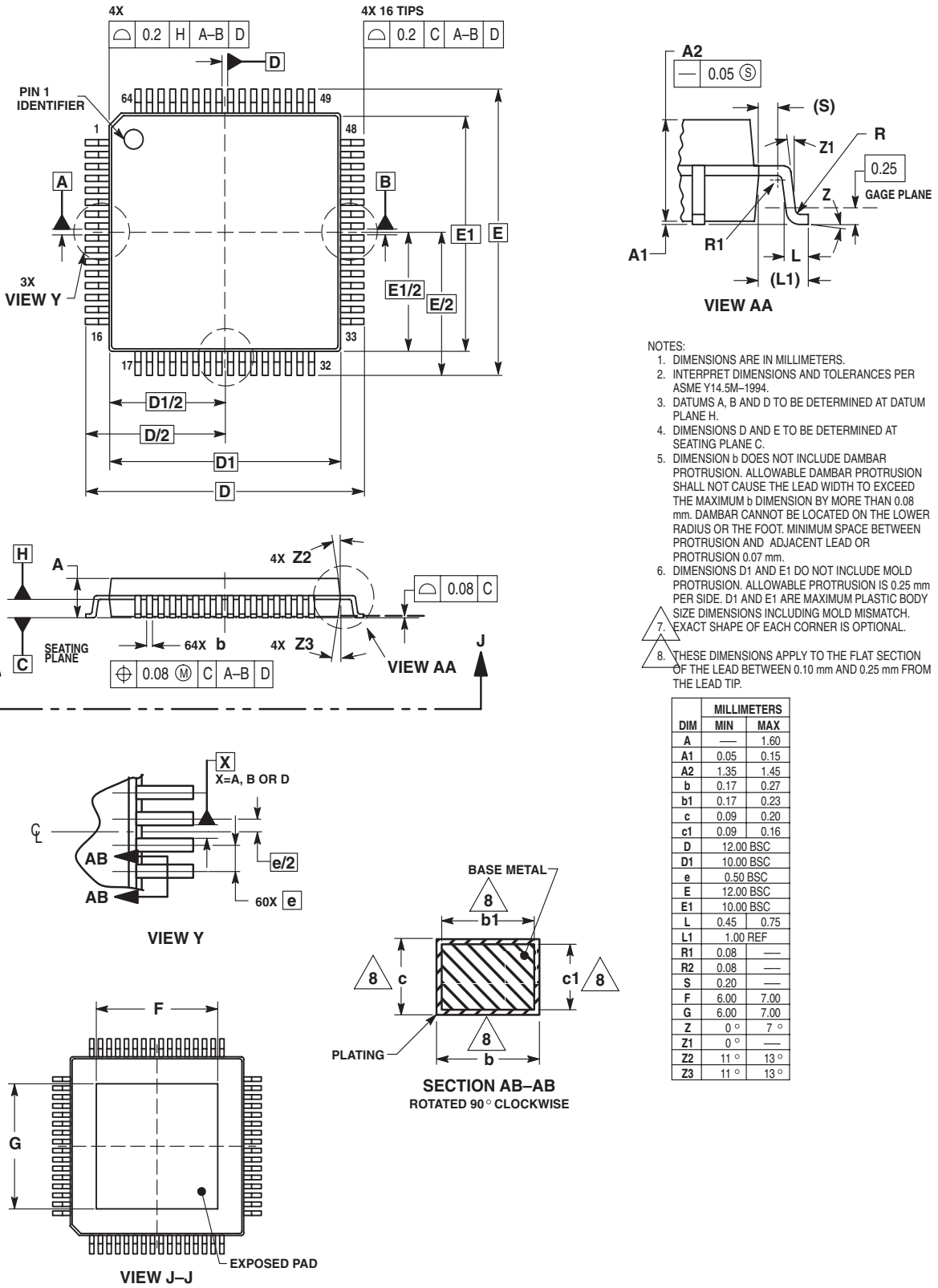
Figure 7 144-pin LQFP Mechanical Dimensions (case no. 918-03)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 8 112-pin LQFP Mechanical Dimensions (case no. 987)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	—
R2	0.08	—
S	0.20	—
F	6.00	7.00
G	6.00	7.00
Z	0°	7°
Z1	0°	—
Z2	11°	13°
Z3	11°	13°

Figure 9 64-pin exposed LQFP Mechanical Dimensions (case no. 840K-01)

Revision History

Table 7 Revision History

Revision Number	Revision Date	Author	Description
1	06-Dec-2006		Updated global memory map for all XF family derivatives.

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