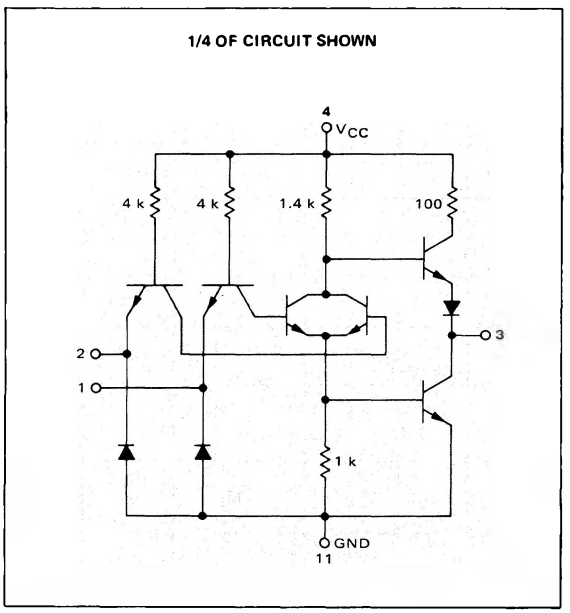
QUAD 2-INPUT "NOR" GATE

# MCBC5400/MCB5400F series

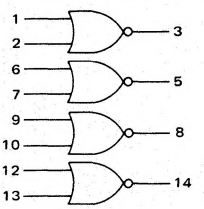
## MCBC5402*
## MCB5402F*

BEAM LEAD




Pin numbers on drawings are for devices in the flat package.

This device consists of four 2-input NOR gates that is produced using beam lead sealed junction technology. These devices are particularly useful in highly reliable systems using hybrid beam lead assembly techniques or standard flat package assembly techniques.




Positive Logic: $3 = \overline{1 + 2}$

Negative Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1

Output Loading Factor = 10

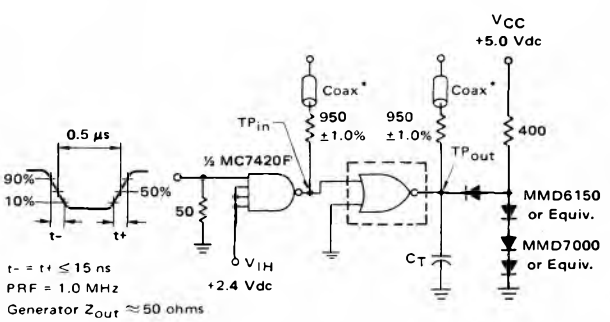
Total Power Dissipation = 48 mW typ/pkg

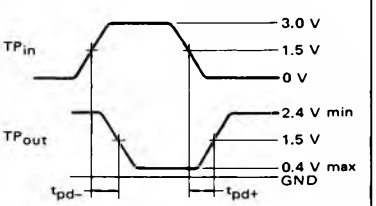
Propagation Delay Time = 10 ns typ

| Package No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Beam No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

### VOLTAGE WAVEFORMS AND DEFINITIONS

### SWITCHING TIME TEST CIRCUIT



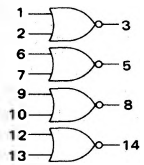

$C_T$ = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*F suffix = 1/4" x 1/4" ceramic package (Case 651) MCBC-prefixed devices are unencapsulated. See General Information section for package and chip details.

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs. Pin numbers used are for devices in the flat package.




| Characteristic | Symbol | Pin Under Test | Test Limits MCBC5402/MCBC5402F −55 to +125°C Min | Max | Unit | TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA $I_{OL}$ | $I_{OH}$ | Volts $V_{IL}$ | $V_{IH}$ | $V_{IHH}$ | $V_{R1}$ | $V_{R2}$ | $V_{th1}$ | $V_{th0}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 16 | 0.4 | 0.4 | 2.4 | 5.5 | 4.5 | 5.0 | 2.0 | 0.8 | 5.0 | 4.5 | 5.5 | |
| | | | | | | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: | | | | | | | | | | | | |
| **Input** | | | | | | | | | | | | | | | | | | |
| Forward Current | $I_F$ | 1 | - | -1.6 | mAdc | - | - | 1 | - | - | 2 | - | - | - | - | - | 4 | 11* |
| Leakage Current | $I_{R1}$ | 1 | - | 40 | μAdc | - | - | - | 1 | - | - | - | - | - | - | - | 4 | 2,11* |
| | $I_{R2}$ | 1 | - | 1.0 | mAdc | - | - | - | - | 1 | - | - | - | - | - | - | 4 | 2,11* |
| **Output** | | | | | | | | | | | | | | | | | | |
| Output Voltage | $V_{OL}$ | 3 | - | 0.4 | Vdc | 3 | - | - | - | - | - | - | 1 | - | - | 4 | - | 2,11* |
| | $V_{OH}$ | 3 | 2.4 | - | Vdc | - | 3 | - | - | - | - | - | - | 2 | - | 4 | - | 1,11* |
| Short-Circuit Current | $I_{SC}$ | 3 | -20 | -55 | mAdc | - | - | - | - | - | - | - | - | - | - | - | 4 | 1,2,3,11* |
| **Power Requirements (Total Device)** | | | | | | | | | | | | | | | | | | |
| Power Supply Drain | $I_{PDH}$ | 4 | - | 27 | mAdc | - | - | - | - | - | - | 1,2,6,7,9, 10,12,13 | - | - | - | - | 4 | 11 |
| | $I_{PDL}$ | 4 | - | 16 | mAdc | - | - | - | - | - | - | - | - | - | - | - | 4 | 1,2,11* |
| **Switching Parameters** | | | | | | Pulse In | Pulse Out | | | | | | | | | | | |
| Turn-On Delay | $t_{pd-}$ | 1,3 | - | 15** | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | - | 2,11* |
| Turn-Off Delay | $t_{pd+}$ | 1,3 | - | 22** | ns | 1 | 3 | - | - | - | - | - | - | - | 4 | - | - | 2,11* |

*Ground inputs to gates not under test.
**Tested only at 25°C.