Freescale Semiconductor, Inc.

MOTOROLA

Communications and Advanced
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MCF5102

Product Brief

MCF5102 ColdFire™ Integrated Microprocessor

ColdFire™ represents a revolutionary new microprocessor architecture that has been optimized for embedded processing applications. It brings new levels of price and performance to cost-sensitive high-volume markets. Based on the concept of Variable-Length RISC technology, ColdFire combines the architectural simplicity of conventional 32-bit Fixed-Length RISC with a memory-saving variable-length instruction set. By employing a variable-length instruction set architecture, ColdFire RISC processors are tuned to offer embedded processor designers significant system-level advantages over conventional fixed length RISC architectures. Binary code for ColdFire processors is denser and therefore takes up less program memory than conventional 32-bit fixed-length machines. This improved code density results in systems that require less memory for a given application and also allows the use of slower and less costly memory to achieve a given performance level.

The MCF5102 is fully ColdFire code-compatible. As the first chip in the Coldfire Family, it has been designed with special capabilities that allow it to also execute the M68000 code that exists today. These extensions to the ColdFire instruction set allow Motorola customers to use the MCF5102 as a bridge to future ColdFire processors for applications requiring the advantages of a variable-length RISC architecture.Compatibility with existing development tools such as compilers, debuggers, real-time operating systems and adapted hardware tools offers MCF5102 developers access to a broad range of mature tool support; enabling an accelerated product development cycle, lower development costs and critical time-to-market advantages.

The primary features of the MCF5102 are as follows:

- High Integer Performance
  - 1 instruction per clock peak performance
- Full Static Design Allows Operation Down To DC To Minimize Power Consumption
- On-Chip Caches
  - 2 Kbytes instruction cache
  - 1 Kbytes data cache
- 4 Separate Access Control Registers
- Simple Instruction Set Architecture
  - 16 user-visible 32-bit-wide registers
  - User-mode compatible with M68K instruction set
  - Supervisor/User modes for system protection
  - Vector base register to relocate exception vector table
  - Optimized for high-level language constructs

- Low Interrupt Latency
- Multiplexed 32-Bit Address and 32-Bit Data Bus To Minimize Board Space And Interconnections
- 3.3-Volt Operation
- 5-Volt TTL Compatible, 5-Volt CMOS Tolerant
- Three-State Pin
- Snoop
- JTAG IEEE 1149.1
- Single Bus Clock Input
- Fast Locking PLL

OVERVIEW

The following paragraphs provide an overview of the MCF5102. Figure 1 shows a block diagram of the MCF5102.

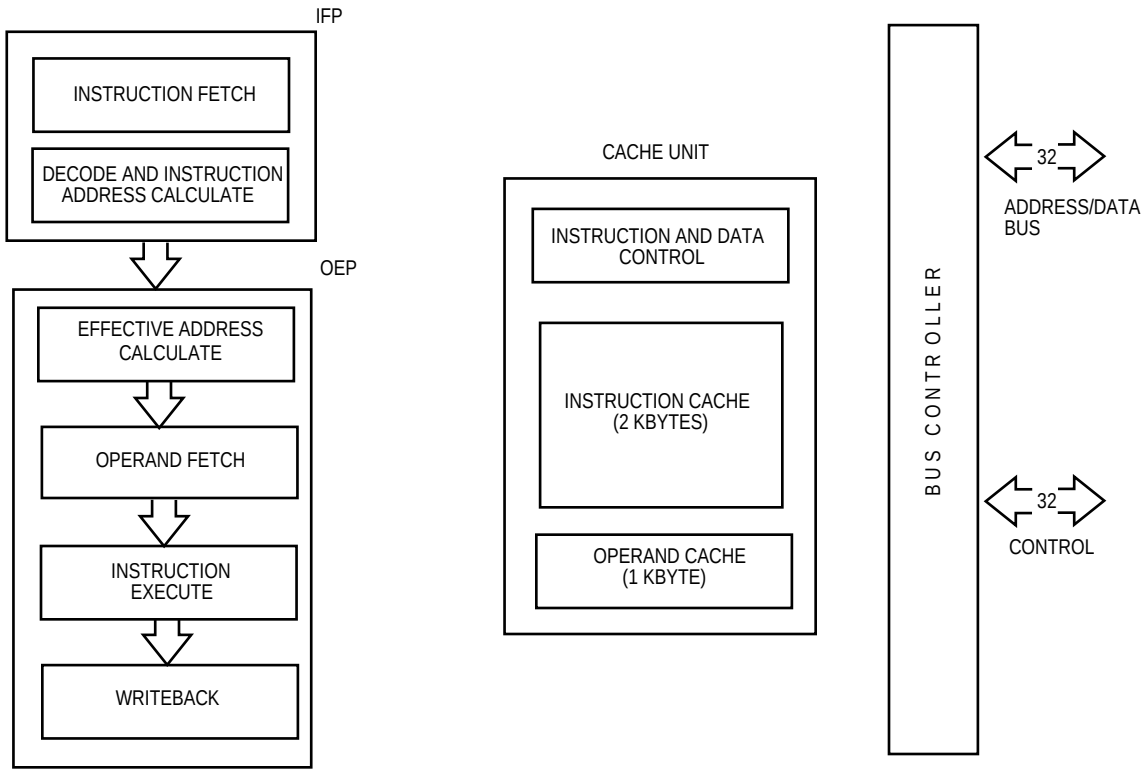

Figure 1. MCF5102 Block Diagram

The ColdFire's processor consisted of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The Instruction Fetch Pipeline (IFP) is a 2-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the 2-stage Operand Execution Pipeline (OEP), which decodes the instruction, fetches the required operands and then executes the required function. Since the IFP and OEP pipelines are decoupled by an instruction buffer which serves as a FIFO queue, the IFP is able to prefetch instructions in advance of their actual use by the OEP thereby

minimizing time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit.

INSTRUCTION FETCH PIPELINE

- Instruction Fetch—Fetching an instruction from memory.
- Decode and Instruction Address Calculate—Converting an instruction into micro-instructions.

OPERAND EXECUTION PIPELINE

- Effective Address <ea> Calculate—If the instruction calls for data from memory, the location of the data is calculated.
- Operand Fetch—Data is fetched from memory.
- Instruction Execute—The data is manipulated during execution.
- Write-Back—The result of the computation is written back to on-chip caches or external memory.

The write-back stage holds the operand until the opportune moment when no data fetches are required. The write-back can defer writes indefinitely until either the data control unit is free or another write is pending from the execution stage. Holding the data in the write-back stage maximizes system performance by not interrupting the incoming instruction or data stream.

ACCESS CONTROL REGISTER

Four access control registers provide protection and caching mode information for four areas of memory space. Two of these ACRs are associated with the data accesses and two with instruction accesses.

INSTRUCTION AND DATA CACHES

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and external accesses to occur simultaneously with instruction execution. For example, if the processor requires both an instruction access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip.

Each cache is accessed by physical addresses. The data cache can be configured as write-through or deferred copyback as defined in the ACRs. This allows for optimizing the system design for high performance with the deferred copyback writes to system memory.

Cache capability of memory is controlled by two bits in the ACRs. Cacheable memory can be either write-through or copyback, with no write-allocate for misses to write-through memory.

CACHE ORGANIZATION. The instruction and data caches are each organized as four-way set-associative, with 16-byte lines. Each line consists of an address tag and state information that shows the line's validity. In the data cache, the state information indicates whether the line is invalid, valid, or dirty.

CACHE COHERENCY. The MCF5102 can snoop the external bus during accesses by other bus masters to maintain coherency between the caches and external memory systems. External cycles can be flagged

on the bus as snoopable or nonsnoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches for a coherency conflict based on the state of the corresponding cache line and the type of external cycle. External write cycles are snooped by both the instruction cache and data cache; whereas, external read cycles are snooped only by the data cache.

Although the internal execution units and the bus snooper circuit all have access to the on-chip caches, the snooper has priority over the execution units to allow the snooper to resolve coherency discrepancies immediately.

BUS CONTROLLER

The bus controller supports a high-speed, multiplexed, synchronous, external bus interface. The bus controller also provides a burst mode for fast data transfer for both reads and writes. The processor uses burst mode to update a single cache line (four long words), minimizing the time it takes to update the cache. Burst write cycles are also performed by the bus controller to transfer four long words to system memory in five clock cycles, maximizing memory write performance. The bus controller operates concurrently with all of the other functional units of the device to maintain maximum system throughput.

POWER CONSUMPTION MANAGEMENT

The MCF5102 is very power efficient due to the use of a 3.3-V power supply and static logic design. The resulting power consumption is less then 1.0 W in full operation @ 25 MHz.The 3.3-V power supply reduces current consumption by 40–60% over microprocessors that use a 5-V power supply.

In addition to operating the device at slower frequencies to reduce power consumption, this processor can dynamically control power with the low-power stop (LPSTOP) instruction. This instruction shuts down active circuits in the processor and halts instruction execution. Current consumption in this standby mode is reduced to about 200 μA. Processing can be resumed by resetting the part or by generating a valid interrupt.

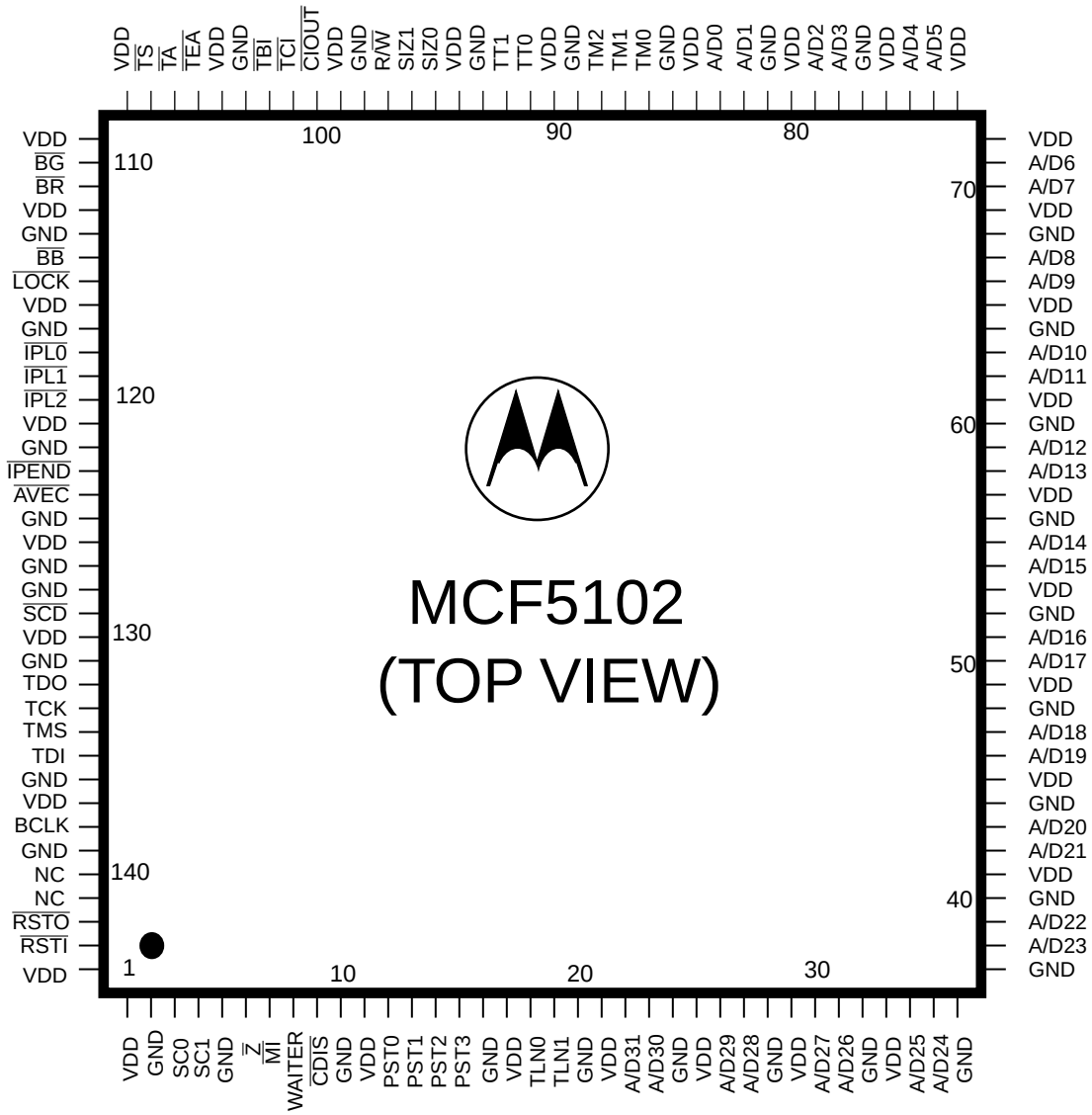

Figure 2. MCF5102 Pin Out

MORE INFORMATION

The following table identifies the packages and operating frequencies available for the MCF5102.

MCF5102 Package/Frequency Availability

	FREQUENCY		
PACKAGE	**16.67MHZ**	**20MHZ**	**25MHZ**
Thin Plastic Quad Flat Pack 144 lead	Available	Available	Available

The documents listed in the following table contain detailed information that pertain to the MCF5102. These documents may be obtained from the Literature Distribution Centers at the addresses listed on the last page of this document.

Documentation

DOCUMENT NUMBER	DOCUMENT TITLE	AVAILABILITY
MCF5102UM/AD	MCF5102 User's Manual	now
M68000PM/AD	M68000 Family Programmer's Reference Manual	now
MCF5200PRM/AD	ColdFire Programmer's Reference Manual	now

Development Tools

All compiler/debugger companies that support the MC68EC040 also support the MCF5102.

COMPANY	COMPANY PHONE NUMBER
RTOS	
ISI	408-542-1500
Microware	515-224-1929
Embedded System Products	713-561-9990
EMULATORS	
Applied Microsystems	206-882-2000

Development Boards

ORDER NUMBER	DESCRIPTION	AVAILABILITY
M68EC040IDP3	M68EC040 Evaluation/Development System	now
M5102EVM	MCF5102 Mezzanine card	now

Note: Both the M68EC040 CPU (or M68EC040 IDP) and the M5102 EVM are required for development.

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.