MCF52235 Reference Manual Addendum

Supported Devices:MCF52230,MCF52231,MCF52232, MCF52233,MCF52234,MCF52235,MCF52236

by:Microcontroller Solutions Group

This addendum document describes corrections to the MCF52235 *Reference Manual*, order number MCF52235RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates

The current available version of the MCF52235 *Reference Manual* is Rev 7.

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1 Addendum for Revision 7

Table 1. MCF52235 Reference Manual Rev. 7 Addendum

Location	Description
Chapter "Clock Module"/Section "Block Diagram"/Figure " Clock Module Block Diagram"	Updated the Figure "Clock Module Block Diagram" by • indicating that an alternate clock source, "PLL bypass clock", is available to the FlexCAN module and • adding a clock mux component controlled by the CANCTRL[CLK_SRC] bit that indicates what clock (system clock/2 or FlexCAN oscillator clock) feeds the FlexCAN module.

Table 1. MCF52235 Reference Manual Rev. 7 Addendum (continued)

Location	Description
Chapter "FlexCAN" Section "FlexCAN Control Register (CANCTRL)" /Table "CANCTRL Field Descriptions"	Change From: $$\text{S clock frequency} \ = \ \frac{f_{sys} \text{ or EXTAL}}{\text{PRESDIV} + 1}$$ Change To: $$\text{S clock frequency} \ = \ \frac{f_{sys/2} \text{ or PLL bypass clock}}{\text{PRESDIV} + 1}$$
Chapter "FlexCAN" Section "FlexCAN Control Register (CANCTRL)" /Table "CANCTRL Field Descriptions"	In the Description of field 13 CLK_SRC bit Change from: 0 Clock source is EXTAL 1 Clock source is the internal bus clock, fsys Change to : 0 Clock source is FlexCAN oscillator clock 1 Clock source is the internal bus clock, fsys/2
Chapter "FlexCAN" /Section "Protocol Timing"/Figure "CAN Engine Clocking Scheme"	In Figure " Change From : $$f_{Tq} \ = \ \frac{f_{sys} \text{ or EXTAL}}{(\text{PRESDIV} + 1)}$$ Change To: $$f_{Tq} \ = \ \frac{f_{sys/2} \text{ or PLLbypass clock}}{\text{PRESDIV} + 1}$$

2 Addendum for Revision 5

Table 2. MCF52235RM Rev. 4 to Rev. 5 Changes

Location	Description
Throughout	• Formatting, layout, spelling, and grammar corrections. • Removed the "Preliminary" designation from the title page and the page footers.
Chapter 1	Added information about the MCF52232 and MCF52236 devices.
Table 2-1 / Page 2-3	Synchronized the "Pin Functions by Primary and Alternate Purpose" table in the device reference manual and data sheet.
Figure 6-3 / Page 6-4	Updated the figure to show the OD bit (bit 31).
Section 7.6.2 / Page 7-5	Deleted the sentence "If CLKMOD0 is driven low during reset, XTAL is sampled to determine clocking mode."
Table 7-4 / Page 7-7	Modified the SYNCR[RFD] description to explain that changing RFD may cause a glitch in the PLL clock.

Table 2. MCF52235RM Rev. 4 to Rev. 5 Changes (continued)

Location	Description
Section 7.8.3 / Page 7-12	Deleted the sentence "The RFD is not in the feedback loop of the PLL, so changing the RFD divisor does not affect PLL operation".
Table 12-5 / Page 12-5	• Added missing information to the RCON[RLOAD] and RCON[MODE] field descriptions. • Deleted the sentence "The default mode can be overridden during reset configuration" from the RCON[MODE] field description.
Table 13-1 / Page 13-2	Corrected PACRn addresses.
Section 13.5.4 / Page 13-8	Updated the section to reflect the fact that the CWT does not cause a hardware reset.
Table 13-12 / Page 13-18	Added an entry for PACR5 and a footnote to clarify the meaning of "—".
Section 15-1 / Page 15-2	Deleted the sentence beginning with "For many peripheral devices...".
Table 15-3 / Page 15-6	Deleted the entry for the (nonexistent) GSWIACK register.
Table 15-13 / Page 15-13	Added the missing EPHY interrupt source (36).
Section 15.3.8 / Page 15-19	Deleted references to the (nonexistent) GSWIACK register.
Chapter 17	Added the section "EzPort Lockout Recovery".
Figure 17-3 / Page 17-5	Updated the FLASHBAR figure to show that WP is read-only with a reset value of 1.
Section 18.4.6 / Page 18-7	Added a subsection, "Duplicate Frame Transmission".
Table 18-9 / Page 18-17	Corrected the ending address of the MIB block counters In the top-level module memory map (was IPSBAR+0x13FF, is IPSBAR+0x12FF).
Section 20.4 / Page 20-12	Deleted the sentence "BCRn decrements when an address transfer write completes for a single-address access (DCRn[SAA] = 0), or when SAA equals 1."
Figure 26-6 / Page 26-9	Added a note to clarify the UCSRn reset values.
Figure 26-22 / Page 26-21	• Corrected the label of the top signal (was UnTXD, is UnRXD). • Corrected the text in the footnote (was TXRTS, is RXRTS).
Figure 26-23 / Page 23-24	Corrected the UnTXD label (was "Input", is "Output").
Figure 26-25 / Page 26-24	• Corrected a label on the bottom row (was UMR1n[PT]=2, is UMR1n[PT]=1). • Deleted duplicate UMR1n[PM]=11 label.
Section 26.4.6 / Page 26-26	• Reordered and renumbered the subsections. • Added example DMA configuration steps.
Table 28-19 / Page 28-20	Changed the description for SEL_VREFH=0 and SEL_VREFL=0 (were "Internal VRx", are "VRH" and "VRL", respectively).
Section 29.3.2.5.1 / Page 29-18	Added missing numerical values to the output example.
Section 29.3.2.6.1 / Page 29-20	Added missing numerical values to the output example.
Section 30.5.1 / Page 30-29	Corrected the section to reflect the fact that there are 19 total FlexCAN interrupts (added 16 individual interrupts per MB).
Table 31-4 / Page 31-6	Changed the reset values for PBR1, PBR2, and PBR3 (was "0x0000_0000", is "See Section").
Section 31.5.1 / Page 31-19	Combined second and third sentences in bullet #2 (was "This type of halt is always first made pending in the processor. Next, the processor samples for pending halt and interrupt conditions once per instruction", is "This type of halt is always first marked as pending in the pecessor, which samples for pending halt and interrupt conditions once per instruction".)

Table 2. MCF52235RM Rev. 4 to Rev. 5 Changes (continued)

Location	Description
Appendix A	• Corrected PACR*n* addresses. • Deleted the entry for the (nonexistent) GSWIACK register.

3 Addendum for Revision 4

Table 3. MCF52235RM Rev. 3 to Rev. 4 Changes

Location	Description
Throughout	Formatting, layout, spelling, and grammar corrections.
Table 2-1 / Page 2-3	Changed the pin number for $\overline{\text{IRQ11}}$ on the 80 LQFP package (was "—", is 41).
Table 3-1 / Page 3-3	• For the PC, changed the reset value (was "Undefined", is "Contents of Location 0x0000_0004") and the "Written with MOVEC entry" value (was "Yes", is "No"). • Changed the reset value for the OTHER_A7 (was "Undefined", is "Contents of Location 0x0000_0000"). • Changed the reset value for the RAMBAR (was "0x0000_0000", is "See Section").
Section 3.2.4 / Page 3-5	Deleted section and moved its information into Section 3.2.
Figure 3-5 / Page 3-6	• Modified the figure to show that Bits 4:0 are read/write. • Changed the access (was "Access: User read-only", is "Access: User read/write").
Table 3-2 / Page 3-6	Removed the last sentence in the C bit field description.
Figure 3-8 / Page 3-7	Modified the figure to show that Bits 4:0 are read/write.
Section 3.4 / Page 3-9	Changed the last sentence in step 2 to "The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address".
Section 3.6.6 / Page 3-25	Added the following note after the table: The execution times for moving the contents of the Racc, Raccext[01,23], MACSR, or Rmask into a destination location <ea>x shown in this table represent the best-case scenario when the store instruction is executed and there are no load or M{S}AC instructions in the EMAC execution pipeline. In general, these store operations require only a single cycle for execution, but if preceded immediately by a load, MAC, or MSAC instruction, the depth of the EMAC pipeline is exposed and the execution time is four cycles.
Figure 4-4 / Page 4-5	Updated the figure to show that bits 11:0 are read-write.
Figure 4-5 / Page 4-10	Updated the MASK register figure to show that bits 31:16 are read-only and are always set.
Equation 4-3 / Page 4-13	Added a minus sign to the exponent so that it is "$-(i + 1 - N)$".
Section 7.7.1.4 / Page 7-10	Added the following note: **Note:** The CCHR can be written at any time. However, changes will take effect only after the PLL is disabled and re-enabled.
Table 11-1 / Page 11-2	Changed the RAMBAR reset value (was "0x0000_0000", is "See Section").
Section 11.2.1 / Page 11-2	• Corrected section to show the proper RAMBAR figure and field description table. • Changed the last bullet to "A reset clears the RAMBAR's priority, backdoor write-protect, and valid bits, and sets the backdoor enable bit. This enables the backdoor port and invalidates the processor port to the SRAM. (The RAMBAR must be initialized before the core can access the SRAM.) All other bits are unaffected.".
Section 18.5.4.6 / Page 18-27	Added the following text to the MMFR description: "Before accessing the MII registers via the MMFR, the software must poll EIR[MII] to make sure that an access is not currently in progress."

Table 3. MCF52235RM Rev. 3 to Rev. 4 Changes (continued)

Location	Description
Figure 19-3 / Page 19-5	Corrected the reset value for ANDIS, DIS100, and DIS10 (was 0, is 1).
Figure 19-4 / Page 19-7	Corrected the name of bit 4 (was PHYADD4, is PHYADD3).
Figure 19-5 / Page 19-7	Corrected the reset value for 100DIS and 10DIS (was 0, is 1).
Section 19.3.3.2 / Page 19-11	• Corrected the name of bit 11 (was PDWN, is 10THD). • Corrected the description of bit 11 (the proper description is found in Revision 2 of the reference manual).
Figure 19-8 / Page 19-13	Corrected the reset value for bit 11 (was 01, is 0).
Section 19.3.3.4 / Page 19-13	• Corrected the reset value for PHYID (was 0b000000, is 0b000110). • Corrected the PHYID field description (was "Composed of bits 15:10.", is "Composed of bits 19:24").
Table 19-10 / Page 19-14	Added a description of the SELECTORFIELD field.
Section 19.3.3.6 / Page 19-15	• Updated the register figure and field description table to show that bits 12:11 are reserved. • Added a description of the SELECTORFIELD field.
Section 19.3.3.7 / Page 19-16	Provided a concise name for bits 10:0 (was "Message/Unformatted Code Field [10:0]", is CODEFIELD).
Section 19.3.3.9 / Page 19-18	Provided a concise name for bits 10:0 (was "Message/Unformatted Code Field [10:0]", is CODEFIELD).
Figure 19-16 / Page 19-20	• Updated the figure to show that the register is read-only. • Added the following footnote to ANCMODE: "This bit is valid only when ANNC is set."
Figure 19-17 / Page 19-21	• Corrected the reset value for FEFLTD (was 1, is 0). • Corrected the reset value for bit 12 (was 1, is 0). • Corrected the reset value for bit 11 (was 0, is 1). • Corrected the reset value for JBDE (was 0, is 1). • Corrected the reset value for POLCORD [was "(1)", is 0].
Table 19-17 / Page 19-21	• Corrected the name of bit 13 (was MIILBO, is MIILBD). • Corrected the description of bit 12 (is "Reserved, should be cleared.") • Corrected the description of bit 11 (is "Reserved, should be set.")
Figure 25-1 / Page 25-1	Corrected signal name (was QSPI_CS[:0], is QSPI_CS[3:0]).
Section 26.2 / Page 26-3	Changed "An internal interrupt request signal notifies the interrupt controller..." to "A request signal is provided to notify the interrupt controller...".
Table 26-6 / Page 26-9	Changed "DTIN" to "DT*n*IN" (to maintain consistent signal names throughout chapter).
Section 26.4.5.2 / Page 26-26	Changed "...complete normally without exception processing..." to "...complete normally without an error termination...".
Section 27.6 / Page 27-12	Changed programming examples from assembly language to pseudocode.
Table 29-1 / Page 29-2	Deleted reference to nonexistent SCMISR register from footnote 2.
Table 31-10 / Page 31-16	• Added the following note to the PBR0[Address] field description: **Note:** PBR0[0] should always be loaded with a 0. • Changed the bit range in the Field column (was 31–1, is 31–0).
Figure 31-8 / Page 31-16	Changed the address of PBR3 (was 0x1C, is 0x1B).
Table 31-22 / Page 31-39	Changed the initial state of the CSR (was 0x0, is 0x0090_0000).

Table 3. MCF52235RM Rev. 3 to Rev. 4 Changes (continued)

Location	Description

Section 31.6.2 / Page 31-43	Added the following note at the end of this section:
	The debug module requires the use of the internal bus to perform BDM commands. For this processor core, if the processor is executing a tight loop that is contained within a single aligned longword, the processor may never grant the internal bus to the debug module, for example:
	
	        align4
	label1: nop
	        bra.b label1
	or
	        align4
	label2: bra.w label2
	The processor grants the internal bus if these loops are forced across two longwords.

Figure 32-2 / Page 32-4	Updated the IDCODE register figure to indicate that the reset values for both PRN and PIN are device-dependent.
Appendix A	Deleted entries for nonexistent CACR, ACR0, and ACR1 registers.

4   Addendum for Revision 3

Table 4. MCF52235RM Rev. 2 to Rev. 3 Changes

Location	Description
Throughout	Formatting, layout, spelling, and grammar corrections.
Section 6.5.1.3 / Page 6-5	Changed field name from "External entropy" to "ENT".
Section 6.5.1.4 / Page 6-6	Changed field name from "Random output" to "RANDOM_OUTPUT".
Chapter 7	Added field description tables to Sections 7.7.1.3, 7.7.1.4, and 7.7.1.5.
Section 8.4.2 / Page 8-13	Replaced erroneous sample assembly code for RTC initialization with valid C code.
Table 9-2 / Page 9-2	Deleted superfluous table.
Table 12-6 / Page 12-5	Added missing part identification number for the MCF52231.
Figure 13-5 / Page 13-9	Corrected name of bit 0 (was CWTIC, is CWTIF).
Chapter 15	Added missing information on GSWIACK and GL*m*lACK registers.
Section 11.1.2 / Page 11-1	Removed text "...within the 256-MByte address space (0x8000_0000-0x8FFF_FFFF)".
Table 11-2 / Page 11-2	Removed text "...within the processor's 256-MByte address space..." and "For proper operation, the base address must be set to between 0x8000_0000 and 0x8FFF-8C000.".

Chapter 14	• Changed naming convention for the port pin data/set data registers:
	    Was: PORT*n*P/SET*n* (e.g., PORTNQP/SETNQ)
	    Is: SET*n* (e.g., SETNQ)
	• Changed naming convention for the bits in the port pin data/set data registers:
	    Was: PORT*n*P*x* (e.g., PORTNQP6)
	    Is: SET*nx* (e.g., SETNQP6)

Section 14.6.5.4 / Page 14-14	Changed PDSR definition (was PDSR [48 bits], is PDSR0 [32 bits] and PDSR1 [16 bits]).
Figure 16-3 / Page 16-4	Replaced register figure with correct 8-bit version.
Section 17.3.2 / Page 17-4	Deleted erroneous reference to external boot mode.
Table 18-11 / Page 18-19	Added RMON_R_DROP counter.

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Table 4. MCF52235RM Rev. 2 to Rev. 3 Changes (continued)

Location	Description
Section 18.5.4.5 / Page 18-25	• Added missing ECR register figure. • Corrected cross-reference in the note of Table 18-16.
Section 18.5.4.23 / Page 18-41	Corrected IPSBAR offset of EMRBR (was 0x11B8, is 0x1188).
Chapter 19	• Reorganized information throughout entire chapter. • Updated register addresses to include proper IPSBAR offsets. • Converted register field descriptions to SRS format. • Corrected register mnemonics as necessary to ensure consistent register naming. • Numerous grammar and stylistic corrections.
Table 20-4 / Page 20-8	Deleted erroneous reference to nonexistent AT bit.
Chapter 22	Deleted erroneous references to nonexistent PIT2 and PIT3 modules.
Section 23.6.13 / Page 23-12	Deleted reference to nonexistent CF bits in the figure and bit descriptions for the GPTFLG2 register.
Chapter 24	Updated register figures and tables to include correct register addresses.
Chapter 25	Added missing equations in Section 25.4.
Chapter 27	Updated register figures and tables to include correct register addresses.
Table 30-1 / Page 30-5	Corrected RXGMASK address (was 0xC_0010, is 0x1C_0010).
Section 30.3.1/ Page 30-6	Added missing illustration of BIts 15:0 in the CANMCR figure and updated field description table accordingly.
Section 30.3.7 / Page 30-15	Added missing IMASK register figure and updated field description table accordingly.
Section 30.3.8 / Page 30-15	Added missing IFLAG register figure and updated field description table accordingly.
Figure 30-9 / Page 30-13	Corrected register mnemonic (was CANCTRL, is ERRSTAT).
Appendix A	• Added GSWIACK register. • Removed trailing R from the names of the global level m IACK registers. • Updated PDSR register names (PDSR0 at IPSBAR+0x10_007C, PDSR1 at IPSBAR+0x10_007A). • Added FEC registers. • Renamed GPIO port pin data/set data registers using the new naming convention (see entry for Chapter 14).

5 Addendum for Revision 2

Table 5. MCF52235RM Rev. 1 to Rev. 2 Changes

Location	Description
Throughout	Language, punctuation, and layout improvements.
Title page	Added "This product incorporates SuperFlash® technology licensed from SST" statement.
Chapter 1	• Corrected missing and incomplete sentences. • Updated block diagram to include correct peripheral signal names. • Revised package information.
Section 1.4.3 / Page 1-10	Corrected second sentence to read "... a 256-bit boundary-scan register...".

Table 5. MCF52235RM Rev. 1 to Rev. 2 Changes (continued)

Location	Description

Table 2-1 / Section 2.2	• Set table caption to repeat on every page.
	• Changed footnote 11 to "VDD1, VDD2, VDDPLL and PHY_VDD pins are for decoupling only, and should NOT have power directly applied to them." and corrected references so that only pins VDDPLL, PHY_VDDA, PHY_VDDRX, PHY_VDDTX, and VDD reference this footnote.
	• Corrected pin numbers as follows:
	    QSPI_CS0, 80 LQFP package: should be 28 instead of 58
	    FlexCAN SYNCA, 112 LQFP package: should be 28 instead of —
	    FlexCAN SYNCA, 80 LQFP package: should be 20 instead of —
	    FlexCAN SYNCB, 112 LQFP package: should be 27 instead of —
	    FlexCAN SYNCB, 80 LQFP package: should be 19 instead of —
	    VSSX, 121MAPBGA package: should be — instead of an empty cell

Section 3.2.11 / Page 3-8	Added cross-reference to FLASHBAR register.
Chapter 6	• Added register and bit acronyms. • Removed references to FIFO-based functionality for RNGOUT. • Formatted register figures and descriptions in accordance with manual conventions.
Chapter 7	Replaced "Low-Power Divider Register (LPDR)" with "Low-Power Control Register (LPCR)" and corrected its address to match the rest of the document.
Chapter 8	Replaced all register addresses with correct values and updated several register names.
Table 8-1 / Page 8-3	Corrected register names in memory map table - changed RCCTL to RTCCTL, DAYS to DAYR, ALARM_DAY to DAY_ALARM.
Section 8.2.1 / Page 8-3	Updated explanation of reset condition (POR resets RTC) in HOURMIN and SECONDS register descriptions
Section 8.2.1.5 / Page 8-7	Deleted extraneous XTL bit description in RTCCTL register description.
Section 8.3.3 / Page 8-12	Deleted extraneous sentence "For example, to turn off the LCD controller..." in Minute Stopwatch description.
Section 11.1.1 / Page 11-1	Corrected SRAM size.
Chapter 14	• Corrected register addresses to include proper offset (IPSBAR+0x10_....). • Updated register figures to SRS standards. • Corrected register figure titles and added field description tables. • In section 14.6.5, changed "If multiple pins are configured for the one function, then the rsult is undefined" to "Some signals can be assigned to different pins (see Table 2-1). However, a signal should not be assigned to more than one pin at the same time. If a signal is assigned to two or more pins simultaneously, the result is undefined."
Figure 14-1 / Page 14-2	Revised signal names to match the names in Chapter 2.
Section 15.1 / Page 15-2	Added cross-reference to exception vector assignments table in the ColdFire Core chapter.
Section 15.1.1.3 / Page 15-3	Updated exception vector mapping instructions and added cross-reference to exception vector assignments table in the ColdFire Core chapter.
Table 15-2 / Page 15-4	• Changed the first interrupt controller number from INTC to INTC0. • Added abbreviation ICBA (Interrupt Controller Base Address) to base address column.
Table 15-3 / Page 15-5	• Replaced references to IPSBAR with proper reference to ICBA in module offset column. • Added *n* to appropriate register names.
Figure 15-2 / Page 15-6	• Changed register name from IPSBMT to IPRL*n*. • Changed field label from INT[16:1] to INT[15:1].
Figure 15-4 / Page 15-8	Changed field label from INT_MASK[16:1] to INT_MASK[15:1].

Table 5. MCF52235RM Rev. 1 to Rev. 2 Changes (continued)

Location	Description
Figure 15-6 / Page 15-9	Changed field label from INTFRCL[16:1] to INTFRCL[15:1].
Section 15.3	Replaced references to IPSBAR with proper reference to ICBA in register figures.
Section 15.3.3 / Page 15-10	Removed duplicate INTFRCL*n* register figure (Figure 15-7).
Table 15-14 / Page 15-15	Corrected FlexCAN section such that source descriptions and flag clearing mechanisms match the corresponding flags.
Section 15.3.7 / Page 15-17	Changed the placeholder letter in the register name from "*n*" to "*m*" (i.e., L*m*IACK).
Chapter 17	• Added clarifying text and reference to Table 17-1 to footnote of CFMSEC, CFMPROT, CFMSACC, and CFMDACC registers. • Added missing titles to register field description tables. • Changed prefix for hexadecimal numbers from $ to 0x.Updated register addresses to include correct IPSBAR offsets.
Section 17.3 / Page 17-4	Added definition and description of FLASHBAR register.
Chapter 20	• Added missing registers to Table 20-1. • Updated register figures to include proper register names and addresses. • Combined Sections 20.3.4 and 20.3.4.1, and revised text to clarify the structure of the BCR*n* and DSR*n* registers. • Added missing figure and bit descriptions for the DCR*n* registers.
Section 21.6 / Page 21-8	• Added cross-reference to CFMCLKD register. • Changed "f$_{SYS}$" to "f$_{SYS/2}$". • Updated values and examples to reflect the 60 MHz system clock. • Added clarifying text to example for calculating FCLK.
Chapter 22	Deleted references to nonexistent PIT2 and PIT3 modules.
Chapter 24	Changed signal names DT*n*IN to DTIN*n* and DT*n*OUT to DTOUT*n* to match the convention used in the rest of the document.
Section 24.1.2 / Page 24-2	• Changed maximum timeout period from 266,521 seconds (~74 hours) to 293,203 s (~81 hours) and related frequency from 66 MHz to 60 MHz. • Changed resolution from 15 ns to 17 ns and related frequency from 66 MHz to 60 MHz.
Section 24.4.2 / Page 24-10	Changed example frequency from 66 MHz to 60 MHz and the result of Equation 24-2 from 2.00 seconds to 2.20 seconds.
Section 25.1.3 / Page 25-2	• Changed minimum baud rate from 129.4 Kbps to 117.6 Kbps. • Changed maximum baud rate from 16.6 Mbps to 15 Mbps. • Changed frequency from 66 MHz to 60 MHz.
Table 25-8 / Page 25-14	• Changed internal bus clock speed from 66 MHz to 60 MHz. • Changed QSPI_CLK values to match the correct 60 MHz clock speed per Equation 25-1 (15 MHz, 7.5 MHz, 3.75 MHz, 1.88 MHz, 937.5 kHz, and 117.6 kHz for QMR = 2, 4, 8, 16, 32, and 255, respectively).
Section 25.5 / Page 25-16	Changed step 1 from "... a QSPI_CLK frequency of 4.125 MHz (assuming a 66-MHz..." to "...a QSPI_CLK frequency of 3.75 MHz (assuming a 60-MHz...".
Chapter 26	Changed signal names to match the convention used in the rest of the document (DT*n*IN to DTIN*n*, DT*n*OUT to DTOUT*n*, U*n*$\overline{\text{RTS}}$ to $\overline{\text{URTS}n}$, U*n*$\overline{\text{CTS}}$ to $\overline{\text{UCTS}n}$, U*n*RXD to URXD*n*, U*n*TXD to UTXD*n*).
Section 26.4.1.2.1 / Page 26-19	• Changed numerator in Equation 26-1 from f$_{sys/2}$ to f$_{sys}$. • Changed values in Equation 26.2 to reflect a 60-MHz clock.
Chapter 28	Deleted superfluous Table 28-5.

Table 5. MCF52235RM Rev. 1 to Rev. 2 Changes (continued)

Location	Description
Section 28.5.7 / Page 28-32	Deleted extraneous sentence at end of first paragraph.
Figure 28-15 / Page 28-26	Changed address of CTRL2 register from IPSBAR+0x19_0001 to IPSBAR+0x19_0002.
Table 31-5 / Page 31-8	Added bit description for the BKD bit in the Configuration/Status Register (CSR).
Section 32.4.3 / Page 32-7	Added missing Table 32-5 (JTAG instructions).
Table A-3	• Corrected spelling of IPSBAR for the ICR034, ICR134, and GPTACFORC registers. • Added missing registers CFMCLKSEL, ICR016, and ICR116. • Added leading zeros to addresses as necessary to adhere to four-digit address convention. • Corrected address of the PPMRH, PPMRL, and GPTAPACNT registers. • Corrected addresses of the DMA controller module registers to match the values in the text. • Corrected several GPIO register names to match the memory map. • Corrected several real-time clock register names. • Updated ADC register entries to show correct register names, addresses, and bit sizes.

6 Addendum for Revision 1

Table 6. MCF52235RM Rev. 0 to Rev. 1 Changes

Location	Description
Throughout	Corrected various spelling, grammar, style, cross-reference, and layout errors.
Table 2-1 / Section 2.2	• Added pin assignments to 121MAPBGA packaging. • Added footnote describing limited functionality when using external PHY. • Corrected various pin assignments and functions. • Deleted duplicate CANTX and CANRX footnote.
Chapter 7	Removed references to 1:1 PLL mode, as it is not available on MCF521x and MCF522xx parts.
Figure 7-1 / Page 7-3	Added PLL pre-divider block.
Table 7-3 / Page 7-5	Added register name (CCHR) to Clock Control High Register and changed reset value from 0x00 to 0x04.
Table 7-4 / Page 7-7	In the description for MFD, changed footnote 1 to include correct equations and values.
Section 7.7.1.4 / Page 7-10	Changed register name from PFD to CCHR and changed reset value from 0b000 to 0b100.
Section 7.8.2 / Page 7-11	Added text to first sentence to: "... reference frequency (i.e., clock frequency divided by the pre-division factor specified by CCHR)..."
Table 8-1 / Section 8.2	Corrected first column to display the proper IPSBAR offset.
Chapter 8	Corrected the addresses in the register figures to show the proper IPSBAR address instead of $BASE_ADDRESS address.
Fig. 8-13 / Page 8-14	Deleted invalid reference to ARM instruction code segment.
Table 9-3/ Page 9-3	• Corrected field order - Bit 13 is CDRNGA, Bit 12 is CDEPHY. • In description for CDGPT, replaced "ICOC" with "GPT".
Section 9.2.4.1 / Page 9-9	Corrected LPCR figure and table - STPMD is a 2-bit field (bits 4 and 3), and bit 1 is LVDSE.
Chapter 11	Corrected conditional text entries to ensure proper display of memory sizes.
Table 11-2 / Page 11-3	Filled in table in PRIU/PRIL field description.
Figure 14-1 / Page 14-2	Added FEC signals and arranged signals in same order as in Table 2-1.

Table 6. MCF52235RM Rev. 0 to Rev. 1 Changes (continued)

Location	Description
Table 14-1 / Page 14-5	Corrected register name at offset $007C to "PDSR" instead of "PDRR".
Section 14.6.5.4 / Page 14-14	Added clear references to footnotes of Figures 14-25, 14-26, and 14-27.
Section 18.5.4.5 / Page 18-25	Added note about loss of functionality when using external PHY.
Section 18.5.4.7 / Page 18-28	Changed formula in paragraph above Table 18-19 to "... 1/(2*5)" instead of "... 1/10" to match layout of equation in Table 18-18 better.
Table 18-19 / Page 18-29	Changed system clock frequency from 66 MHz to 60 MHz to reflect highest possible clock frequency.
Section 19.2.9 / Page 19-4	Replaced "Flashes in half-duplex mode when a collision occurs on the network..." with "Flashes when a collision occurs on a network in half duplex mode...".
Section 20.4	Removed duplicate register figures.
Section 27.6.1 / Page 27-12	Added missing line of code to note: `I2CR = 0x80     ; re-enable`
Section 27.6.2 / Page 27-13	Replaced instances of MBB with IBB.
Section 29.2	Replaced "Address" with "IPSBAR Offset" in the register figures.

7 Revision History

Table 7 provides a revision history for this document.

Table 7. Revision History Table

Rev. Number	Substantive Changes	Date of Release
0	Initial release.	04/2006
1	Various technical corrections as described in Table 6.	06/2006
2	Various technical corrections as described in Table 5.	08/2006
3	Various technical corrections as described in Table 4.	11/2006
4	Various technical corrections as described in Table 3.	01/2007

Table 7. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
5	• Various technical corrections as described in Table 2. • Added missing corrections against the following entities to Table 3: Table 3-1 Figure 3-5 Table 3-2 Figure 3-8 Section 3.4 Section 3.6.6 Figure 4-4 Figure 4-5 Equation 4-3 Table 11-1 Section 11.2.1 Table 31-10 Figure 31-8 Table 31-22 Section 31.6.2 • Changed the headings and table titles to specify both the old and the new revision numbers.	08/2007
6.0	Corrected errors in Chapter "Clock Module" and "FlexCAN" as described in Table 1	12/2011

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