MCF5227x
ColdFire® embedded microprocessor

Target Applications
- HVAC building and control systems
- Security and access control systems
- Lighting control systems
- Test and measurement equipment
- Environmental and building automation
- Point-of-sale systems
- Operator interfaces
- Patient monitoring systems
- Laboratory equipment
- High-end appliances

Overview
Freescale's MCF5227x ColdFire® microprocessor family is the ideal device for developers looking to add more control options to their consumer or industrial applications. Featuring an integrated LCD controller and touchscreen module, the MCF5227x family is designed to provide an easy way to add support for graphical LCD interfaces to industrial systems. The MCF5227x devices are also equipped with integrated USB On-The-Go (OTG) and CAN modules giving developers the ability to upgrade or standardize their serial communications. The crossbar switch allows the 128K of integrated SRAM to be accessed by the core, DMA, USB OTG and LCD controller, which helps improve performance. These and other features make the MCF5227x devices ideal for human interface applications that require a broad range of peripherals and high performance for multi-functional industrial and consumer applications.
The MCF5227x family is also easy to use. Freescale provides a comprehensive suite of development tools to help developers design in these devices quickly and easily.

Cost-Effective Development Tools

CodeWarrior® Development Studio for ColdFire Architectures V7.0 Complimentary**
CodeWarrior Development Studio for ColdFire Architectures V7.0 is a single tool suite that supports software development for Freescale's ColdFire family of 32-bit products. This support coupled with the cross-platform capabilities of the award-winning CodeWarrior Integrated Development Environment (IDE) simplifies code migration and re-use for faster product development. Processor Expert™, a graphical device initialization tool, is also available in the development studio.

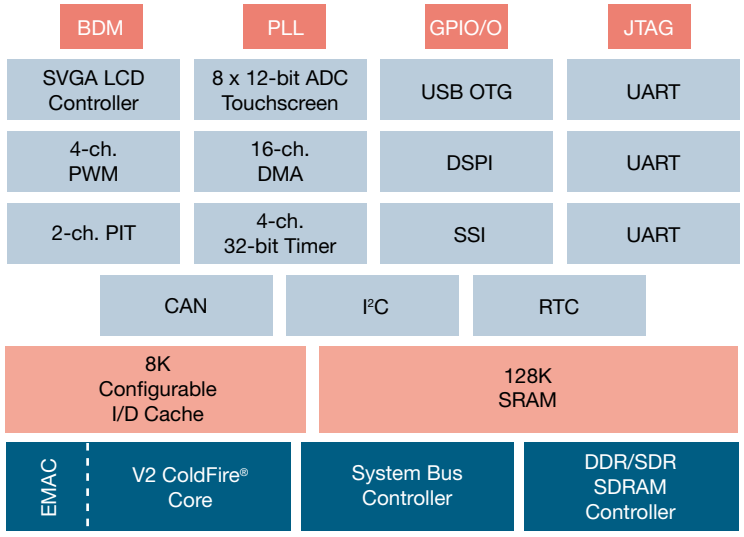
Linux® Board Support Package Complimentary**
Linux Board Support Packages (BSPs) for Freescale silicon are tested and certified, ensuring a fully operational tool chain, kernel and board specific modules that are ready to use together within a fix configuration for specific hardware reference platforms. These BSPs provide the foundation you need to begin your project quickly.

M52277EVB
$449*
The M52277EVB is a full development system for the MCF5227x microprocessor family. Featuring a 3.5" LCD panel, the M52277EVB allows evaluation of the major features on the MCF5227x devices, including the LCD and touchscreen controller, USB OTG, CAN and several other peripherals.

*Prices indicated are MSRP
**Subject to license agreement

Part Number	Temp Ranges	Package
MCF52277CVM160	-40°C to +85°C	196 BGA
MCF52274CLU120	-40°C to +85°C	176 QFP

MCF5227 Block Diagram



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ColdFire

Features	Benefits
CPU and System Configuration	
• 32-bit V2 ColdFire Central Processing Unit (CPU) offering 152 MIPS at 160 MHz • 1.5V Core, 1.8V, 2.5V, 3.3V Bus I/O	• Offers strong performance and functionality for improved system performance throughout the entire voltage and temperature range
• Enhanced Multiply Accumulate (eMAC)	• For digital signal processing and fast multiply operations
• Cross Bar Switch Technology (XBS)	• Enables concurrent, non-blocking accesses to peripherals, RAM or external memory from multiple bus masters
• Reset Controller	• Separate reset in and reset out signals • Six sources of reset: power-on reset (POR), external, software, watchdog timer, loss of lock and JTAG instruction
• Interrupt Controllers	• Two interrupt controllers supporting up to 64 interrupt sources each, organized as seven programmable levels • Combinational path to provide wake-up from low power modes
Memory	
• 128K Dual Ported SRAM	• Large bank of memory for enhanced performance. Data available in one clock cycle.
• 8K Cache	• Configurable as instruction only, data only or split instruction/data (I/D)
• SDR/DDR SDRAM Controller	• Supports a glueless interface to SDR, DDR, and mobile DDR SDRAM devices • Supports up to 512 MB of memory; minimum memory configuration of 8 MB
• FlexBus (External Interface)	• Glueless connections to 8-, 16- and 32-bit external memory devices • Up to six chip selects available
Power Management	
• Low Power Operating Modes	• Fully static operation with processor sleep and whole chip stop modes • Very rapid response to interrupts from low-power sleep mode • Software controlled disable of external clock output for low power consumption
• Peripheral power management register to enable/disable clocks to most modules	• Allows the enable/disable of clocks to most peripherals, lowering overall power consumption
Peripherals	
• Integrated LCD Controller	• Support for single (non-split) screen monochrome/color LCD panels and self-refresh type LCD panels • Maximum supported panel size of 800 x 600
• ADC and Touchscreen Controller	• 12-bit 125K sample/sec ADC for touchscreen and general purpose measurements • True touchscreen controller (embedded touchscreen circuitry) with support for 4/5/7 and 8 wire configurations
• USB Host, Device and On-the-Go Module	• USB 1.1 and 2.0 compliant full-speed USB controller with DMA
• FlexCAN Module	• Full implementation of the CAN protocol specification version 2.0B • Flexible Message Buffers configurable as receive or transmit
• Synchronous Serial Interface (SSI)	• Supports synchronous transmit and receive sections • Normal, network, and gated clock modes of operation
• Real Time Clock (RTC)	• Full clock; days, hours, minutes and seconds • Ability to wake processor from low-power modes (wait, doze and stop) via the real time clock interrupts
• Programmable Interrupt Timers (PIT)	• Two programmable interrupt timers each with 16-bit counter • Configurable as a down counter or free-running counter
• DMA Timers	• Four 32-bit timers with DMA and interrupt request trigger capability • Input capture and reference compare modes
• DMA Serial Peripheral Interface (DSPI)	• Full-duplex, three-wire synchronous transfer; up to 16 pre-programmed transfers • Up to three chip selects available
• 3x Universal Asynchronous Receiver Transmitters (UARTs)	• Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity • Error-detection capabilities
• I^2C Module	• Interchip bus interface for EEPROMS, LCD controllers, A/D converters and keypads • Fully compatible with industry standard I^2C bus
• Pulse Width Modulation (PWM) Module	• Four independent PWM channels with programmable period and duty cycle
• DMA Controller	• 16 full programmable channels with 32-byte transfer control descriptor
• Phase Locked Loop (PLL)	• Provides 37.5 MHz–160 MHz clock to CPU
• Up to 55 GPIOs	• Bit manipulation support via set/clear functions • Various unused peripheral pins may be used as GPIO
Development Support	
• Background Debug Mode (BDM) Revision B+	• Real time debug support, with four PC break point registers and a pair of address breakpoint registers with optional data
• JTAG Support	• JTAG part identification and part revision numbers

Learn More: For current information about ColdFire products and documentation, please visit **www.freescale.com/coldfire**.

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