MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2128

16K BIT STATIC RAM

The MCM2128 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

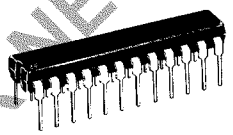
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the chip enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2128 is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout. A 24 pin dual-in-line 600 mil wide package is also available.

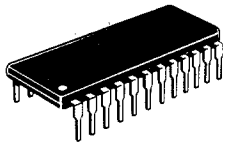
- Single +5 Volt Operation (±10%)
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2128-10 - 100 ns (Maximum)
  MCM2128-12 - 120 ns (Maximum)
  MCM2128-15 - 150 ns (Maximum)
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

MOS
(N-CHANNEL, SILICON-GATE)

2,048 × 8 BIT STATIC RANDOM ACCESS MEMORY

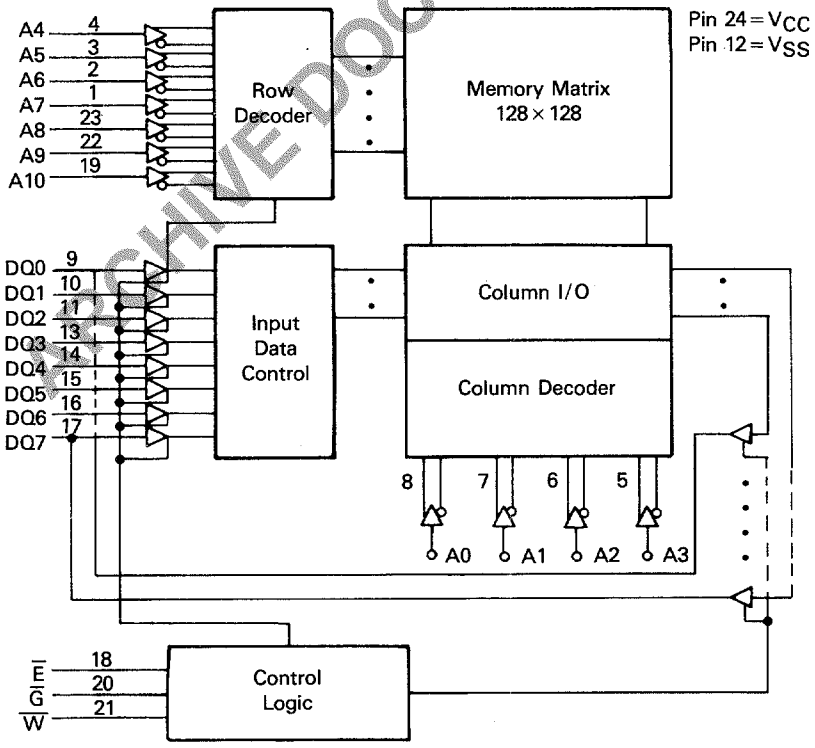


N PACKAGE
300 MIL PLASTIC
CASE 724

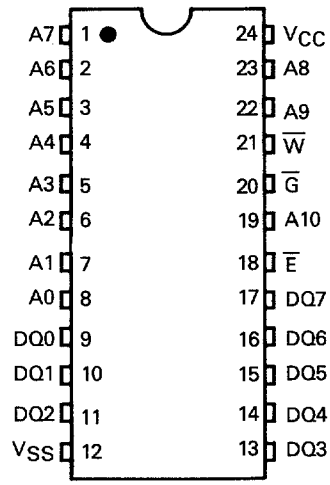


P PACKAGE
600 MIL PLASTIC
CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−0.5 to +7.0	V
DC Output Current	20	mA
Power Dissipation	0.9	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −3 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	I_{LI}	−1.0	+1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	I_{LO}	−1.0	+1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC1}	—	120	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 4.0 mA) See Figure 1	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −2.0 mA) See Figure 1	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except $\overline{E}$, DQ	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	5	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Input Pulse Levels ..... 0 and 3.0 Volts
Input Rise and Fall Times ..... 5 ns
Input and Output Timing Reference Levels ..... 1.5 Volts
Output Load ..... See Figure 1

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM2128-10		MCM2128-12		MCM2128-15		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	100	—	120	—	150	—	ns
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	—	100	—	120	—	150	ns
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	—	100	—	120	—	150	ns
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	—	35	—	50	—	55	ns
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	10	—	10	—	10	—	ns
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	—	5	—	5	—	ns
Chip Enable High to Output High Z (Chip Disable to Output Disable) [2]	t_{EHQZ}	t_{CHZ}	—	40	—	40	—	55	ns
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	5	—	5	—	5	—	ns
Output Enable High to Output High Z (Output Disable to Output Disable) [2]	t_{GHQZ}	t_{OHZ}	—	35	—	35	—	50	ns
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	—	50	—	60	—	60	ns

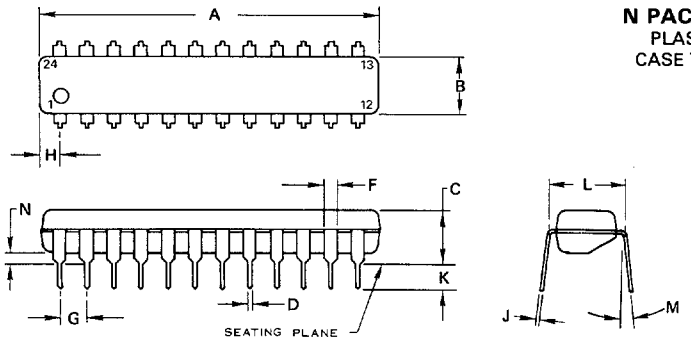
NOTES:
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

WRITE CYCLE (See Notes 1, 3, 4 and 5)

Parameter	Symbol		MCM2128-10		MCM2128-12		MCM2128-15		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	100	—	120	—	150	—	ns
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	80	—	100	—	120	—	ns
Address Valid to Write Low (Address Setup to End of Write)	t_{AVWL}	t_{AS}	10	—	10	—	10	—	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	70	—	85	—	100	—	ns
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	40	—	50	—	60	—	ns
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	5	—	5	—	5	—	ns
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	5	—	5	—	5	—	ns
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	—	30	—	35	—	50	ns

NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. t_{WHAX} is measured from the earlier of chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
3. A write occurs during the overlap of low $\overline{E}$ and low $\overline{W}$.
4. t_{ELWH} is specified as the time from the chip selection to end of write in write cycle and t_{WLWH} is specified as the overlap time of low $\overline{E}$ and low $\overline{W}$.
5. Output enable ($\overline{G}$) can be low or high in write cycle, if $\overline{G}$ is high the output buffers will remain in the high impedance state.
6. If chip enable ($\overline{E}$) and output enable ($\overline{G}$) are low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
7. If the chip enable ($\overline{E}$) low transition occurs simultaneously with or later than the write enable ($\overline{W}$) low transition, the output buffers will remain in the high impedance state.
8. If the chip enable ($\overline{E}$) high transition occurs simultaneously with the write enable ($\overline{W}$) high transition, the output buffers will remain in the high impedance state.

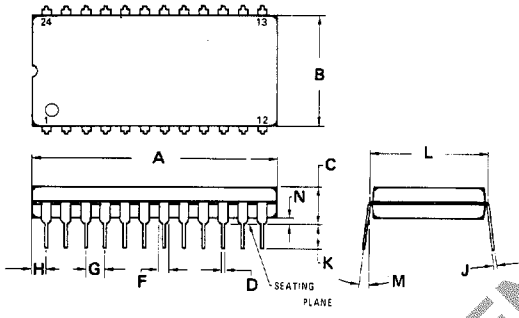
PACKAGE DIMENSIONS



N PACKAGE
PLASTIC
CASE 724-02

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040



P PACKAGE
PLASTIC
CASE 709-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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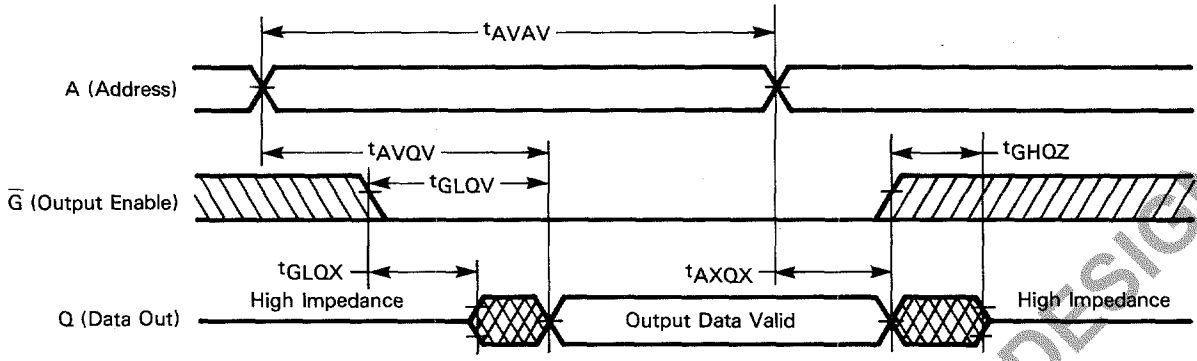
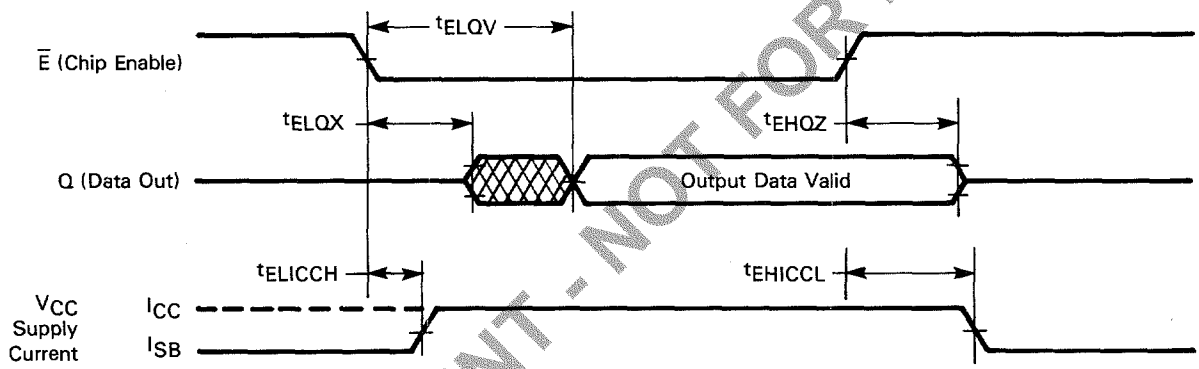
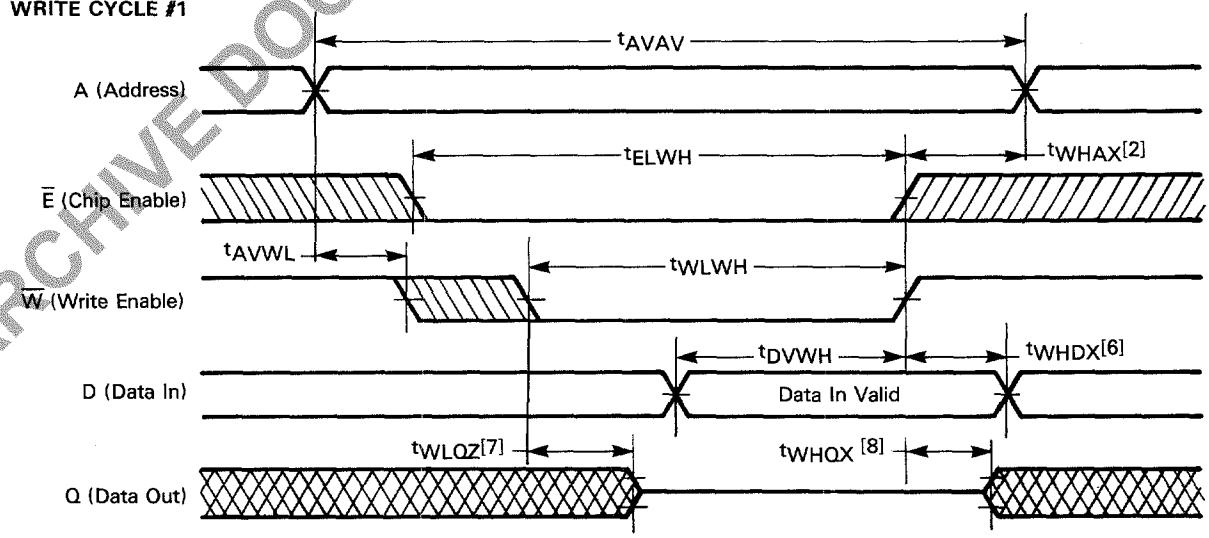
Read Cycle #1 ($\overline{W}=V_{IH}$, $\overline{E}=V_{IL}$)



Read Cycle #2 ($\overline{W}=V_{IH}$, $\overline{G}=V_{IL}$) (See Note 3)



WRITE CYCLE #1



WRITE CYCLE #2

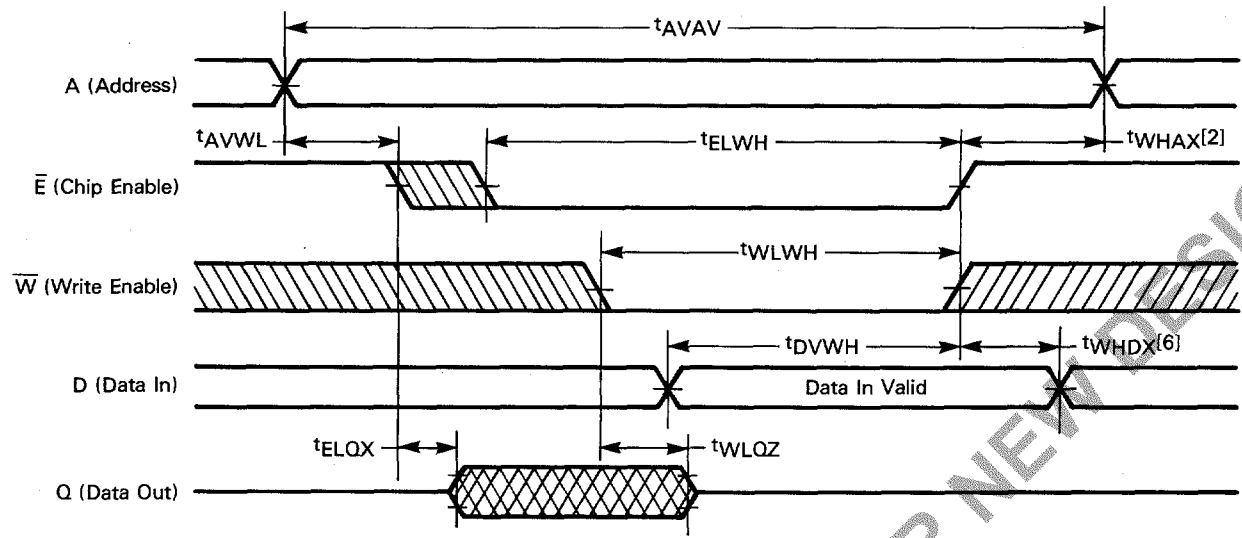


FIGURE 1 — OUTPUT LOAD

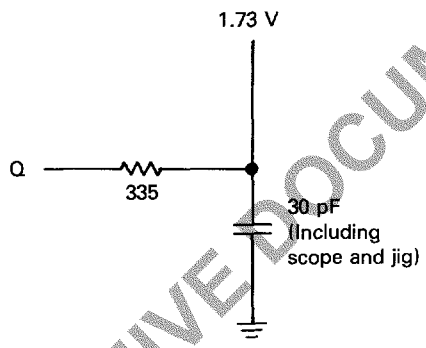


FIGURE 2 — EQUIVALENT LOAD