MCM6949

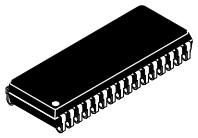
1M x 4 Bit Static Random Access Memory

The MCM6949 is a 4,194,304–bit static random access memory organized as 1,048,576 words of 4 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6949 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6949 is available in a 400 mil, 32–lead surface–mount SOJ package.

- Single 3.3 V – 5%, + 10% Power Supply
- Fast Access Time: 8/10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 195/165/160/155 mA Maximum, Active AC

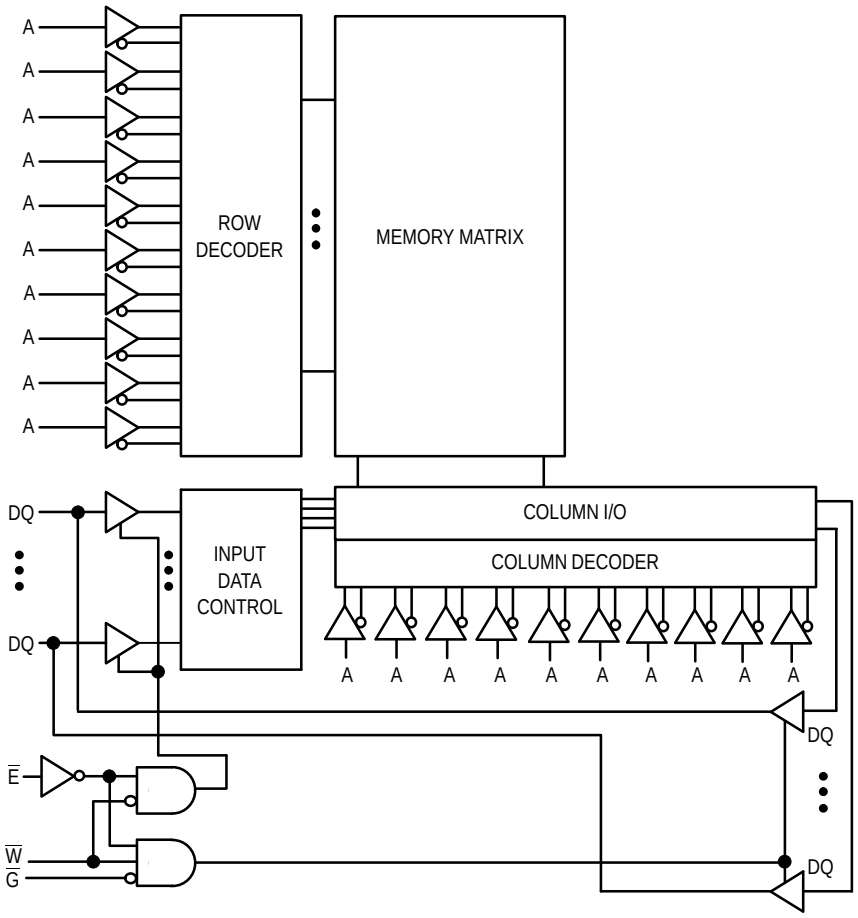


YJ PACKAGE
400 MIL SOJ
CASE 857A–02

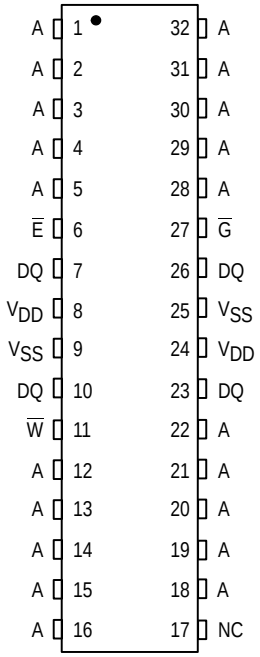
PIN NAMES	
A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Input/Output
NC	No Connection
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground

REV 9
5/20/99

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{DDA}
L	L	H	Read	D_{out}	Read	I_{DDA}
L	X	L	Write	High–Z	Write	I_{DDA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{DD}	– 0.5 to + 5.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V – 5%, + 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.63	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	0 to + 70°C	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{DD} = Max)	MCM6949–8: t_{AVAV} = 8 ns	I_{DD}	195	mA
	MCM6949–10: t_{AVAV} = 10 ns		165	
	MCM6949–12: t_{AVAV} = 12 ns		160	
	MCM6949–15: t_{AVAV} = 15 ns		155	
AC Standby Current (V_{DD} = Max, $\overline{E}$ = V_{IH}, No Other Restrictions on Other Inputs)	MCM6949–8: t_{AVAV} = 8 ns	I_{SB1}	55	mA
	MCM6949–10: t_{AVAV} = 10 ns		50	
	MCM6949–12: t_{AVAV} = 12 ns		50	
	MCM6949–15: t_{AVAV} = 15 ns		45	
CMOS Standby Current ($\overline{E}$ ≥ V_{DD} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V) (V_{DD} = Max, f = 0 MHz)		I_{SB2}	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V – 5%, + 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6949–8		MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	2	—	2	—	2	—	2	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 200 mV from steady–state voltage.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

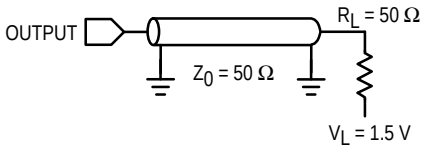
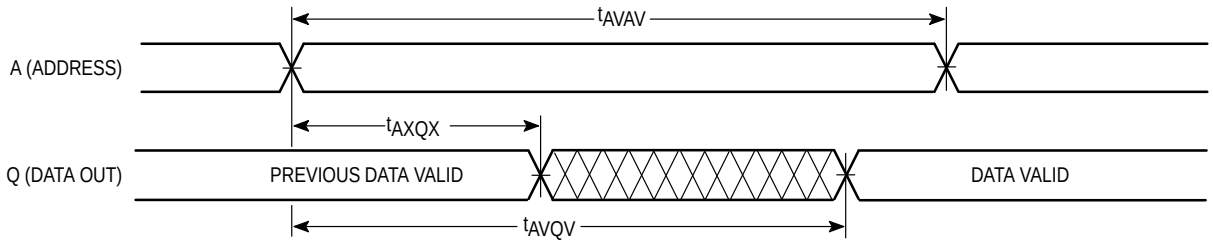


Figure 1. AC Test Load

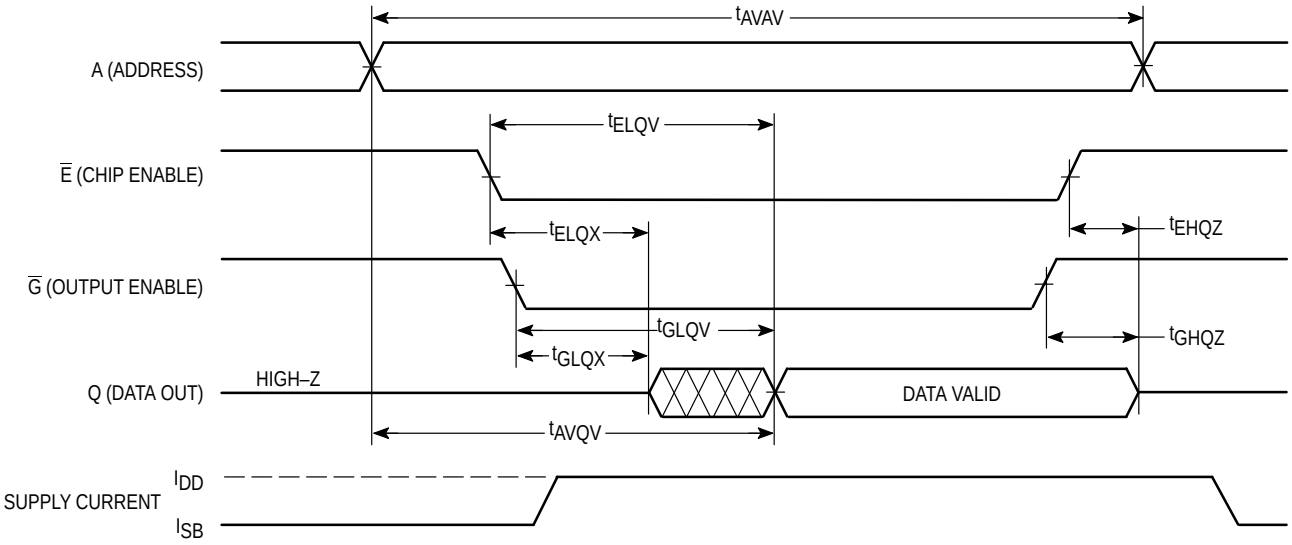
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

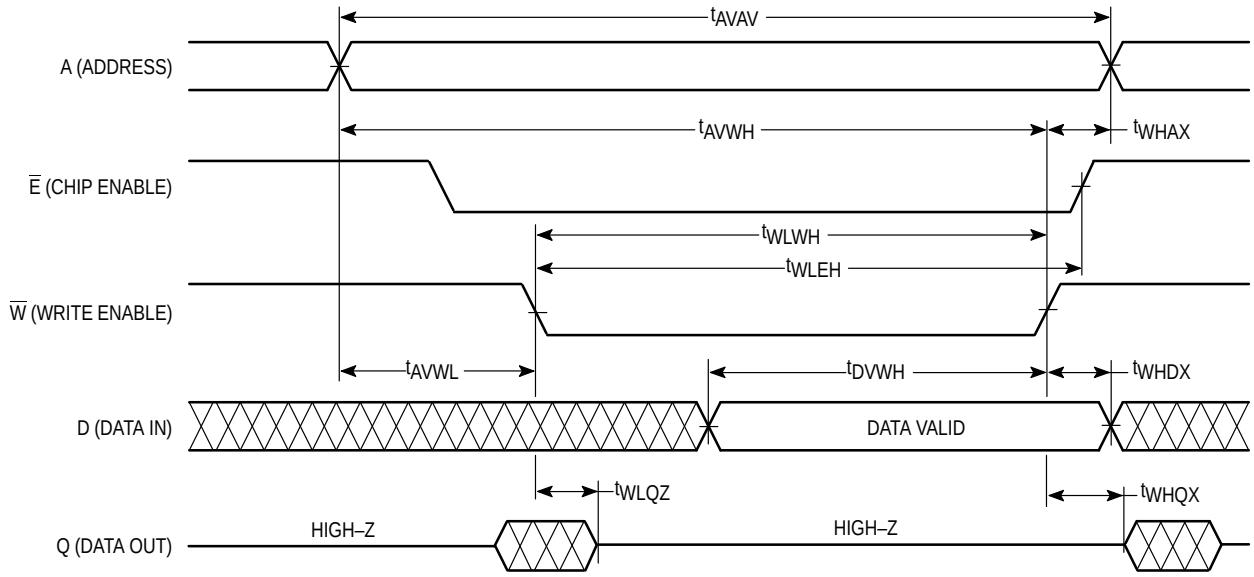


WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6949–8		MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH} t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min, both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

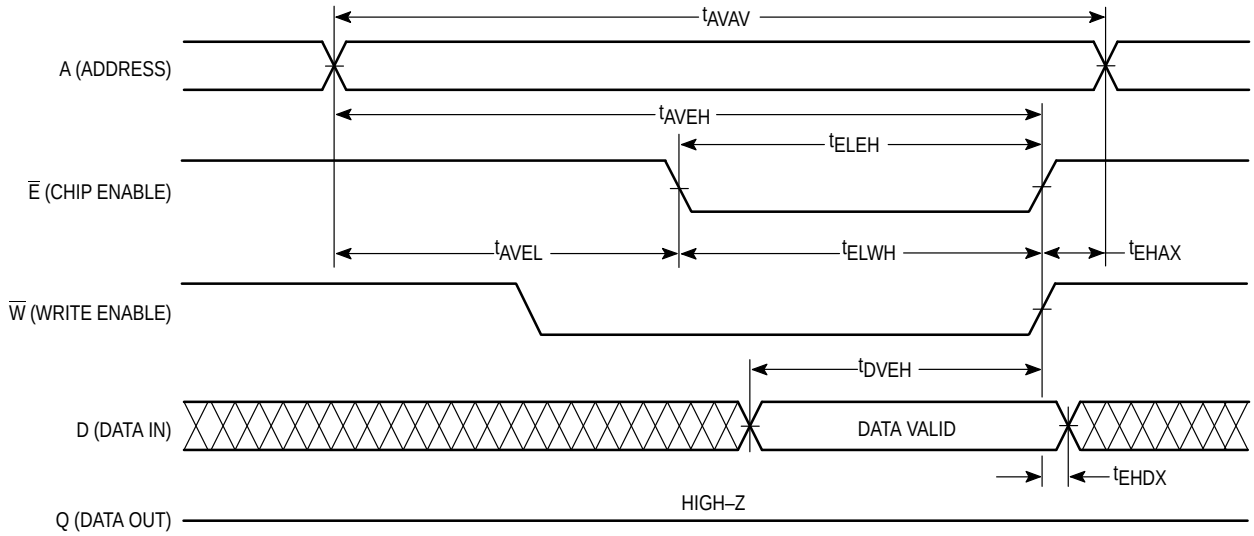


WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6949–8		MCM6949–10		MCM6949–12		MCM6949–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	12	—	ns	5, 6
Enable Pulse Width ($\overline{G}$ High)	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

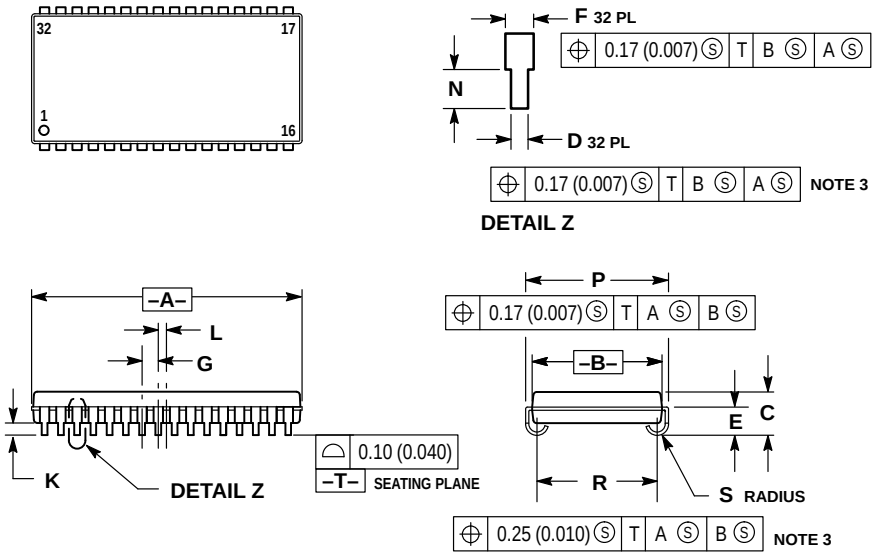
MCM 6949 XX XX XX

- MCM — Motorola Memory Prefix
- 6949 — Part Number
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- XX — Package (YJ = 400 mil SOJ)
- XX — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6949YJ8, MCM6949YJ8R, MCM6949YJ10, MCM6949YJ10R, MCM6949YJ12, MCM6949YJ12R, MCM6949YJ15, MCM6949YJ15R

PACKAGE DIMENSIONS

YJ PACKAGE
400 MIL SOJ
CASE 857A–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE –T–.
4. DIMENSION A AND D DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado, 80217. 1-303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848
– http://sps.motorola.com/mfax/

HOME PAGE: http://motorola.com/sps/

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141, 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 81-3-5487-8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T., Hong Kong. 852-26668334

CUSTOMER FOCUS CENTER: 1-800-521-6274