128K x 36 Bit Flow–Through BurstRAM Synchronous Fast Static RAM

MCM69F737

ZP PACKAGE
PBGA
CASE 999–02

TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F737 is a 4M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the PowerPC™ and other high performance microprocessors. It is organized as 128K words of 36 bits each. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K).

Addresses (SA), data inputs (DQx), and all control signals except output enable (G) and linear burst order (LBO) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either ADSP or ADSC input pins. Subsequent burst addresses can be generated internally by the MCM69F737 (burst sequence operates in linear or interleaved mode dependent upon the state of LBO) and controlled by the burst address advance (ADV) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write (SBx), synchronous global write (SGW), and synchronous write enable (SW) are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". SBa controls DQa, SBb controls DQb, etc. Individual bytes are written if the selected byte writes SBx are asserted with SW. All bytes are written if either SGW is asserted or if all SBx and SW are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F737 operates from a 3.3 V core power supply and all outputs operate on a 2.5 V or 3.3 V power supply. All inputs and outputs are JEDEC standard JESD8–5 compatible.

- MCM69F737–7.5: 7.5 ns Access/8.5 ns Cycle (117 MHz)
  MCM69F737–8: 8 ns Access/10 ns Cycle (100 MHz)
  MCM69F737–8.5: 8.5 ns Access/11ns Cycle (90 MHz)
  MCM69F737–11: 11 ns Access/20 ns Cycle (50 MHz)
- 3.3 V + 10%, – 5% Core Power Supply, 2.5 V or 3.3 V I/O Supply
- ADSP, ADSC, and ADV Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Single–Cycle Deselect Timing
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- PB1 Version 2.0 Compatible
- JEDEC Standard 119–Pin PBGA and 100–Pin TQFP Packages
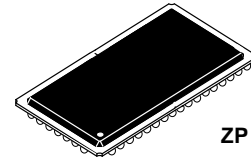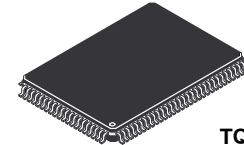
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MOTOROLA

FUNCTIONAL BLOCK DIAGRAM
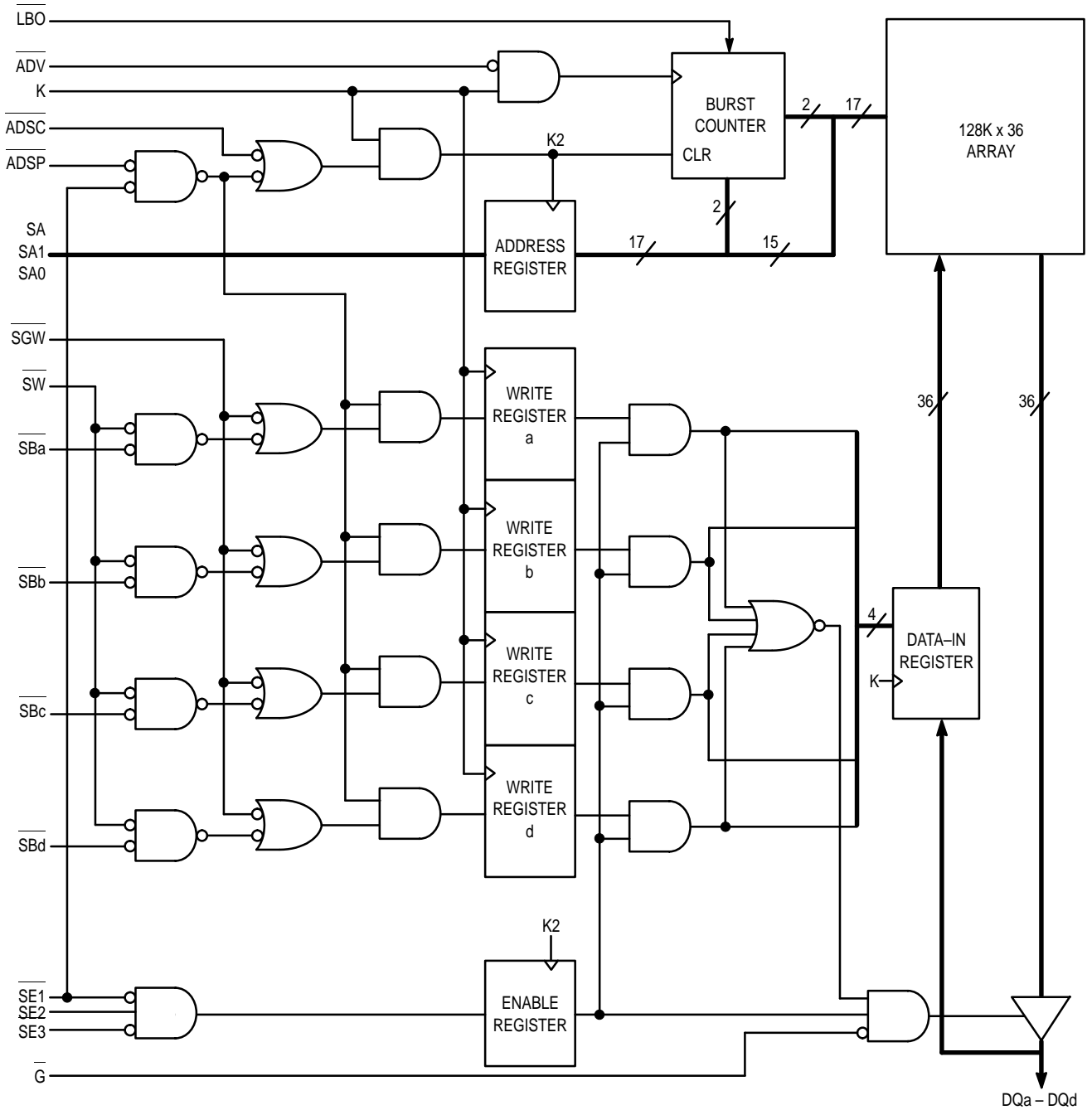
PIN ASSIGNMENTS

TOP VIEW 119 BUMP PBGA

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	ADSP	SA	SA	V_{DDQ}
B	NC	SE2	SA	ADSC	SA	SE3	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	SE1	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	G	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	SBc	ADV	SBb	DQb	DQb
H	DQc	DQc	V_{SS}	SGW	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	SBd	NC	SBa	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	SW	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA1	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA0	V_{SS}	DQa	DQa
R	NC	SA	LBO	V_{DD}	NC	SA	NC
T	NC	NC	SA	SA	SA	NC	NC
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

TOP VIEW 100 PIN TQFP

Top pins (left to right, 100–81): SA, SA, SE1, SE2, SBd, SBc, SBb, SBa, SE3, V_{DD}, V_{SS}, K, SGW, SW, G, ADSC, ADSP, ADV, SA, SA

Bottom pins (left to right, 31–50): LBO, SA, SA, SA, SA, SA1, SA0, NC, NC, V_{SS}, V_{DD}, NC, NC, SA, SA, SA, SA, SA, SA, SA

Left side:

Pin	Signal
1	DQc
2	DQc
3	DQc
4	V_{DDQ}
5	V_{SS}
6	DQc
7	DQc
8	DQc
9	DQc
10	V_{SS}
11	V_{DDQ}
12	DQc
13	DQc
14	NC
15	V_{DD}
16	NC
17	V_{SS}
18	DQd
19	DQd
20	V_{DDQ}
21	V_{SS}
22	DQd
23	DQd
24	DQd
25	DQd
26	V_{SS}
27	V_{DDQ}
28	DQd
29	DQd
30	DQd

Right side:

Pin	Signal
80	DQb
79	DQb
78	DQb
77	V_{DDQ}
76	V_{SS}
75	DQb
74	DQb
73	DQb
72	DQb
71	V_{SS}
70	V_{DDQ}
69	DQb
68	DQb
67	V_{SS}
66	NC
65	V_{DD}
64	NC
63	DQa
62	DQa
61	V_{DDQ}
60	V_{SS}
59	DQa
58	DQa
57	DQa
56	DQa
55	V_{SS}
54	V_{DDQ}
53	DQa
52	DQa
51	DQa

Not to Scale

PBGA PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
4B	ADSC	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
4A	ADSP	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ, WRITE, or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
4G	ADV	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P (b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H (c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4F	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
4K	K	Input	Clock: This signal registers the address, data in, and all control signals except G and LBO.
3R	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 3T, 4T, 5T	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
4N, 4P	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
5L, 5G, 3G, 3L (a) (b) (c) (d)	SBx	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
4E	SE1	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks ADSP or deselects chip when ADSC is asserted.
2B	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
6B	SE3	Input	Synchronous Chip Enable: Active low for depth expansion.
4H	SGW	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
4M	SW	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
4C, 2J, 4J, 6J, 4R	V_{DD}	Supply	Core Power Supply.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	Supply	I/O Power Supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground.
1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

TQFP PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADSC	Input	Synchronous Address Status Controller: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a READ, WRITE, or chip deselect.
84	ADSP	Input	Synchronous Address Status Processor: Active low, interrupts any ongoing burst and latches a new external address. Used to initiate a new READ, WRITE, or chip deselect (exception — chip deselect does not occur when ADSP is asserted and SE1 is high).
83	ADV	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	G	Input	Asynchronous Output Enable Input: Low — enables output buffers (DQx pins). High — DQx pins are high impedance.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except G and LBO.
31	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low — linear burst counter (68K/PowerPC). High — interleaved burst counter (486/i960/Pentium).
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1, SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	SBx	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). SGW overrides SBx.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — blocks ADSP or deselects chip when ADSC is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	SE3	Input	Synchronous Chip Enable: Active low for depth expansion.
88	SGW	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the SBx and SW signals. If only byte write signals SBx are being used, tie this pin high.
87	SW	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins. If only byte write signals SBx are being used, tie this pin low.
15, 41, 65, 91	V$_{DD}$	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V$_{DDQ}$	Supply	I/O Power Supply.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V$_{SS}$	Supply	Ground.
14, 16, 38, 39, 42, 43, 64, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 Through 5)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	High–Z	X[5]
Begin Read	External	0	1	0	1	0	X	0	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES:
1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any SBx and SW low or 2) SGW is low.
3. G is an asynchronous signal and is not sampled by the clock K. G drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, G must be negated prior to the start of the write cycle to ensure proper write data setup times. G must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This read assumes the RAM was previously deselected.

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{DD})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	SGW	SW	SBa	SBb	SBc	SBd
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	V_{SS} − 0.5 to + 4.6	V	
I/O Supply Voltage	V_{DDQ}	V_{SS} − 0.5 to V_{DD}	V	2
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	V_{SS} − 0.5 to V_{DD} + 0.5	V	2
Input Voltage (Three–State I/O)	V_{IT}	V_{SS} − 0.5 to V_{DDQ} + 0.5	V	2
Output Current (per I/O)	I_{out}	± 20	mA	
Package Power Dissipation	P_D	1.6	W	3
Ambient Temperature	T_A	0 to 70	°C	
Die Temperature	T_J	110	°C	3
Temperature Under Bias	T_{bias}	− 10 to 85	°C	
Storage Temperature	T_{stg}	− 55 to 125	°C	

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER- ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady–state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static volt- ages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maxi- mum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS — PBGA

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	38 22	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	14	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	5	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

PACKAGE THERMAL CHARACTERISTICS — TQFP

Rating		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	1, 2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, − 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS: 2.5 V I/O Supply (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
I/O Supply Voltage	V_{DDQ}	2.375	2.5	2.9	V
Input Low Voltage	V_{IL}	− 0.3	—	0.7	V
Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V
Input High Voltage (I/O Pins)	V_{IH2}	1.7	—	V_{DDQ} + 0.3	V

RECOMMENDED OPERATING CONDITIONS: 3.3 V I/O Supply (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
I/O Supply Voltage	V_{DDQ}	3.135	3.3	V_{DD}	V
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V
Input High Voltage	V_{IH}	2	—	V_{DD} + 0.5	V
Input High Voltage (I/O Pins)	V_{IH2}	2	—	V_{DDQ} + 0.5	V
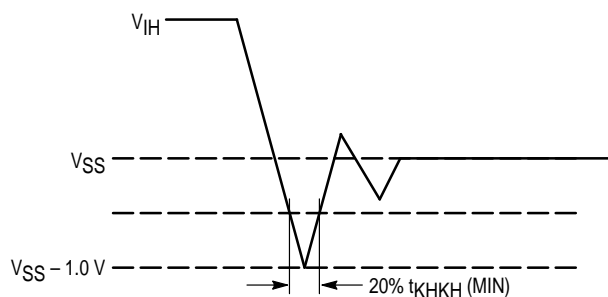
Figure 1. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current ($0\ V \leq V_{in} \leq V_{DD}$)	$I_{lkg(I)}$	—	—	± 1	μA	
Output Leakage Current ($0\ V \leq V_{in} \leq V_{DDQ}$)	$I_{lkg(O)}$	—	—	± 1	μA	
AC Supply Current (Device Selected, MCM69F737–7.5 All Outputs Open, Freq = Max) MCM69F737–8 Includes V_{DD} Only MCM69F737–8.5 MCM69F737–11	I_{DDA}	—	—	350 325 300 250	mA	1, 2, 3
CMOS Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at CMOS Levels)	I_{SB2}	—	—	45	mA	4, 5
TTL Standby Supply Current (Device Deselected, Freq = 0, V_{DD} = Max, All Inputs Static at TTL Levels)	I_{SB3}	—	—	50	mA	4, 6
Clock Running (Device Deselected, MCM69F737–7.5 Freq = Max, V_{DD} = Max, MCM69F737–8 All Inputs Toggling at CMOS Levels) MCM69F737–8.5 MCM69F737–11	I_{SB4}	—	—	190 175 165 145	mA	4, 5
Static Clock Running (Device Deselected, Freq = Max, V_{DD} = Max, All Inputs Static at TTL Levels)	I_{SB5}	—	—	95	mA	4, 6
Output Low Voltage (I_{OL} = 2 mA) V_{DDQ} = 2.5 V	V_{OL}	—	—	0.7	V	
Output High Voltage (I_{OL} = – 2 mA) V_{DDQ} = 2.5 V	V_{OH}	1.7	—	—	V	
Output Low Voltage (I_{OL} = 8 mA) V_{DDQ} = 3.3 V	V_{OL2}	—	—	0.4	V	
Output High Voltage (I_{OL} = – 4 mA) V_{DDQ} = 3.3 V	V_{OH2}	2.4	—	—	V	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing.
2. All addresses transition simultaneously low (LSB) then high (MSB).
3. Data states are all zero.
4. Device is deselected as defined by the Truth Table.
5. CMOS levels for I/O's are $V_{IT} \leq V_{SS}$ + 0.2 V or $\geq V_{DDQ}$ – 0.2 V. CMOS levels for other inputs are $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ – 0.2 V.
6. TTL levels for I/O's are $V_{IT} \leq V_{IL}$ or $\geq V_{IH2}$. TTL levels for other inputs are $V_{in} \leq V_{IL}$ or $\geq V_{IH}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . 1.25 V
Input Pulse Levels . . . . 0 to 2.5 V
Input Rise/Fall Time . . . . 1.0 V/ns (20 to 80%)

Output Timing Reference Level . . . . 1.25 V
Output Load . . . . See Figure 2 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM69F737–7.5 117 MHz		MCM69F737–8 100 MHz		MCM69F737–8.5 90 MHz		MCM69F737–11 50 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	8.5	—	10	—	11	—	20	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	7.5	—	8	—	8.5	—	11	ns	
Output Enable to Output Valid	t_{GLQV}	—	3.5	—	3.5	—	3.5	—	3.5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	0	—	ns	3, 4, 5
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	2	—	ns	3, 4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	3, 4
Output Disable to Q High–Z	t_{GHQZ}	—	3.5	—	3.5	—	3.5	—	3.5	ns	3, 4
Clock High to Q High–Z	t_{KHQZ}	2	3.5	2	3.5	2	3.5	2	3.5	ns	3, 4, 5
Setup Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	1.5	—	2	—	2	—	2	—	ns	
Hold Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, $SE2$ high, and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. This parameter is sampled and not 100% tested.
4. Measured at ± 200 mV from steady state.
5. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
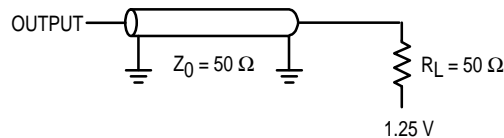
Figure 2. AC Test Load
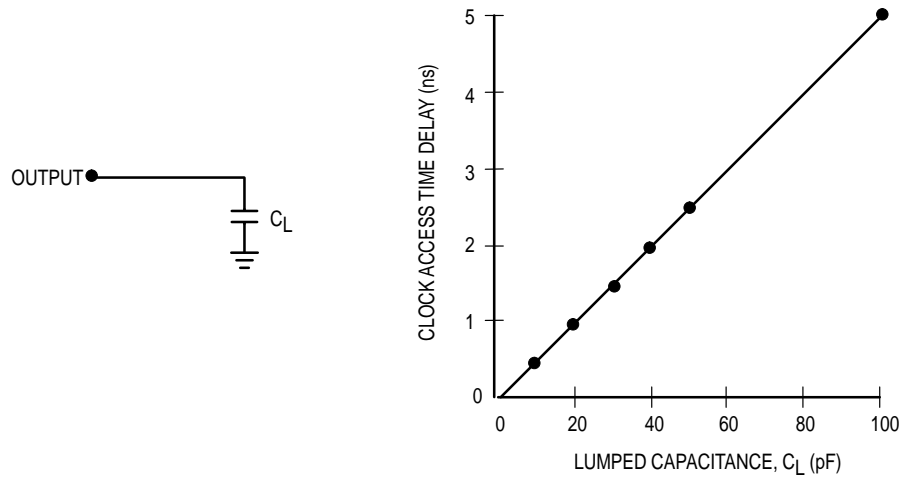
Figure 3. Lumped Capacitive Load and Typical Derating Curve

OUTPUT LOAD

OUTPUT
BUFFER

TEST POINT
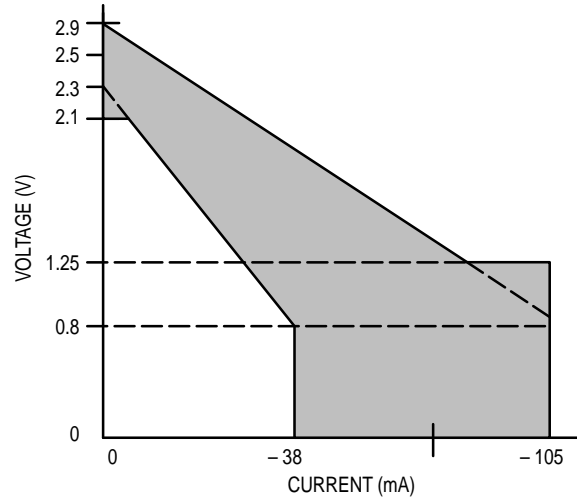
UNLOADED RISE AND FALL TIME MEASUREMENT
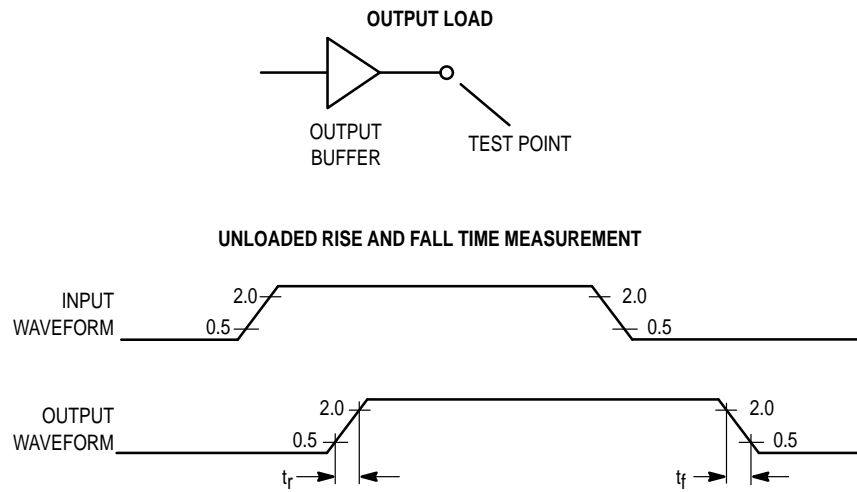
NOTES:
    1. Input waveform has a slew rate of 1 V/ns.
    2. Rise time is measured from 0.5 to 2.0 V unloaded.
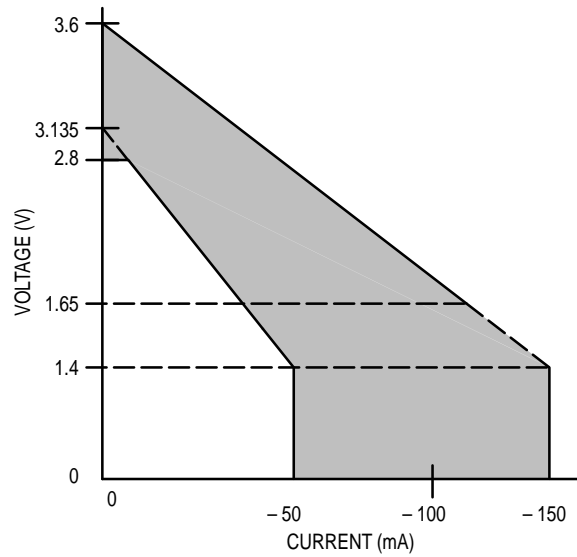   3. Fall time is measured from 2.0 to 0.5 V unloaded.

Figure 4. Unloaded Rise and Fall Time Characterization

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 38	– 105
0	– 38	– 105
0.8	– 38	– 105
1.25	– 26	– 83
1.5	– 20	– 70
2.3	0	– 30
2.7	0	– 10
2.9	0	0

(a) Pull–Up for 2.5 V I/O Supply

PULL–UP		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	– 50	– 150
0	– 50	– 150
1.4	– 50	– 150
1.65	– 46	– 130
2.0	– 35	– 101
3.135	0	– 25
3.6	0	0

(b) Pull–Up for 3.3 V I/O Supply

PULL–DOWN		
VOLTAGE (V)	I (mA) MIN	I (mA) MAX
– 0.5	0	0
0	0	0
0.4	10	20
0.8	20	40
1.25	31	63
1.6	40	80
2.8	40	80
3.2	40	80
3.4	40	80
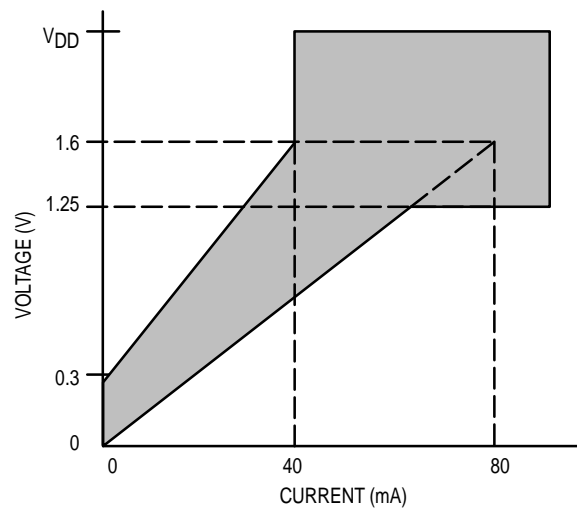
(c) Pull–Down

Figure 5. Typical Output Buffer Characteristics

READ/WRITE CYCLES

Signal labels (top to bottom): K, SA, $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$, $\overline{\text{ADV}}$, $\overline{\text{SE1}}$, $\overline{\text{E}}$, $\overline{\text{W}}$, $\overline{\text{G}}$, DQx

Timing parameters: t_{KHKH}, t_{KHKL}, t_{KLKH}, t_{KHQV}, t_{KHQX1}, t_{KHQX2}, t_{KHQZ}, t_{GHQZ}, t_{GLQV}, t_{GLQX}

SA values: A, B, C, D

DQx values: Q(n), Q(A), Q(B), Q(B+1), Q(B+2), Q(B+3), Q(B), D(C), D(C+1), D(C+2), D(C+3), Q(D)

Cycle labels: DESELECTED, SINGLE READ, BURST READ, BURST WRITE, SINGLE READ

BURST WRAPS AROUND

$\overline{\text{ADSP}}$, SA
SE2, $\overline{\text{SE3}}$
IGNORED
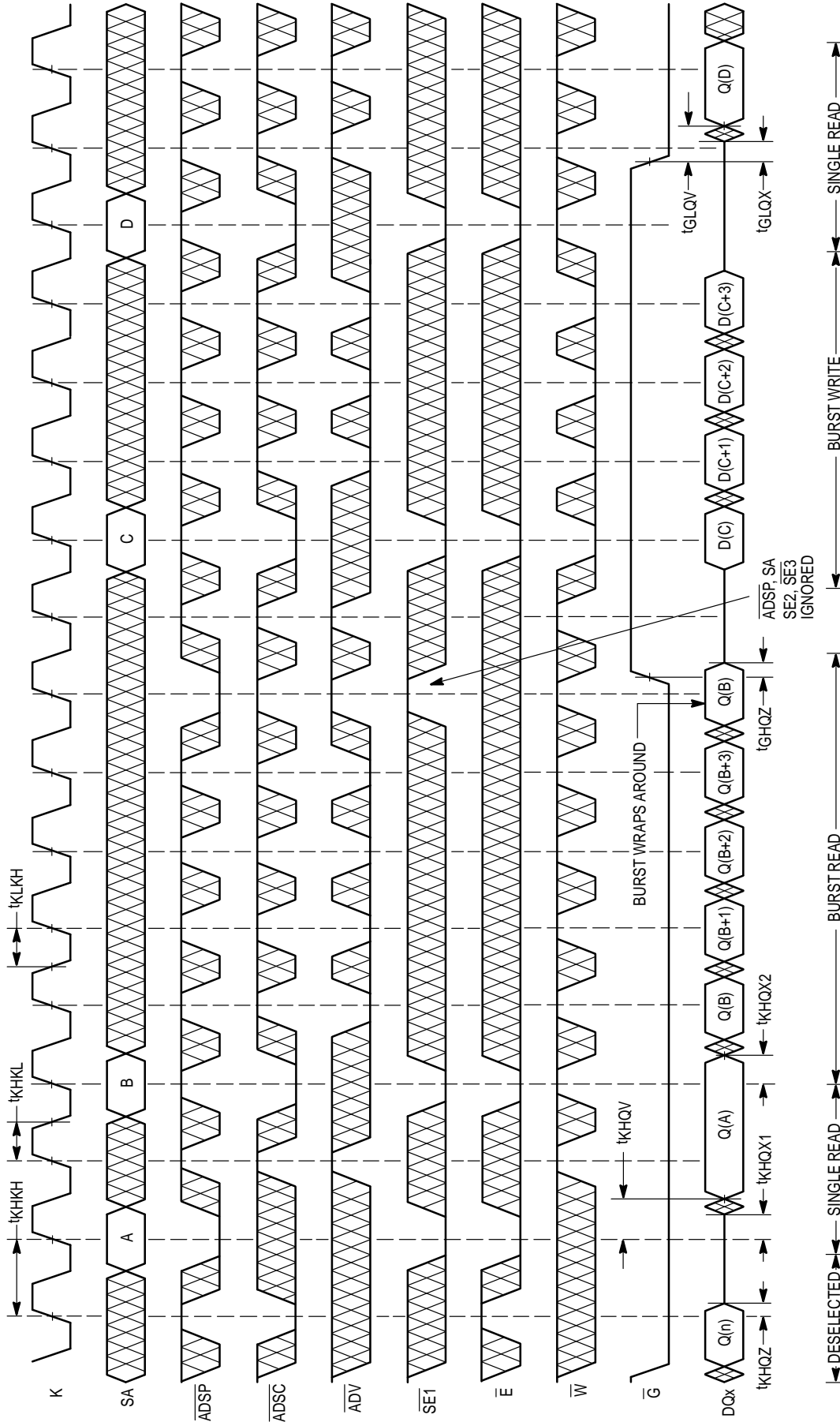
NOTE: $\overline{\text{E}}$ low = SE2 high and $\overline{\text{SE3}}$ low.
$\overline{\text{W}}$ low = $\overline{\text{SGW}}$ low and/or $\overline{\text{SW}}$ and $\overline{\text{SBx}}$ low.

APPLICATION INFORMATION

STOP CLOCK OPERATION

In the stop clock mode of operation, the SRAM will hold all state and data values even though the clock is not running (full static operation). The SRAM design allows the clock to start with ADSP and ADSC, and stops the clock after the last write data is latched, or the last read data is driven out.

When starting and stopping the clock, the AC clock timing and parametrics must be strictly maintained. For example, clock pulse width and edge rates must be guaranteed when starting and stopping the clocks.

To achieve the lowest power operation for all three stop clock modes, stop read, stop write, and stop deselect:

- Force the clock to a low state.
- Force the control signals to an inactive state (this guarantees any potential source of noise on the clock input will not start an unplanned on activity).
- Force the address inputs to a low state (V_{IL}), preferably < 0.2 V.

STOP CLOCK WITH READ TIMING
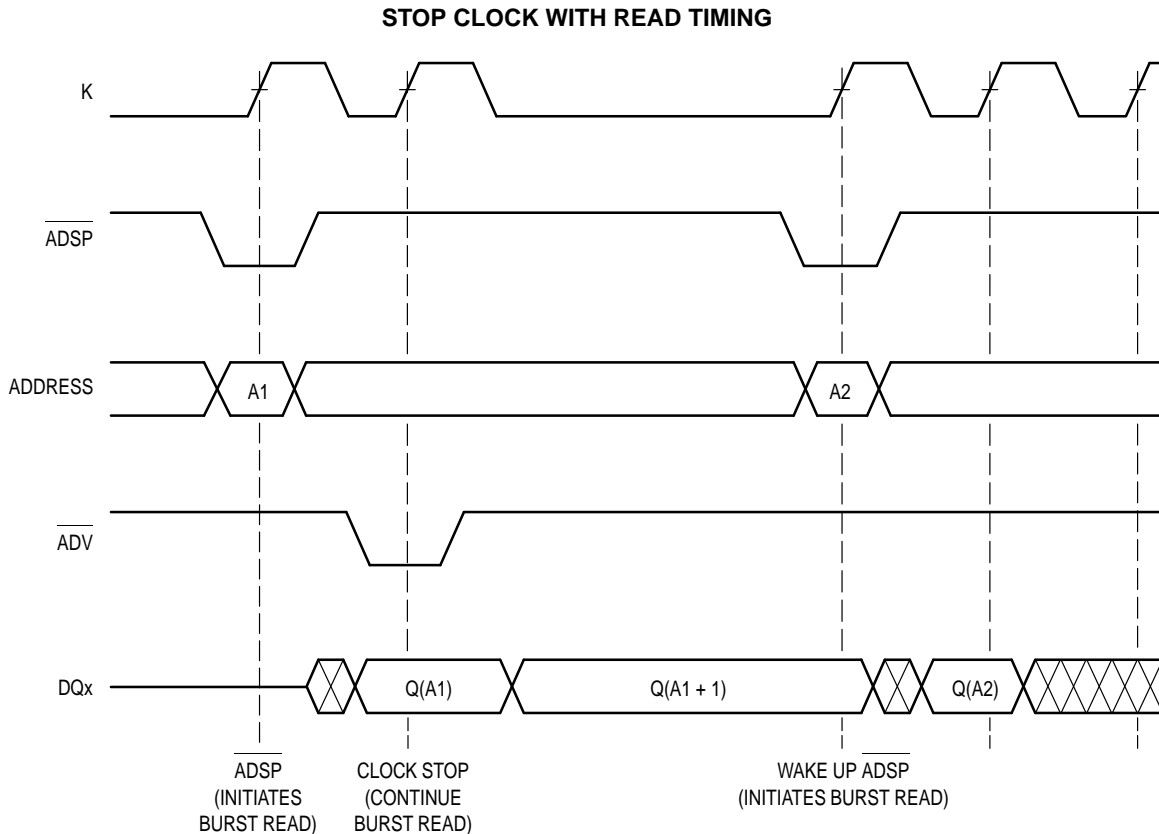
NOTE: For lowest possible power consumption during stop clock, the addresses should be driven to a low state (V_{IL}). Best results are obtained if V_{IL} < 0.2 V.

STOP CLOCK WITH WRITE TIMING
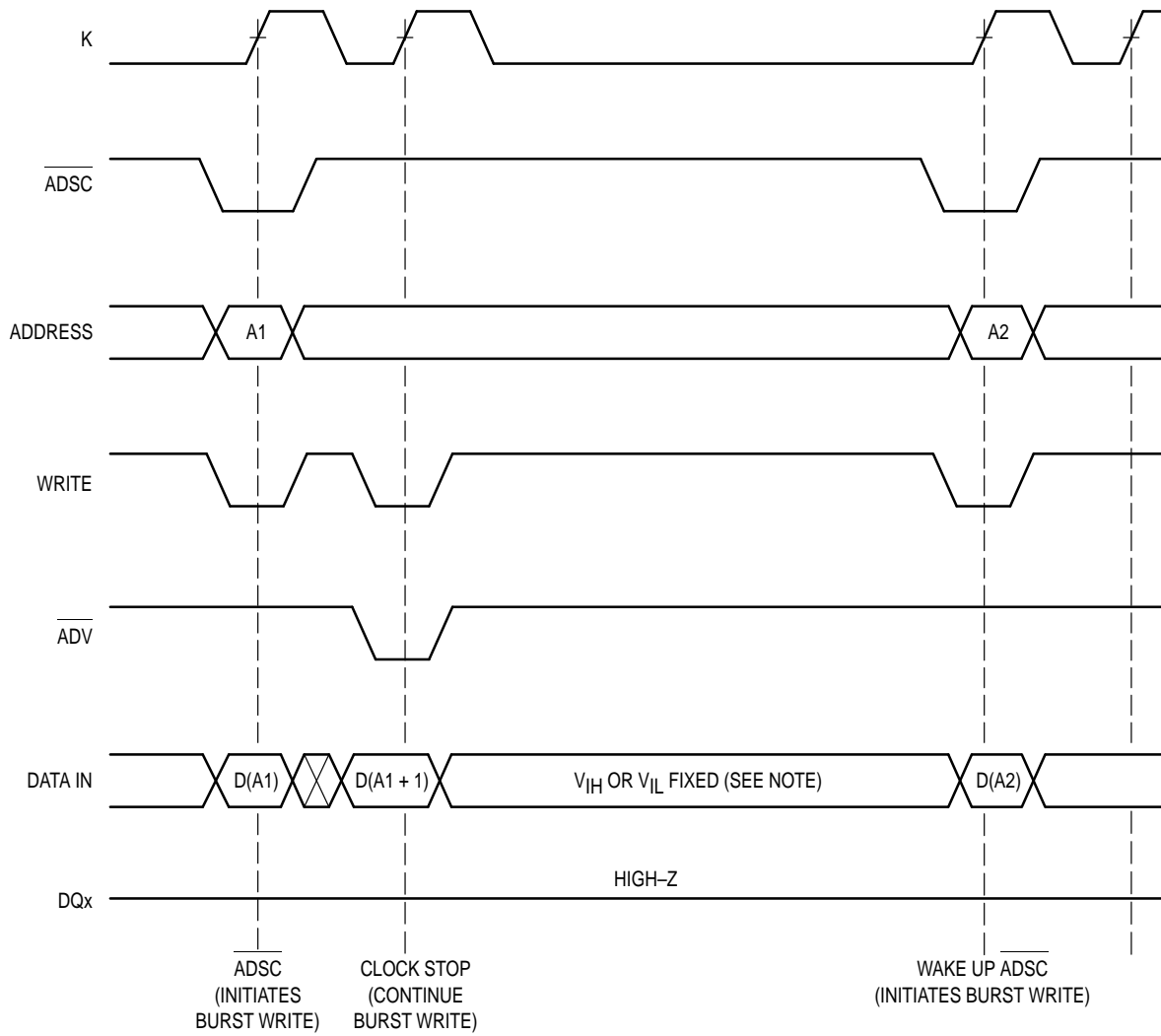
K

$\overline{\text{ADSC}}$

ADDRESS   A1   A2

WRITE

$\overline{\text{ADV}}$

DATA IN   D(A1)   D(A1 + 1) V_{IH} OR V_{IL} FIXED (SEE NOTE)   D(A2)

DQx   HIGH–Z

ADSC
(INITIATES
BURST WRITE)

CLOCK STOP
(CONTINUE
BURST WRITE)

WAKE UP $\overline{\text{ADSC}}$
(INITIATES BURST WRITE)

NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

STOP CLOCK WITH DESELECT OPERATION TIMING
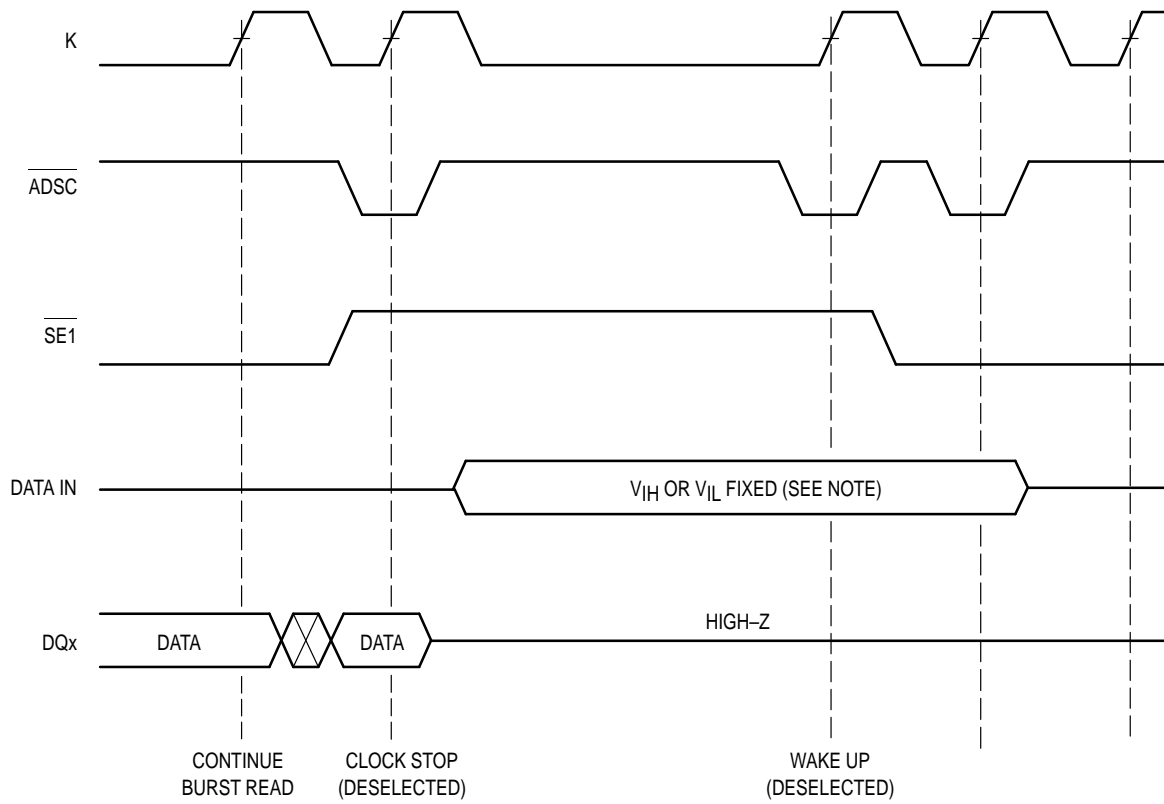
K		
$\overline{ADSC}$		
$\overline{SE1}$		
DATA IN	V_{IH} OR V_{IL} FIXED (SEE NOTE)	
DQx	DATA · DATA · HIGH–Z	

CONTINUE BURST READ   CLOCK STOP (DESELECTED)   WAKE UP (DESELECTED)

NOTE: While the clock is stopped, DATA IN must be fixed in a high (V_{IH}) or low (V_{IL}) state to reduce the DC current of the input buffers. For lowest power operation, all data and address lines should be held in a low (V_{IL}) state and control lines held in an inactive state.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for PowerPC–based and other high end MPU–based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous inter-face can make use of the MCM69F737. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 6.

CONTROL PIN TIE VALUES EXAMPLE (H ≥ V_{IH}, L ≤ V_{IL})

Non–Burst	ADSP	ADSC	ADV	SE1	SE2	LBO
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	H	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.
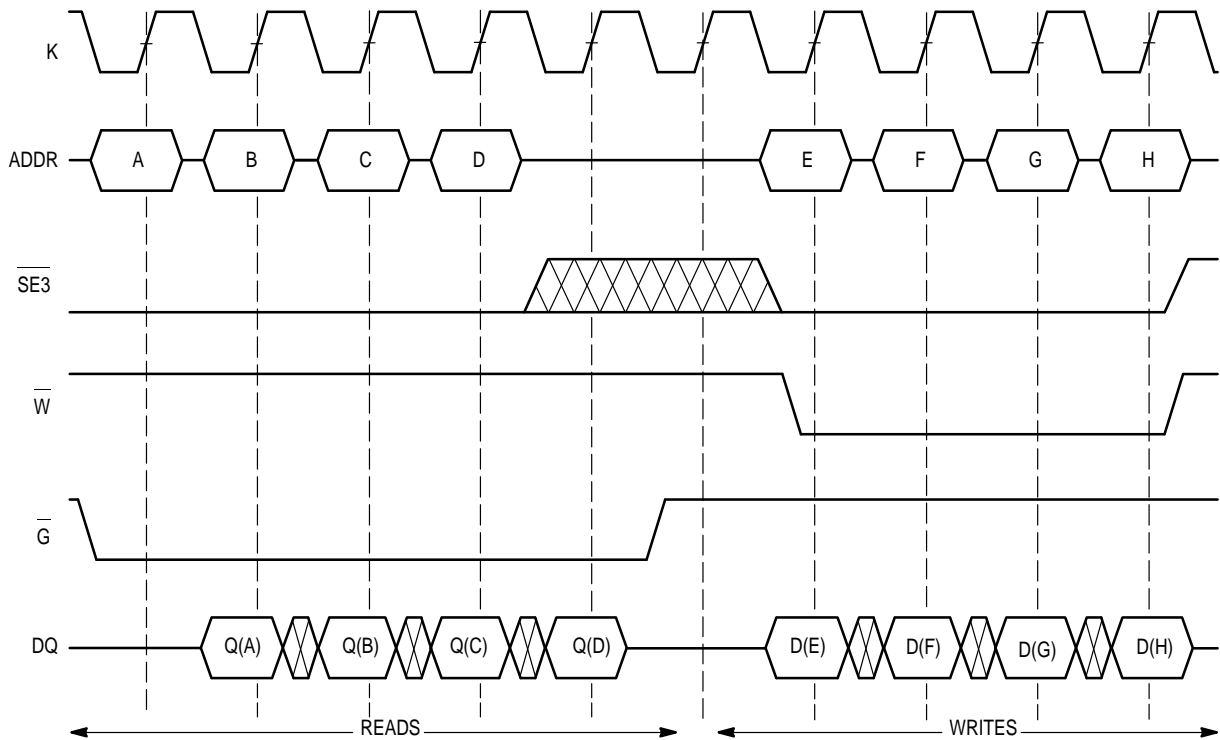
Figure 6. Example Configuration as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)

MCM **69F737** **XX** **X** **X**

Motorola Memory Prefix

Part Number

Blank = Trays, R = Tape and Reel

Speed (7.5 = 7.5 ns, 8 = 8 ns, 8.5 = 8.5 ns, 11 = 11 ns)

Package (ZP = PBGA, TQ = TQFP)

Full Part Numbers —
MCM69F737ZP7.5	MCM69F737ZP8	MCM69F737ZP8.5	MCM69F737ZP11
MCM69F737ZP7.5R	MCM69F737ZP8R	MCM69F737ZP8.5R	MCM69F737ZP11R
MCM69F737TQ7.5	MCM69F737TQ8	MCM69F737TQ8.5	MCM69F737TQ11
MCM69F737TQ7.5R	MCM69F737TQ8R	MCM69F737TQ8.5R	MCM69F737TQ11R

PACKAGE DIMENSIONS

ZP PACKAGE
7 x 17 BUMP PBGA
CASE 999–02

TOP VIEW

BOTTOM VIEW
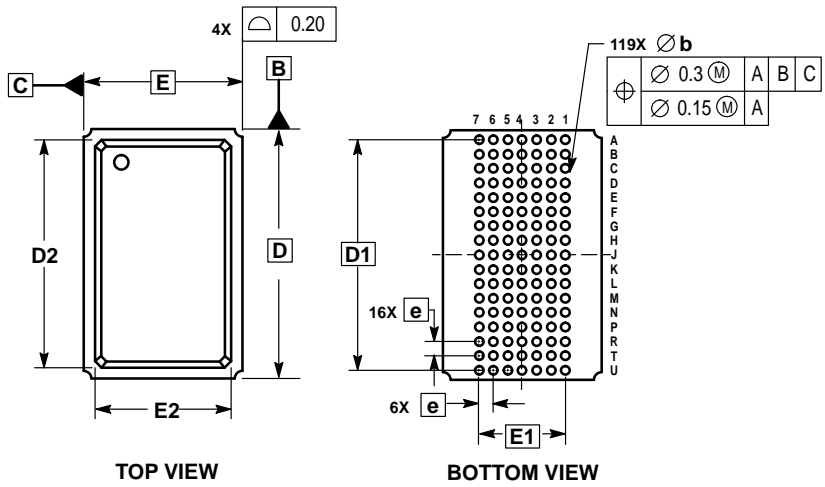
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. ALL DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	—	2.40
A1	0.50	0.70
A2	1.30	1.70
A3	0.80	1.00
D	22.00 BSC	
D1	20.32 BSC	
D2	19.40	19.60
E	14.00 BSC	
E1	7.62 BSC	
E2	11.90	12.10
b	0.60	0.90
e	1.27 BSC	
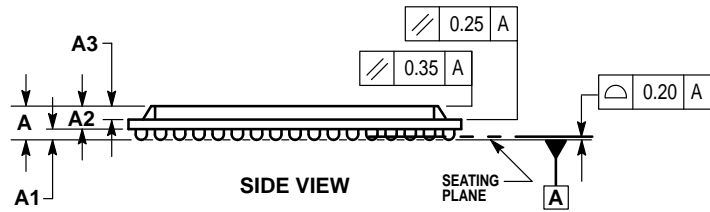
SIDE VIEW

SEATING PLANE

TQ PACKAGE
TQFP
CASE 983A–01

4X
| ⌒ | 0.20 (0.008) | H | A–B | D |

2X 30 TIPS
| ⌒ | 0.20 (0.008) | C | A–B | D |

—D—

80 51
81 50

—A—

—B—

E/2

E1 E

E1/2

100 31
1 30

D1/2 D/2

D1

D

2X 20 TIPS
| ⌒ | 0.20 (0.008) | C | A–B | D |

A

—H—

—C—
SEATING
PLANE

θ2

θ3

| ⌒ | 0.10 (0.004) | C |

VIEW AB

| — | 0.05 (0.002) Ⓢ |

S

θ1

A2

0.25 (0.010)
GAGE PLANE

R2

A1

R1

L2

L

L1

θ

VIEW AB

e

e/2

B

B

—X—

X=A, B, OR D

VIEW Y

BASE
METAL

PLATING

b1

c

c1

b

| ⊕ | 0.13 (0.005) Ⓜ | C | A–B Ⓢ | D Ⓢ |
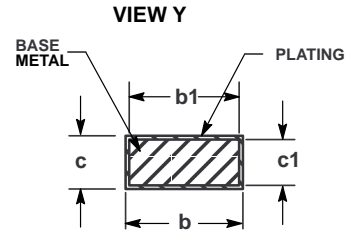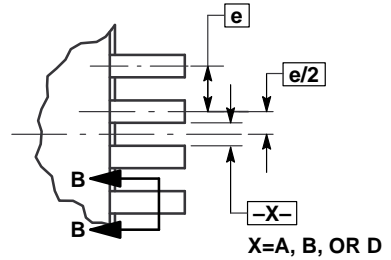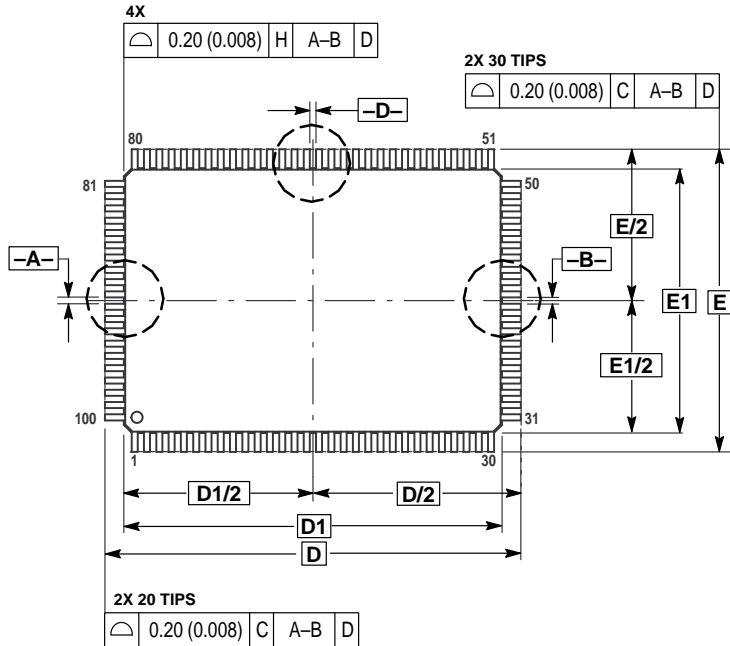
SECTION B–B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).
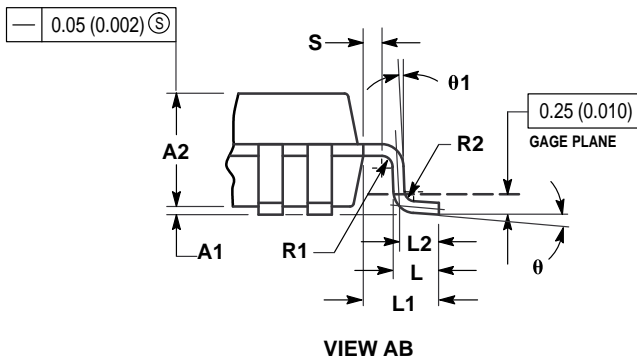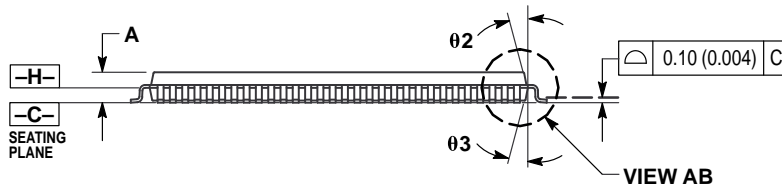
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	——	1.60	——	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	——	0.008	——
R1	0.08	——	0.003	——
R2	0.08	0.20	0.003	0.008
θ	0 °	7 °	0 °	7 °
θ1	0 °	——	0 °	——
θ2	11 °	13 °	11 °	13 °
θ3	11 °	13 °	11 °	13 °

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