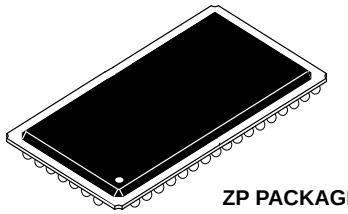
# MCM69L737A
# MCM69L819A

*Advance Information*

# 4M Late Write LVTTL



**ZP PACKAGE**
**PBGA**
**CASE 999–01**

The MCM69L737A/819A is a 4 megabit synchronous late write fast static RAM designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The MCM69L819A organized as 256K words by 18 bits, and the MCM69L737A organized as 128K words by 36 bits wide are fabricated in Motorola's high performance silicon gate BiCMOS technology.

The differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock a cycle after address and control signals. Read data is available at the falling edge of the CK clock.

The RAM uses LVTTL 3.3 V inputs and outputs.

The synchronous write and byte enables allow writing to individual bytes or the entire word.

- Byte Write Control
- Single 3.3 V + 10%, – 5% Operation
- LVTTL 3.3 V I/O ($V_{DDQ}$)
- Register to Latch Synchronous Operation
- Asynchronous Output Enable
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x18 or x36 organization
- MCM69L737A/819A–8.5 = 8.5 ns
  MCM69L737A/819A–9 = 9 ns
  MCM69L737A/819A–9.5 = 9.5 ns
- Sleep Mode Operation (ZZ Pin)
- 119 Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) Package

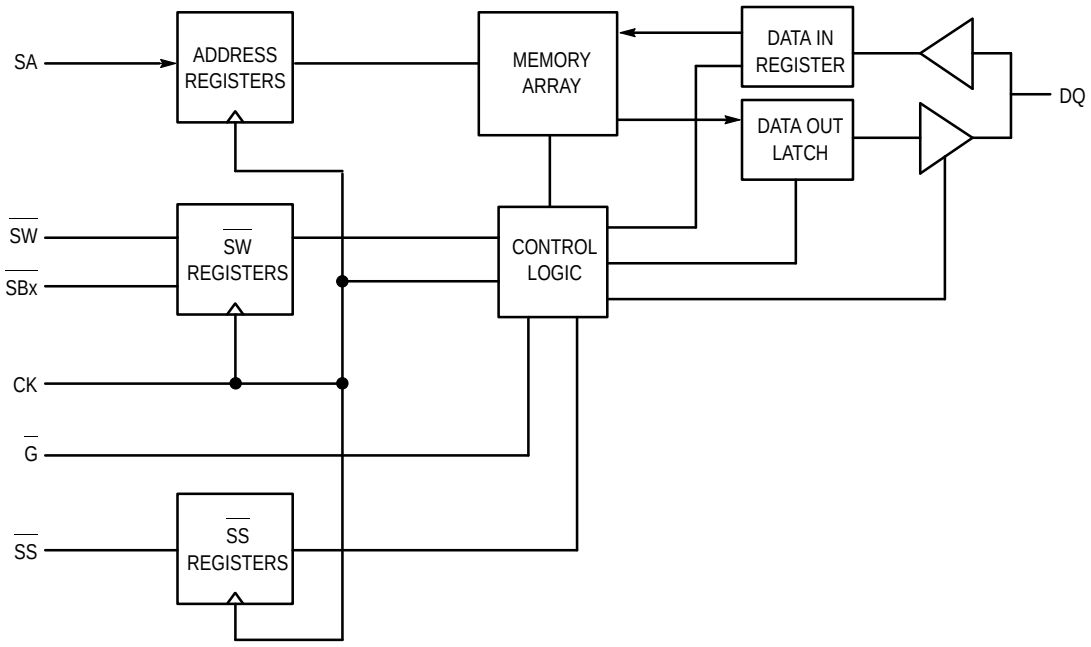
This document contains information on a new product. Specifications and information herein are subject to change without notice.

**REV 1**
**8/15/97**



MOTOROLA

## FUNCTIONAL BLOCK DIAGRAM




## PIN ASSIGNMENTS

### TOP VIEW

**MCM69L737A**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | SA | SA | NC | SA | SA | $V_{DDQ}$ |
| B | NC | NC | SA | NC | SA | NC | NC |
| C | NC | SA | SA | $V_{DD}$ | SA | SA | NC |
| D | DQc | DQc | $V_{SS}$ | NC | $V_{SS}$ | DQb | DQb |
| E | DQc | DQc | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | DQb | DQb |
| F | $V_{DDQ}$ | DQc | $V_{SS}$ | G | $V_{SS}$ | DQb | $V_{DDQ}$ |
| G | DQc | DQc | $\overline{SBc}$ | NC | $\overline{SBb}$ | DQb | DQb |
| H | DQc | DQc | $V_{SS}$ | NC | $V_{SS}$ | DQb | DQb |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | DQd | DQd | $V_{SS}$ | CK | $V_{SS}$ | DQa | DQa |
| L | DQd | DQd | $\overline{SBd}$ | CK | $\overline{SBa}$ | DQa | DQa |
| M | $V_{DDQ}$ | DQd | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | DQa | $V_{DDQ}$ |
| N | DQd | DQd | $V_{SS}$ | SA | $V_{SS}$ | DQa | DQa |
| P | DQd | DQd | $V_{SS}$ | SA | $V_{SS}$ | DQa | DQa |
| R | NC | SA | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | SA | NC |
| T | NC | NC | SA | SA | SA | NC | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**MCM69L819A**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | SA | SA | NC | SA | SA | $V_{DDQ}$ |
| B | NC | NC | SA | NC | SA | NC | NC |
| C | NC | SA | SA | $V_{DD}$ | SA | SA | NC |
| D | DQb | NC | $V_{SS}$ | NC | $V_{SS}$ | DQa | NC |
| E | NC | DQb | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | DQa |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | G | $V_{SS}$ | DQa | $V_{DDQ}$ |
| G | NC | DQb | $\overline{SBb}$ | NC | $V_{SS}$ | NC | DQa |
| H | DQb | NC | $V_{SS}$ | NC | $V_{SS}$ | DQa | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | DQb | $V_{SS}$ | CK | $V_{SS}$ | NC | DQa |
| L | DQb | NC | $V_{SS}$ | CK | $\overline{SBa}$ | DQa | NC |
| M | $V_{DDQ}$ | DQb | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | DQb | NC | $V_{SS}$ | SA | $V_{SS}$ | DQa | NC |
| P | NC | DQb | $V_{SS}$ | SA | $V_{SS}$ | NC | DQa |
| R | NC | SA | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | SA | NC |
| T | NC | SA | SA | NC | SA | SA | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**MCM69L737A PIN DESCRIPTIONS**

| PBGA Pin Locations | Symbol | Type | Description |
|---|---|---|---|
| 4K | CK | Input | Address, data in and control input register clock. Active high. |
| 4L | $\overline{CK}$ | Input | Address, data in and control input register clock. Active low. |
| (a) 6K, 7K, 6L, 7L, 6M, 6N, 7N, 6P, 7P<br>(b) 6D, 7D, 6E, 7E, 6F, 6G, 7G, 6H, 7H<br>(c) 1D, 2D, 1E, 2E, 2F, 1G, 2G, 1H, 2H<br>(d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P | DQx | I/O | Synchronous Data I/O. |
| 4F | $\overline{G}$ | Input | Output Enable: Asynchronous pin, active low. |
| 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C,<br>5C, 6C, 4N, 4P, 2R, 6R, 3T, 4T, 5T | SA | Input | Synchronous Address Inputs: Registered on the rising clock edge. |
| 5L, 5G, 3G, 3L<br>(a), (b), (c), (d) | $\overline{SBx}$ | Input | Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the SW input. Has no effect on read cycles, active low. |
| 4E | $\overline{SS}$ | Input | Synchronous Chip Enable: Registered on the rising clock edge, active low. |
| 4M | $\overline{SW}$ | Input | Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes. |
| 4U | TCK | Input | Test Clock (JTAG). |
| 3U | TDI | Input | Test Data In (JTAG). |
| 5U | TDO | Output | Test Data Out (JTAG). |
| 2U | TMS | Input | Test Mode Select (JTAG). |
| 7T | ZZ | Input | Enables sleep mode. |
| 4C, 2J, 4J, 6J, 4R, 3R | $V_{DD}$ | Supply | Core Power Supply. |
| 1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U | $V_{DDQ}$ | Supply | Output Power Supply: provides operating power for output buffers. |
| 3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H,<br>3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R | $V_{SS}$ | Supply | Ground. |
| 4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C, 4D, 4G,<br>4H, 3J, 5J, 1R, 7R, 1T, 2T, 6T, 6U | NC | — | No Connection: There is no connection to the chip.<br>Note: 3J and 5J are tied common. |

**MCM69L819A PIN DESCRIPTIONS**

| PBGA Pin Locations | Symbol | Type | Description |
|---|---|---|---|
| 4K | CK | Input | Address, data in and control input register clock. Active high. |
| 4L | $\overline{CK}$ | Input | Address, data in and control input register clock. Active low. |
| (a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P<br>(b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P | DQx | I/O | Synchronous Data I/O. |
| 4F | $\overline{G}$ | Input | Output Enable: Asynchronous pin, active low. |
| 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C,<br>6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T | SA | Input | Synchronous Address Inputs: Registered on the rising clock edge. |
| 5L, 3G<br>(a), (b) | $\overline{SBx}$ | Input | Synchronous Byte Write Enable: Enables writes to byte x in conjunction with the SW input. Has no effect on read cycles, active low. |
| 4E | $\overline{SS}$ | Input | Synchronous Chip Enable: Registered on the rising clock edge, active low. |
| 4M | $\overline{SW}$ | Input | Synchronous Write: Registered on the rising clock edge, active low. Writes all enabled bytes. |
| 4U | TCK | Input | Test Clock (JTAG). |
| 3U | TDI | Input | Test Data In (JTAG). |
| 5U | TDO | Output | Test Data Out (JTAG). |
| 2U | TMS | Input | Test Mode Select (JTAG). |
| 7T | ZZ | Input | Enables sleep mode. |
| 4C, 2J, 4J, 6J, 4R, 3R | $V_{DD}$ | Supply | Core Power Supply. |
| 1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U | $V_{DDQ}$ | Supply | Output Power Supply: provides operating power for output buffers. |
| 3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H,<br>3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P, 5R | $V_{SS}$ | Supply | Ground. |
| 4A, 1B, 2B, 4B, 6B, 7B, 1C, 7C,<br>2D, 4D, 7D, 1E, 6E, 2F, 1G, 4G, 6G,<br>2H, 4H, 7H, 3J, 5J, 1K, 6K, 2L, 7L, 6M, 2N,<br>7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U | NC | — | No Connection: There is no connection to the chip.<br>Note: 3J and 5J are tied common. |

**ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$, See Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | – 0.5 to + 4.6 | V |
| Output Supply Voltage | $V_{DDQ}$ | – 0.5 to $V_{DD}$ + 0.5 | V |
| Voltage On Any Pin | $V_{in}$ | – 0.5 to $V_{DD}$ + 0.5 | V |
| Input Current (per I/O) | $I_{in}$ | ± 50 | mA |
| Output Current (per I/O) | $I_{out}$ | ± 70 | mA |
| Power Dissipation (See Note 2) | $P_D$ | — | W |
| Operating Temperature | $T_A$ | 0 to + 70 | °C |
| Temperature Under Bias | $T_{bias}$ | – 10 to + 85 | °C |
| Storage Temperature | $T_{stg}$ | – 55 to + 125 | °C |

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

**PBGA PACKAGE THERMAL CHARACTERISTICS**

| Rating | | Symbol | Max | Unit | Notes |
|---|---|---|---|---|---|
| Junction to Ambient (Still Air) | | $R_{\theta JA}$ | 53 | °C/W | 1, 2 |
| Junction to Ambient (@200 ft/min) | Single Layer Board | $R_{\theta JA}$ | 38 | °C/W | 1, 2 |
| Junction to Ambient (@200 ft/min) | Four Layer Board | $R_{\theta JA}$ | 22 | °C/W | |
| Junction to Board (Bottom) | | $R_{\theta JB}$ | 14 | °C/W | 3 |
| Junction to Case (Top) | | $R_{\theta JC}$ | 5 | °C/W | 4 |

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC–883 Method 1012.1).

**CLOCK TRUTH TABLE**

| K CLK | ZZ | SS | SW | SBa | SBb | SBc | SBd | DQ (n) | DQ (n+1) | Mode |
|---|---|---|---|---|---|---|---|---|---|---|
| L – H | L | L | H | X | X | X | X | $D_{out}$ 0–35 | X | Read Cycle All Bytes |
| L – H | L | L | L | L | H | H | H | High–Z | $D_{in}$ 0–8 | Write Cycle 1st Byte |
| L – H | L | L | L | H | L | H | H | High–Z | $D_{in}$ 9–17 | Write Cycle 2nd Byte |
| L – H | L | L | L | H | H | L | H | High–Z | $D_{in}$ 18–26 | Write Cycle 3rd Byte |
| L – H | L | L | L | H | H | H | L | High–Z | $D_{in}$ 27–35 | Write Cycle 4th Byte |
| L – H | L | L | L | L | L | L | L | High–Z | $D_{in}$ 0–35 | Write Cycle All Bytes |
| L – H | L | L | L | H | H | H | H | High–Z | High–Z | Abort Write Cycle |
| L – H | L | H | X | X | X | X | X | High–Z | X | Deselect Cycle |
| X | H | X | X | X | X | X | X | High–Z | High–Z | Sleep Mode |

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS** (See Notes 1 through 4)

| Parameter | Symbol | Min | Typical –8.5 | Typical –9 | Typical –9.5 | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Core Power Supply Voltage | $V_{DD}$ | 3.15 | — | — | — | 3.6 | V | |
| Output Driver Supply Voltage | $V_{DDQ}$ | 3.15 | — | — | — | 3.6 | V | |
| Active Power Supply Current (x18)<br>(x36) | $I_{DD1}$ | —<br>— | 320<br>370 | 320<br>370 | 300<br>350 | 480<br>550 | mA | 5 |
| Quiescent Active Power Supply Current | $I_{DD2}$ | — | 180 | 180 | 180 | 250 | mA | 6, 10 |
| Active Standby Power Supply Current | $I_{SB1}$ | — | 170 | 170 | 170 | 250 | mA | 7 |
| Quiescent Standby Power Supply Current | $I_{SB2}$ | — | 150 | 150 | 150 | 230 | mA | 8, 10 |
| Sleep Mode Power Supply Current | $I_{SB3}$ | — | 30 | 30 | 30 | 50 | mA | 9, 10 |

NOTES:
1. All data sheet parameters specified to full range of $V_{DD}$ unless otherwise noted. All voltages are referenced to voltage applied to $V_{SS}$ bumps.
2. Supply voltage applied to $V_{DD}$ connections.
3. Supply voltage applied to $V_{DDQ}$ connections.
4. All power supply currents measured with outputs open or deselected.
5. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), SS registered active, 50% read cycles.
6. $V_{DD} = V_{DD}$ (max), $t_{KHKH}$ = dc, SS registered active.
7. $V_{DD} = V_{DD}$ (max), $t_{KHKH} = t_{KHKH}$ (min), SS registered inactive.
8. $V_{DD} = V_{DD}$ (max), $t_{KHKH}$ = dc, SS registered inactive, ZZ low.
9. $V_{DD} = V_{DD}$ (max), $t_{KHKH}$ = dc, SS registered inactive, ZZ high.
10. 200 mV ≥ $V_{in} \ge V_{DDQ}$ – 200 mV.

**DC INPUT CHARACTERISTICS**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| DC Input Logic High | $V_{IH}$ (dc) | 2.0 | $V_{DD}$ + 0.3 | V | |
| DC Input Logic Low | $V_{IL}$ (dc) | – 0.3 | 0.8 | V | 1 |
| Input Leakage Current | $I_{lkg}$ | — | ± 5 | µA | 2 |
| Clock Input Leakage Current | $I_{clkg}$ | — | ± 8 | µA | 2 |
| Clock Input Signal Voltage | $V_{in}$ | – 0.3 | $V_{DD}$ + 0.3 | V | |
| Clock Input Differential Voltage | $V_{DIF}$ (dc) | 0.2 | $V_{DD}$ + 0.6 | V | 3 |
| Clock Input Common Mode Voltage Range (See Figure 3) | $V_{CM}$ (dc) | 1.1 | 2.1 | V | 4 |

NOTES:
1. Inputs may undershoot to – 0.5 V (peak) for up to 20% $t_{KHKH}$ (e.g., 2 ns at a clock cycle time of 10 ns).
2. $0 V \le V_{in} \le V_{DDQ}$ for all pins.
3. Minimum instantaneous differential input voltage required for differential input clock operation.
4. Maximum rejectable common mode input voltage variation.

**DC OUTPUT CHARACTERISTICS**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output Leakage Current | $I_{lkg}$ | – 1.0 | 1.0 | µA | |
| Output Low Voltage | $V_{OL}$ | — | 0.4 | V | 1 |
| Output High Voltage | $V_{OH}$ | 2.4 | — | V | 2 |

NOTES:
1. $I_{OL}$ = 8.0 mA.
2. $I_{OH}$ = – 8.0 mA.

**CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, $0°C \le T_A \le 70°C$, Periodically Sampled Rather Than 100% Tested)

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | $C_{in}$ | 4 | 5 | pF |
| Input/Output Capacitance | $C_{I/O}$ | 7 | 8 | pF |
| CK, CK Capacitance | $C_{CK}$ | 4 | 5 | pF |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

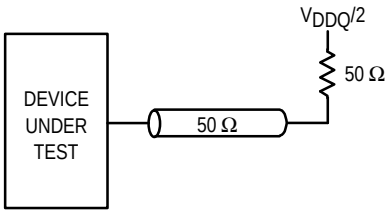
($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Reference Level . . . . . 1.5 V
Clock Input Timing Reference Level . . . . . Differential Cross–Point
Clock Input Pulse Level . . . . . 1.8 V to 2.1 V

**READ/WRITE CYCLE TIMING** (See Note 1)

| Parameter | Symbol | MCM69L737A–8.5 MCM69L819A–8.5 | | MCM69L737A–9 MCM69L819A–9 | | MCM69L737A–9.5 MCM69L819A–9.5 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Cycle Time | $t_{KHKH}$ | 8 | — | 8 | — | 9 | — | ns | |
| Clock High Pulse Width | $t_{KHKL}$ | 3.2 | — | 3.2 | — | 3.6 | — | ns | |
| Clock Low Pulse Width | $t_{KLKH}$ | 3.2 | — | 3.2 | — | 3.6 | — | ns | |
| Clock High to Output Valid | $t_{KHQV}$ | — | 8.5 | — | 9 | — | 9.5 | ns | |
| Clock Low to Output Valid | $t_{KLQV}$ | — | 3.5 | — | 3.5 | — | 4 | ns | |
| Clock Low to Output Hold | $t_{KLQX}$ | 0.5 | — | 0.5 | — | 0.5 | — | ns | 2 |
| Clock Low to Output Low–Z | $t_{KLQX1}$ | 1 | — | 1 | — | 1 | — | ns | 2, 3 |
| Clock High to Output High–Z | $t_{KHQZ}$ | 1 | 3.5 | 1 | 3.5 | 1 | 4 | ns | 2, 3 |
| Output Enable Low to Output Low–Z | $t_{GLQX}$ | 0.5 | — | 0.5 | — | 0.5 | — | ns | |
| Output Enable Low to Output Valid | $t_{GLQV}$ | — | 3.5 | — | 3.5 | — | 4 | ns | |
| Output Enable to Output Hold | $t_{GHQX}$ | 0.5 | — | 0.5 | — | 0.5 | — | ns | |
| Output Enable High to Output High–Z | $t_{GHQZ}$ | — | 3.5 | — | 3.5 | — | 4 | ns | 2, 3 |
| Setup Times: Address<br>Data In<br>Chip Select<br>Write Enable | $t_{AVKH}$<br>$t_{DVKH}$<br>$t_{SVKH}$<br>$t_{WVKH}$ | 0.5 | — | 0.5 | — | 0.5 | — | ns | |
| Hold Times: Address<br>Data In<br>Chip Select<br>Write Enable | $t_{KHAX}$<br>$t_{KHDX}$<br>$t_{KHSX}$<br>$t_{KHWX}$ | 1 | — | 1 | — | 1 | — | ns | |

NOTES:
1. In no case may control input signals (e.g., $\overline{SS}$) be operated with pulse widths less than the minimum clock input pulse width specifications (e.g., $t_{KHKL}$) or at frequencies that exceed the applied K clock frequency.
2. This parameter is sampled, and not 100% tested.
3. Measured at ± 200 mV from steady state.




## TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**Figure 1. AC Test Load**

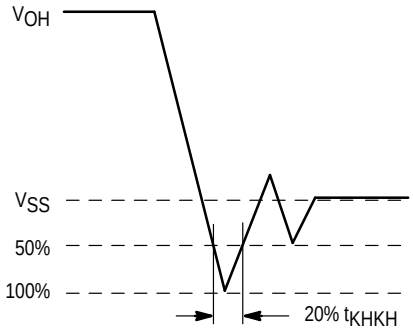
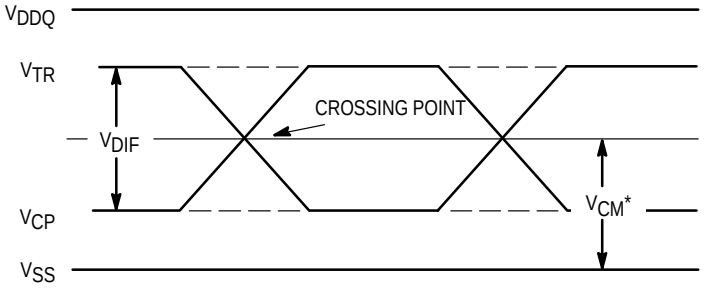


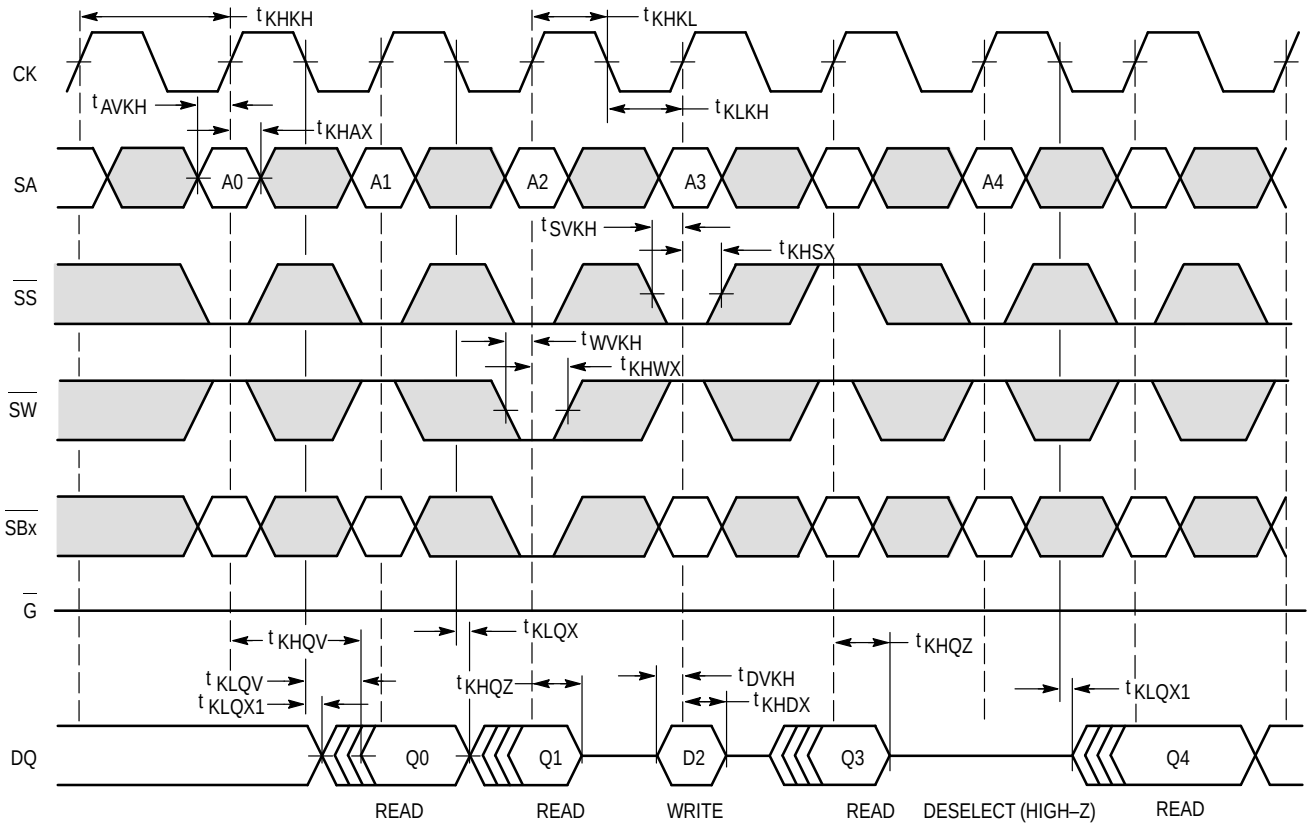

**Figure 2. Undershoot Voltage**



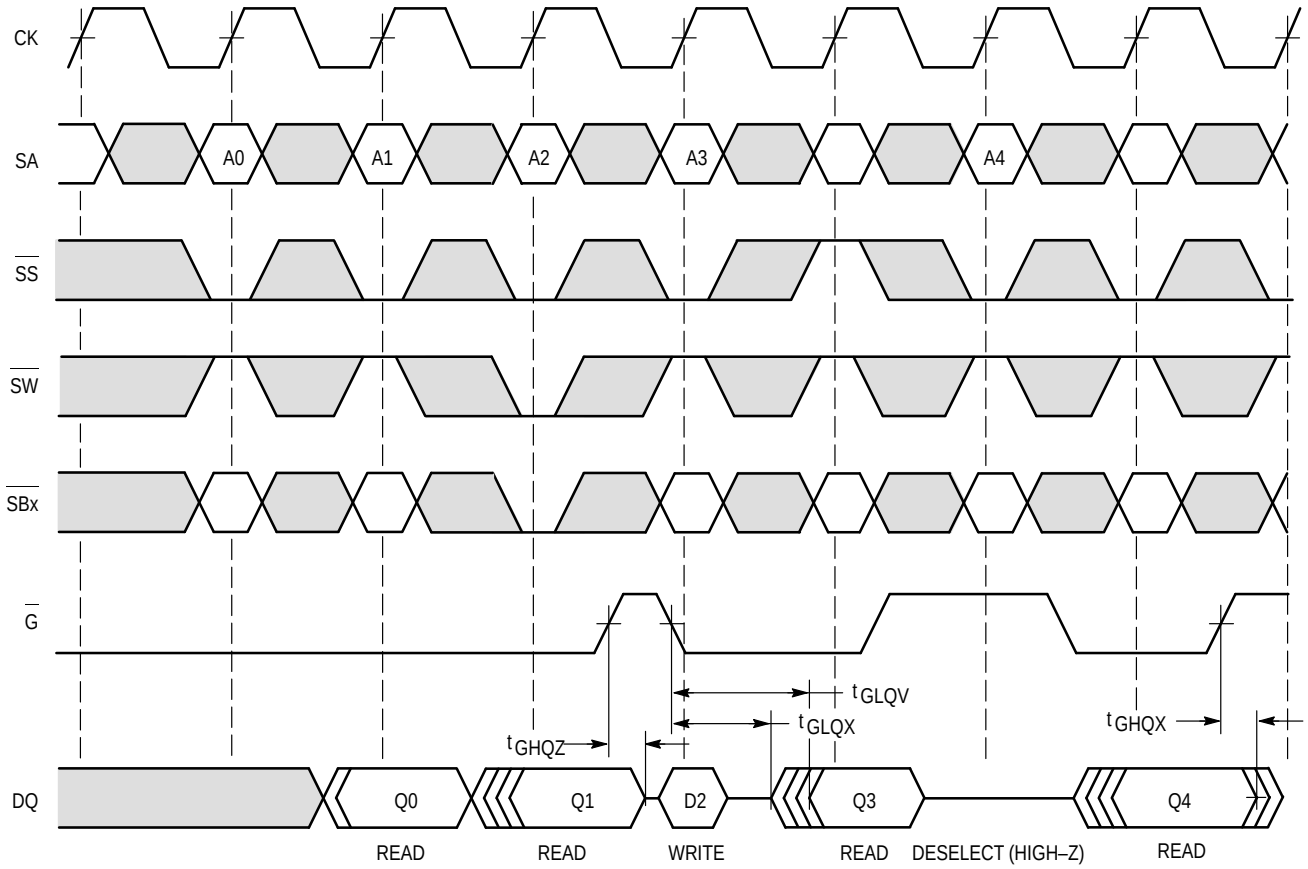

*$V_{CM}$, the Common Mode Input Voltage, equals $V_{TR} – ((V_{TR} – V_{CP})/2)$.

**Figure 3. Differential Inputs/Common Mode Input Voltage**

## REGISTER LATCH READ–WRITE–READ CYCLES



**REGISTER LATCH READ–WRITE–READ CYCLES**
**(G Controlled)**



## FUNCTIONAL OPERATION

### READ AND WRITE OPERATIONS

All control signals except $\overline{G}$ are registered on the rising edge of the CK clock. These signals must meet the setup and hold times shown in the AC Characteristics table. On the falling edge of the current cycle, the output latch becomes transparent and data is available. The output data is latched on the rising edge of the next clock. The output data is available at the output at $t_{KLQV}$ or $t_{KHQV}$ whichever is later. $t_{KHQV}$ is the internal latency of the device. During this same cycle a new read address can be applied to the address pins.

A write cycle can occur on the next cycle as long as $t_{KHQZ}$ and $t_{DVKH}$ are met. Read cycles may follow write cycles immediately.

G, SS, and SW control output drive. Chip deselect via a high on SS at the rising edge of the CK clock has its effect on the output drivers immediately. SW low deselects the output drivers immediately (on the same cycle). Output selecting via a low on SS and high on SW at a rising CK clock has its effect on the output drivers at $t_{KLQX}$. Output drive is also controlled directly by output enable, G. G is an asynchronous input. No clock edges are required to enable or disable the output with G.

Output data will be valid the latter of $t_{GLQV}$, $t_{KHQV}$, or $t_{KLQV}$. Outputs will begin driving at $t_{KLQX1}$. Outputs will hold previous data until $t_{KLQX}$, $t_{GHQX}$ or $t_{KHQZ}$ in the case of a write following a read.

### WRITE AND BYTE WRITE FUNCTIONS

Note that in the following discussion the term “byte” refers to nine bits of the RAM I/O bus. In all cases, the timing parameters described for synchronous write input (SW) apply to each of the byte write enable inputs (SBa, SBb, etc.).

Byte write enable inputs have no effect on read cycles. This allows the system designer not interested in performing byte writes to connect the byte enable inputs to active low ($V_{SS}$). Reads of all bytes proceed normally and write cycles, activated via a low on SW, and the rising edge of the CK clock, write the entire RAM I/O width. This way the designer is spared having to drive multiple write input buffer loads.

Byte writes are performed using the byte write enable inputs in conjunction with the synchronous write input (SW). It is important to note that writing any one byte will inhibit a read of all bytes at the current address. The RAM cannot simultaneously read one byte and write another at the same address. A write cycle initiated with none of the byte write enable inputs active is neither a read or a write. No write will occur, but the outputs will be deselected as in a normal write cycle.

### LATE WRITE

The write address is sampled on the first rising edge of clock and write data is sampled on the following rising edge.

The late write feature is implemented with single stage write buffering. Write buffering is transparent to the user. A comparator monitors the address bus and, when necessary, routes buffer contents to the outputs to assure coherent operation. This occurs in all cases whether there is a byte write or a full word is written.

### POWER UP AND INITIALIZATION

The following supply voltage application sequence is recommended: $V_{SS}$, $V_{DD}$, then $V_{DDQ}$. Please note, per the Absolute Maximum Ratings table, $V_{DDQ}$ is not to exceed $V_{DD}$ + 0.5 V, whatever the instantaneous value of $V_{DD}$. Once supplies have reached specification levels, a minimum dwell of 1.0 ms with C/K clock inputs cycling is required before beginning normal operations.

## SERIAL BOUNDARY SCAN TEST ACCESS PORT OPERATION

### OVERVIEW

The serial boundary scan test access port (TAP) on this RAM is designed to operate in a manner consistent with IEEE Standard 1149.1–1990 (commonly referred to as JTAG), but does not implement all of the functions required for 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the RAMs critical speed path. Nevertheless, the RAM supports the standard TAP controller architecture. (The TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with Standard 1149.1 compliant TAPs. The TAP operates using conventional JEDEC Standard 8–1B Low Voltage (3.3 V) TTL/CMOS logic level signaling.

### DISABLING THE TEST ACCESS PORT

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to $V_{SS}$ to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to $V_{DD}$ through a 1 k resistor. TDO should be left unconnected.

### TAP DC OPERATING CHARACTERISTICS

($0°C \le T_A \le 70°C$, Unless Otherwise Noted)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Logic Input Logic High | $V_{IH}1$ | 2.0 | $V_{DD}$ + 0.3 | V | |
| Logic Input Logic Low | $V_{IL}1$ | – 0.3 | 0.8 | V | |
| Logic Input Leakage Current | $I_{lkg}$ | — | ± 5 | µA | 1 |
| CMOS Output Logic Low | $V_{OL}1$ | — | 0.2 | V | 2 |
| CMOS Output Logic High | $V_{OH}1$ | $V_{DD}$ – 0.2 | — | V | 3 |
| TTL Output Logic Low | $V_{OL}2$ | — | 0.4 | V | 4 |
| TTL Output Logic High | $V_{OH}2$ | 2.4 | — | V | 5 |

NOTES:
1. $0 V \le V_{in} \le V_{DDQ}$ for all logic input pins.
2. $I_{OL}1 \le 100$ µA. Sampled, not 100% tested.
3. $|I_{OH}1| \le 100$ µA. Sampled, not 100% tested.
4. $I_{OL}2 \le 8$ mA.
5. $|I_{OH}2| \le 8$ mA.

## TAP AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ $T_A$ ≤ 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20% to 80%)
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Reference Level . . . . . 1.5 V

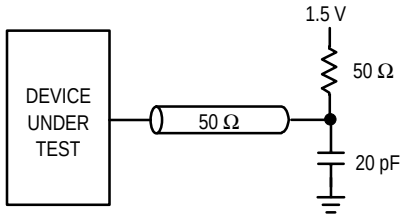
Output Test Load . . . . . 50 Ω Parallel Terminated T–line with 20 pF Receiver Input Capacitance
Test Load Termination Supply Voltage ($V_T$) . . . . . 1.5 V

### TAP CONTROLLER TIMING

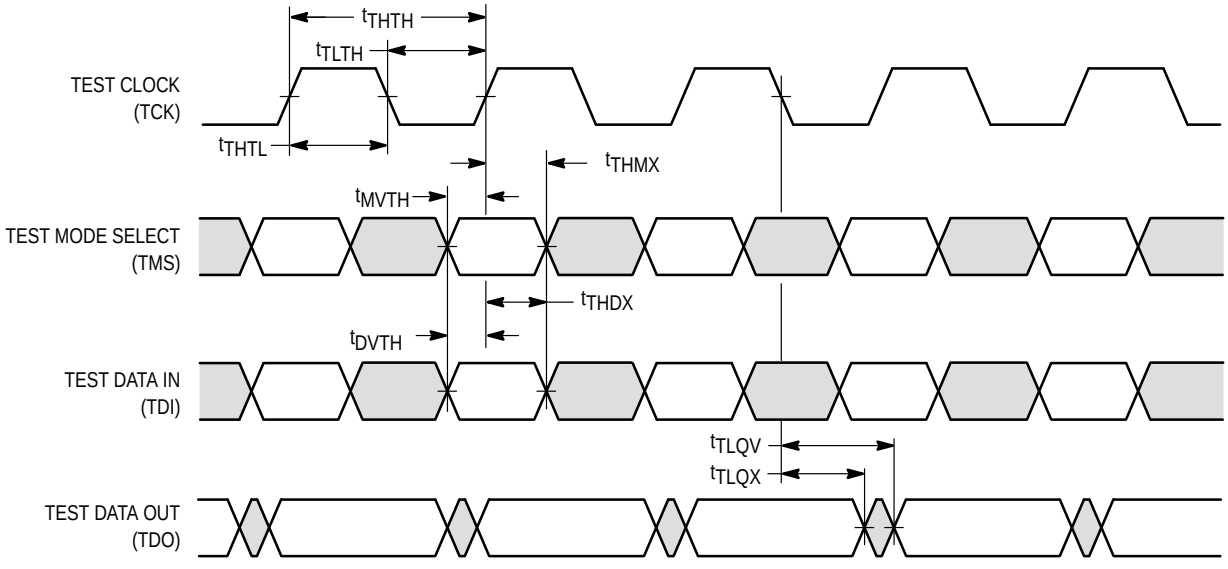
| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Cycle Time | $t_{THTH}$ | 100 | — | ns | |
| Clock High Time | $t_{THTL}$ | 40 | — | ns | |
| Clock Low Time | $t_{TLTH}$ | 40 | — | ns | |
| TMS Setup | $t_{MVTH}$ | 10 | — | ns | |
| TMS Hold | $t_{THMX}$ | 10 | — | ns | |
| TDI Valid to TCK High | $t_{DVTH}$ | 10 | — | ns | |
| TCK High to TDI Don't Care | $t_{THDX}$ | 10 | — | ns | |
| Capture Setup | $t_{CS}$ | 10 | — | ns | 1 |
| Capture Hold | $t_{CH}$ | 10 | — | ns | 1 |
| TCK Low to TDO Unknown | $t_{TLQX}$ | 0 | — | ns | |
| TCK Low to TDO Valid | $t_{TLOV}$ | — | 20 | ns | |

NOTES:
1. $t_{CS}$ + $t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure accurate pad data capture.

### AC TEST LOAD




### TAP CONTROLLER TIMING DIAGRAM



## TEST ACCESS PORT PINS

### TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

### TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.

### TDI — TEST DATA IN (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to Figure 5, TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.

### TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (refer to Figure 5, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

### TRST — TAP RESET

This device does not have a TRST pin. TRST is optional in **IEEE 1149.1.** The test–logic reset state is entered while TMS is held high for five rising edges of TCK. Power on reset circuitry is included internally. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

## TEST ACCESS PORT REGISTERS

### OVERVIEW

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected it is “placed” between the TDI and TDO pins.

### INSTRUCTION REGISTER

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power–up or whenever the controller is placed in test–logic–reset state.

### BYPASS REGISTER

The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.

### BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input and I/O connections on the RAM (not counting the TAP pins). This also includes a number of place holder locations (always set to a logic 1) reserved for density upgrade address pins. There are a total of 70 bits in the case of the x36 device and 51 bits in the case of the x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bump/Bit Scan Order tables describe which device bump connects to each boundary scan register location. The first column defines the bit’s position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

### IDENTIFICATION (ID) REGISTER

The ID Register is a 32–bit register that is loaded with a device and vendor specific 32–bit code when the controller is put in capture–DR state with the IDCODE command loaded in the instruction register. The code is loaded from a 32–bit on–chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into shift–DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

**ID Register Presence Indicator**

| Bit No. | 0 |
|---|---|
| Value | 1 |

**Motorola JEDEC ID Code (Compressed Format, per IEEE Standard 1149.1 – 1990**

| Bit No. | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

**Reserved For Future Use**

| Bit No. | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|
| Value | x | x | x | x | x | x |

**Device Width**

| Configuration | Bit No. | 22 | 21 | 20 | 19 | 18 |
|---|---|---|---|---|---|---|
| 128K x 36 | Value | 0 | 0 | 1 | 0 | 0 |
| 256K x 18 | Value | 0 | 0 | 0 | 1 | 1 |

**Device Depth**

| Configuration | Bit No. | 27 | 26 | 25 | 24 | 23 |
|---|---|---|---|---|---|---|
| 128K x 36 | Value | 0 | 0 | 1 | 0 | 1 |
| 256K x 18 | Value | 0 | 0 | 1 | 1 | 0 |

**Revision Number**

| Bit No. | 31 | 30 | 29 | 28 |
|---|---|---|---|---|
| Value | x | x | x | x |

**Figure 4. ID Register Bit Meanings**

**MCM69L737A Bump/Bit Scan Order**

| Bit No. | Signal Name | Bump ID | | Bit No. | Signal Name | Bump ID |
|---|---|---|---|---|---|---|
| 1 | M2 | 5R | | 36 | SA | 3B |
| 2 | SA | 4P | | 37 | NC | 2B |
| 3 | SA | 4T | | 38 | SA | 3A |
| 4 | SA | 6R | | 39 | SA | 3C |
| 5 | SA | 5T | | 40 | SA | 2C |
| 6 | ZZ | 7T | | 41 | SA | 2A |
| 7 | DQa | 6P | | 42 | DQc | 2D |
| 8 | DQa | 7P | | 43 | DQc | 1D |
| 9 | DQa | 6N | | 44 | DQc | 2E |
| 10 | DQa | 7N | | 45 | DQc | 1E |
| 11 | DQa | 6M | | 46 | DQc | 2F |
| 12 | DQa | 6L | | 47 | DQc | 2G |
| 13 | DQa | 7L | | 48 | DQc | 1G |
| 14 | DQa | 6K | | 49 | DQc | 2H |
| 15 | DQa | 7K | | 50 | DQc | 1H |
| 16 | $\overline{\text{SBa}}$ | 5L | | 51 | $\overline{\text{SBc}}$ | 3G |
| 17 | $\overline{\text{CK}}$ | 4L | | 52 | NC | 4D |
| 18 | CK | 4K | | 53 | $\overline{\text{SS}}$ | 4E |
| 19 | $\overline{\text{G}}$ | 4F | | 54 | NC | 4G |
| 20 | $\overline{\text{SBb}}$ | 5G | | 55 | NC | 4H |
| 21 | DQb | 7H | | 56 | $\overline{\text{SW}}$ | 4M |
| 22 | DQb | 6H | | 57 | $\overline{\text{SBd}}$ | 3L |
| 23 | DQb | 7G | | 58 | DQd | 1K |
| 24 | DQb | 6G | | 59 | DQd | 2K |
| 25 | DQb | 6F | | 60 | DQd | 1L |
| 26 | DQb | 7E | | 61 | DQd | 2L |
| 27 | DQb | 6E | | 62 | DQd | 2M |
| 28 | DQb | 7D | | 63 | DQd | 1N |
| 29 | DQb | 6D | | 64 | DQd | 2N |
| 30 | SA | 6A | | 65 | DQd | 1P |
| 31 | SA | 6C | | 66 | DQd | 2P |
| 32 | SA | 5C | | 67 | SA | 3T |
| 33 | SA | 5A | | 68 | SA | 2R |
| 34 | NC | 6B | | 69 | SA | 4N |
| 35 | SA | 5B | | 70 | M1 | 3R |

**MCM69L819A Bump/Bit Scan Order**

| Bit No. | Signal Name | Bump ID | | Bit No. | Signal Name | Bump ID |
|---|---|---|---|---|---|---|
| 1 | M2 | 5R | | 36 | SBb | 3G |
| 2 | SA | 6T | | 37 | NC | 4D |
| 3 | SA | 4P | | 38 | SS | 4E |
| 4 | SA | 6R | | 39 | NC | 4G |
| 5 | SA | 5T | | 40 | NC | 4H |
| 6 | ZZ | 7T | | 41 | SW | 4M |
| 7 | DQa | 7P | | 42 | DQb | 2K |
| 8 | DQa | 6N | | 43 | DQb | 1L |
| 9 | DQa | 6L | | 44 | DQb | 2M |
| 10 | DQa | 7K | | 45 | DQb | 1N |
| 11 | $\overline{\text{SBa}}$ | 5L | | 46 | DQb | 2P |
| 12 | $\overline{\text{CK}}$ | 4L | | 47 | SA | 3T |
| 13 | CK | 4K | | 48 | SA | 2R |
| 14 | $\overline{\text{G}}$ | 4F | | 49 | SA | 4N |
| 15 | DQa | 6H | | 50 | SA | 2T |
| 16 | DQa | 7G | | 51 | M1 | 3R |
| 17 | DQa | 6F | | | | |
| 18 | DQa | 7E | | | | |
| 19 | DQa | 6D | | | | |
| 20 | SA | 6A | | | | |
| 21 | SA | 6C | | | | |
| 22 | SA | 5C | | | | |
| 23 | SA | 5A | | | | |
| 24 | NC | 6B | | | | |
| 25 | SA | 5B | | | | |
| 26 | SA | 3B | | | | |
| 27 | NC | 2B | | | | |
| 28 | SA | 3A | | | | |
| 29 | SA | 3C | | | | |
| 30 | SA | 2C | | | | |
| 31 | SA | 2A | | | | |
| 32 | DQb | 1D | | | | |
| 33 | DQb | 2E | | | | |
| 34 | DQb | 2G | | | | |
| 35 | DQb | 1H | | | | |

NOTES:

1. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “place holder” bit that is forced to logic 1. These pads are reserved for use as address inputs on higher density RAMs that follow this pad out and scan order standard.
2. In scan mode, differential inputs CK and $\overline{\text{CK}}$ are referenced to each other and must be at opposite logic levels for reliable operation.
3. M1 and M2 are not ordinary inputs and may not respond to standard I/O logic levels. M1 and M2 must be driven to within 100 mV of a $V_{DD}$ or $V_{SS}$ supply rail to ensure consistent results.
4. ZZ must remain at $V_{IL}$ during boundary scan to ensure consistent results.

## TAP CONTROLLER INSTRUCTION SET

### OVERVIEW

There are two classes of instructions defined in Standard 1149.1–1990; the standard (public) instructions, and device specific (private) instructions. Some public instructions, are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the RAM or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in capture–IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the shift–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to update–IR state. The TAP instruction sets for this device are listed in the following tables.

## STANDARD (PUBLIC) INSTRUCTIONS

### BYPASS

The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift–DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction register, moving the TAP controller into the capture–DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time ($t_{CS}$ plus $t_{CH}$). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

Moving the controller to shift–DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the update–DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the pause–DR command. This functionality is not IEEE 1149.1 compliant.

### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore, this device is not IEEE 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE/PRELOAD instruction described above, except the RAM outputs are forced to High–Z any time the instruction is loaded.

### IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture–DR mode and places the ID register between the TDI and TDO pins in shift–DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test–logic–reset state.

## DEVICE SPECIFIC (PUBLIC) INSTRUCTION

### SAMPLE–Z

If the SAMPLE–Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (High–Z) and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift–DR state.

## DEVICE SPECIFIC (PRIVATE) INSTRUCTION

### NOOP

Do not use these instructions; they are reserved for future use.

**STANDARD (PUBLIC) INSTRUCTION CODES**

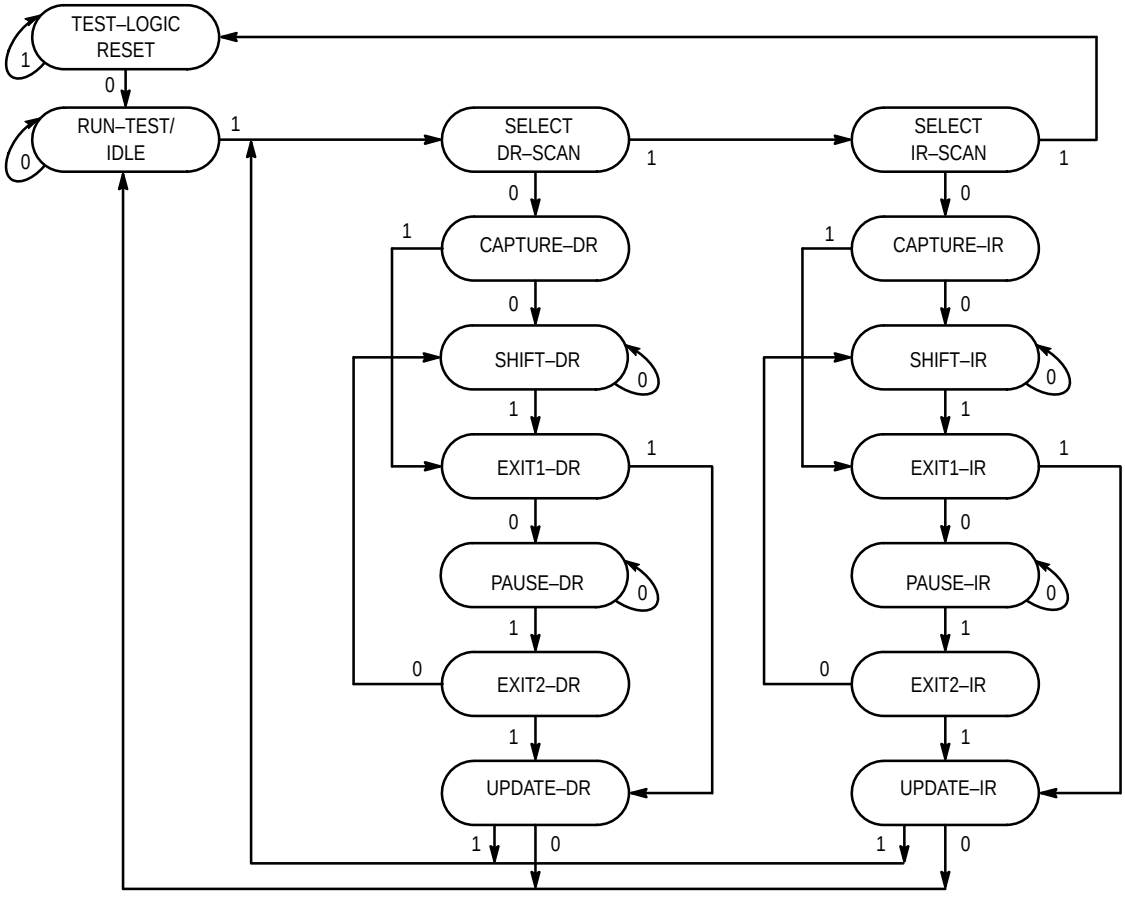
| Instruction | Code* | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM outputs to High–Z state. **NOT IEEE 1149.1 COMPLIANT.** |
| IDCODE | 001** | Preloads ID register and places it between TDI and TDO. Does not affect RAM operation. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect RAM operation. Does not implement IEEE 1149.1 PRELOAD function. **NOT IEEE 1149.1 COMPLIANT.** |
| BYPASS | 111 | Places bypass register between TDI and TDO. Does not affect RAM operation. |
| SAMPLE–Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all RAM output drivers to High–Z state. |

* Instruction codes expressed in binary, MSB on left, LSB on right.
** Default instruction automatically loaded at power–up and in test–logic–reset state.

**STANDARD (PRIVATE) INSTRUCTION CODES**

| Instruction | Code* | Description |
|---|---|---|
| NO OP | 011 | Do not use these instructions; they are reserved for future use. |
| NO OP | 101 | Do not use these instructions; they are reserved for future use. |
| NO OP | 110 | Do not use these instructions; they are reserved for future use. |

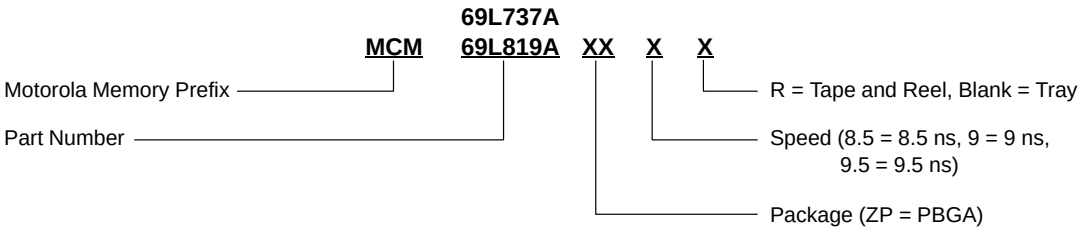
* Instruction codes expressed in binary, MSB on left, LSB on right.




NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

**Figure 5. TAP Controller State Diagram**

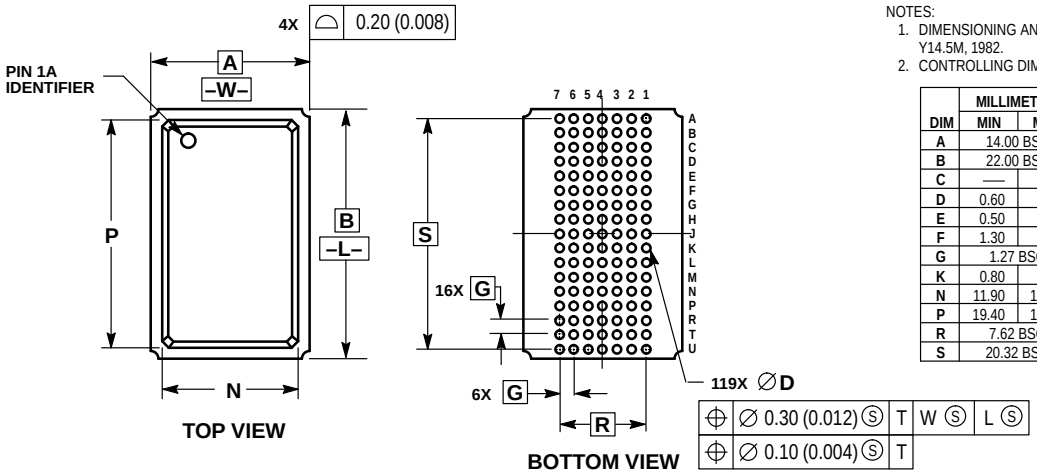
## ORDERING INFORMATION
**(Order by Full Part Number)**

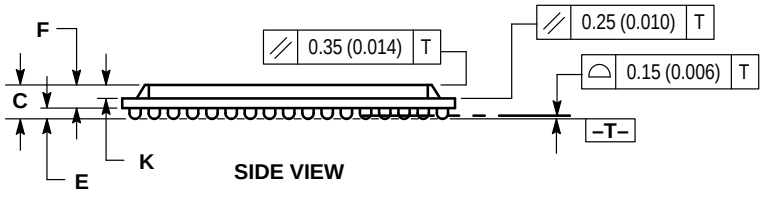



| | | | |
|---|---|---|---|
| Full Part Numbers — | MCM69L737AZP8.5 | MCM69L737AZP9 | MCM69L737AZP9.5 |
| | MCM69L819AZP8.5 | MCM69L819AZP9 | MCM69L819AZP9.5 |
| | MCM69L737AZP8.5R | MCM69L737AZP9R | MCM69L737AZP9.5R |
| | MCM69L819AZP8.5R | MCM69L819AZP9R | MCM69L819AZP9.5R |

## PACKAGE DIMENSIONS

**ZP PACKAGE**
**7 X 17 BUMP PBGA**
**CASE 999–01**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 14.00 BSC | | 0.551 BSC | |
| B | 22.00 BSC | | 0.866 BSC | |
| C | — | 2.40 | — | 0.094 |
| D | 0.60 | 0.90 | 0.024 | 0.035 |
| E | 0.50 | 0.70 | 0.020 | 0.028 |
| F | 1.30 | 1.70 | 0.051 | 0.067 |
| G | 1.27 BSC | | 0.050 BSC | |
| K | 0.80 | 1.00 | 0.031 | 0.039 |
| N | 11.90 | 12.10 | 0.469 | 0.476 |
| P | 19.40 | 19.60 | 0.764 | 0.772 |
| R | 7.62 BSC | | 0.300 BSC | |
| S | 20.32 BSC | | 0.800 BSC | |

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