

The RF Line

2.1-2.2 GHz SiFET

RF Integrated Power Amplifier

The MHVIC2115R2 is a 26 Volt integrated power amplifier designed for driver and output stage W-CDMA applications. The device is a three-stage amplifier with input matching using Motorola's high voltage LDMOS IC process. The device is packaged in a PFP-16 power flat pack package that provides excellent thermal performance through a solderable backside contact.

Driver Application

- Typical W-CDMA Performance: -53 dBc ACPR, 2.1-2.2 GHz, 26 Volts, $I_{DQ1} = 96$ mA, $I_{DQ2} = 204$ mA, $I_{DQ3} = 111$ mA, 3GPP Test Model 1, Measured in a 3.84 MHz BW @ 5 MHz offset, 64 DTCH
Output Power — 23 dBm
Power Gain — 34 dB

- Gain Flatness = 0.3 dB from 2.1-2.17 GHz

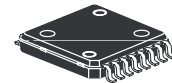
Output Application

- Typical W-CDMA Performance: -45 dBc ACPR, 2.1-2.2 GHz, 27 Volts, $I_{DQ1} = 56$ mA, $I_{DQ2} = 61$ mA, $I_{DQ3} = 117$ mA, 3GPP Test Model 1, Measured in a 1.0 MHz BW @ 4 MHz offset, 64 DTCH
Output Power — 34 dBm
Power Gain — 30 dB
PAE = 16%

- P1dB = 15 Watts, Gain Flatness = 0.2 dB from 2.1 to 2.2 GHz
- On-Chip Input Matching to 50 Ohms Impedance
- High Gain and High Linearity
- Integrated ESD Protection
- Temperature Compensation Capability
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC2115R2

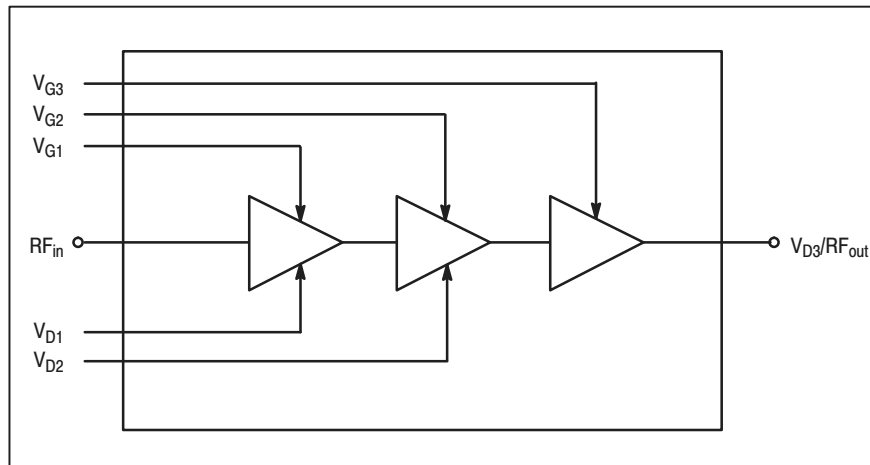
2.2 GHz, 26 V, 23/34 dBm
W-CDMA
RF LDMOS INTEGRATED CIRCUIT



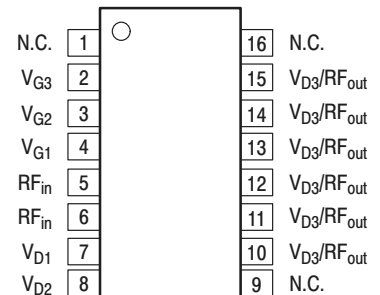
CASE 978-03
PFP-16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C



PIN CONNECTIONS



(Top View)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		$^{\circ}\text{C/W}$
Driver Application ($P_{out} = +0.2 \text{ W CW}$)	Stage 1, 26 Vdc, $I_{DQ} = 96 \text{ mA}$ Stage 2, 26 Vdc, $I_{DQ} = 204 \text{ mA}$ Stage 3, 26 Vdc, $I_{DQ} = 111 \text{ mA}$	3.5	
Output Application ($P_{out} = +2.5 \text{ W CW}$)	Stage 1, 27 Vdc, $I_{DQ} = 56 \text{ mA}$ Stage 2, 27 Vdc, $I_{DQ} = 61 \text{ mA}$ Stage 3, 27 Vdc, $I_{DQ} = 117 \text{ mA}$	2.7	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

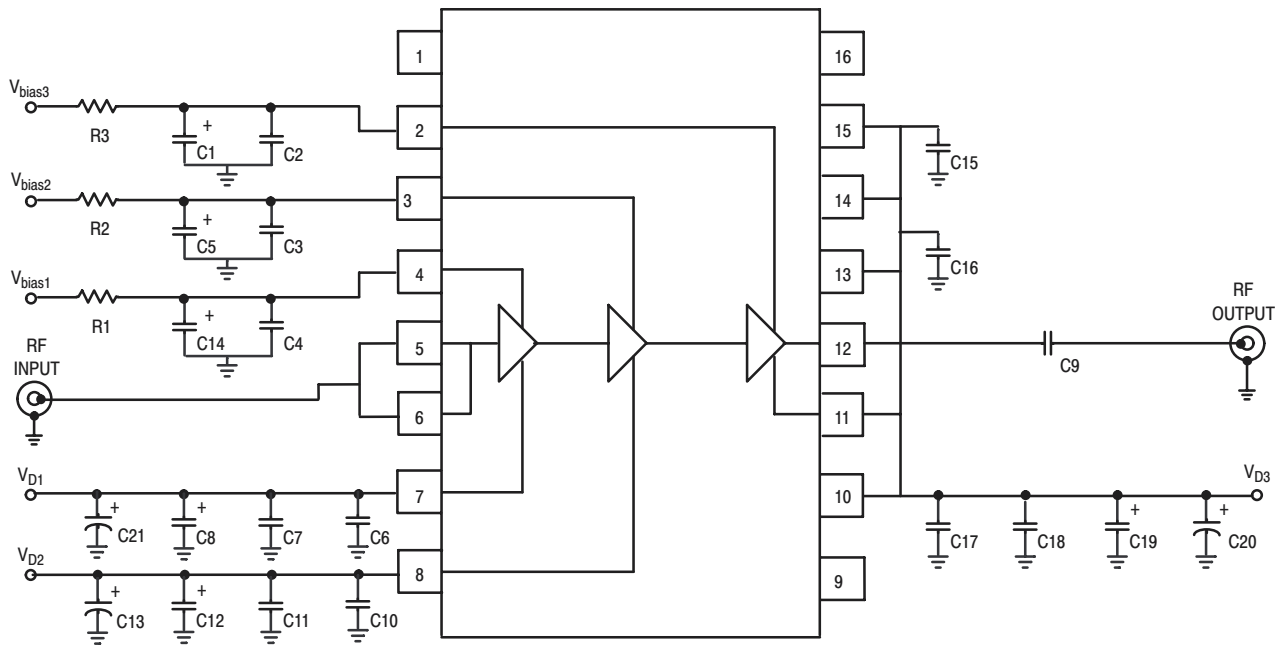
ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$, 50 ohm system unless otherwise noted)

W-CDMA CHARACTERISTICS (In Motorola Test Fixture) $V_{DS} = 26 \text{ V}$, $I_{DQ1} = 96 \text{ mA}$, $I_{DQ2} = 204 \text{ mA}$, $I_{DQ3} = 111 \text{ mA}$, 2.11–2.17 GHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ $P_{out} = 23 \text{ dBm}$	G_{ps}	31	34	—	dB
Gain Flatness @ $P_{out} = 23 \text{ dBm}$	G_F	—	0.3	0.5	dB
Input Return Loss @ $P_{out} = 23 \text{ dBm}$	IRL	—	-12	-10	dB
Group Delay	—	—	1.7	—	ns
Phase Linearity	—	—	0.2	—	$^{\circ}$
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 23 \text{ dBm}$, 5 MHz Offset	ACPR	—	-53	-50	dBc
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 28 \text{ dBm}$, 5 MHz Offset	ACPR	—	-50	—	dBc

W-CDMA CHARACTERISTICS (In Motorola Test Fixture) $V_{DS} = 27 \text{ V}$, $I_{DQ1} = 56 \text{ mA}$, $I_{DQ2} = 61 \text{ mA}$, $I_{DQ3} = 117 \text{ mA}$, 2.1–2.2 GHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ $P_{out} = 34 \text{ dBm}$	G_{ps}	—	30	—	dB
Gain Flatness @ $P_{out} = 34 \text{ dBm}$	G_F	—	0.2	—	dB
Input Return Loss @ $P_{out} = 34 \text{ dBm}$	IRL	—	-12	—	dB
Power Added Efficiency @ $P_{out} = 34 \text{ dBm}$	PAE	—	16	—	%
1-Carrier W-CDMA Conditions: Adjacent Channel Power Ratio @ $P_{out} = 34 \text{ dBm}$, 4 MHz Offset	ACPR	—	-45	—	dBc



- | | | | |
|---------------------------|---|---------------|---|
| C1, C5, C8, C12, C14, C19 | 1 μ F SMT Tantalum Chip Capacitors | C13, C20, C21 | 330 μ F Electrolytic Capacitors (MCR35V337M10X16) |
| C2, C3, C4, C7, C11, C18 | 0.01 μ F Chip Capacitors (0805C103K5RACTR) | R1, R2, R3 | 1 k Ω Chip Resistors (0805) |
| C6, C10, C17 | 6.8 pF Chip Capacitors, ACCU-P (AVX 08051J6R8BBT) | PCB | Arlon, 20 mils, $\epsilon_r = 2.55$ |
| C9, C15, C16 | 1.8 pF Chip Capacitors, ACCU-P (AVX 08051J1R8BBT) | | |

Figure 1. 2.2 GHz Demo Board Schematic

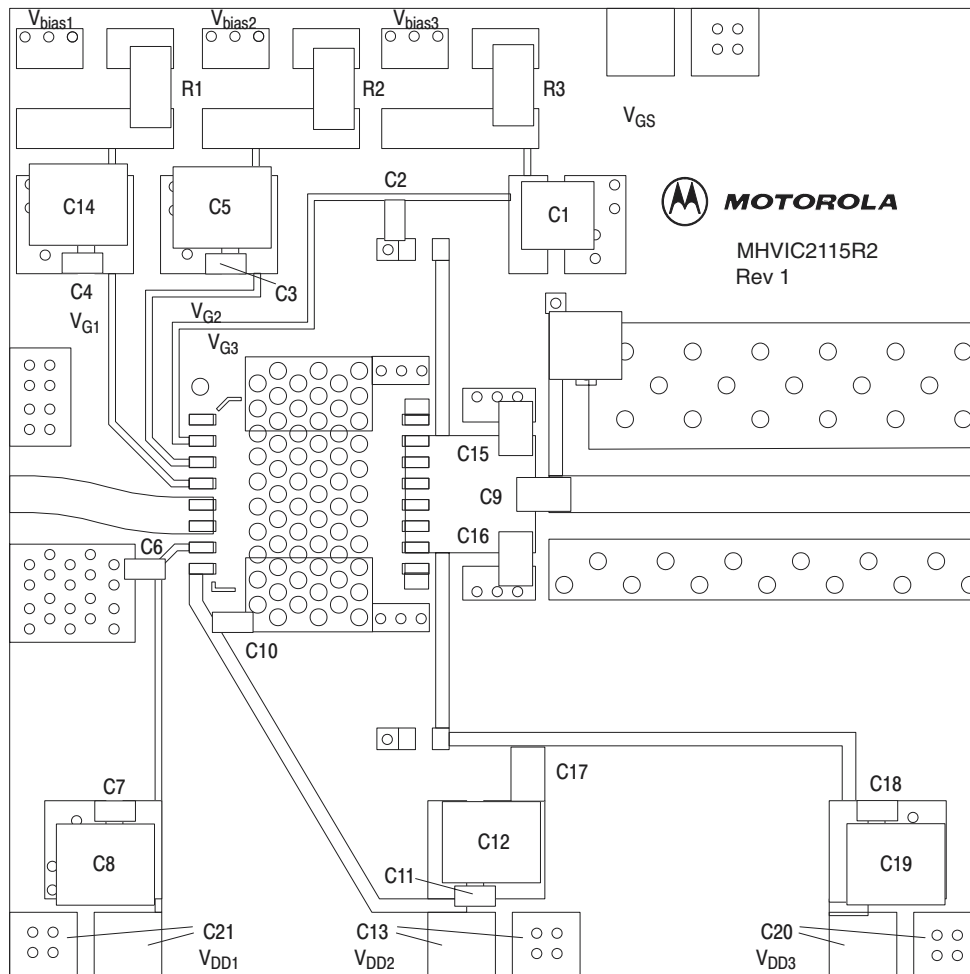


Figure 2. 2.2 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

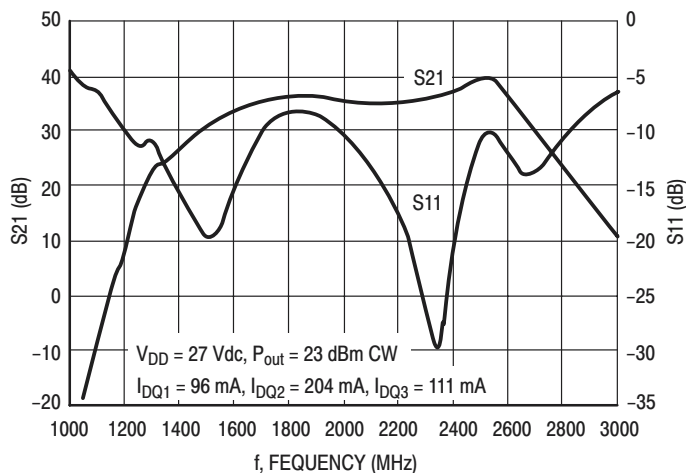


Figure 3. Broadband Frequency Response

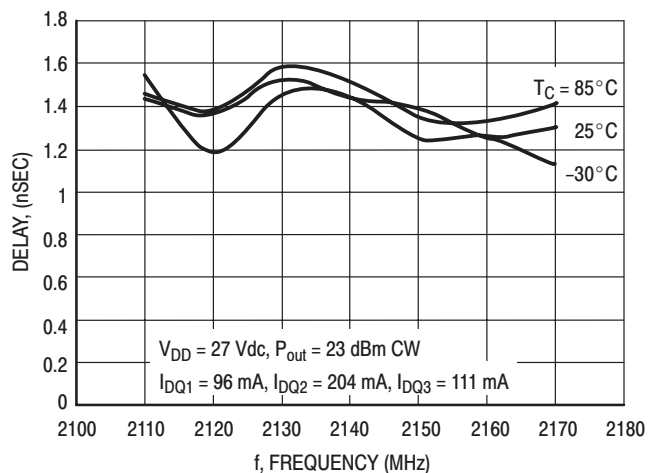


Figure 4. Delay versus Frequency

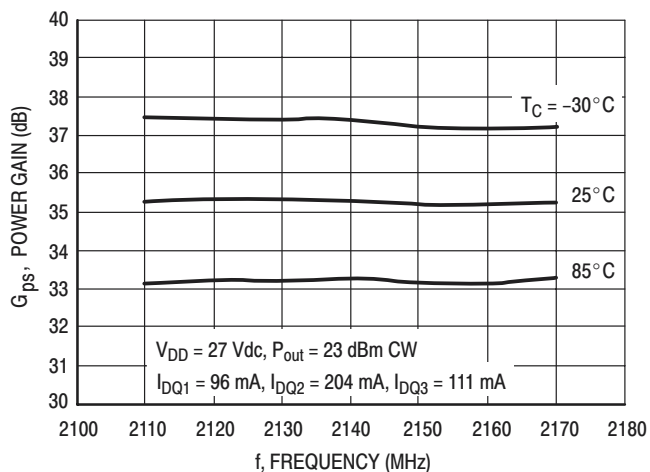


Figure 5. Power Gain versus Frequency

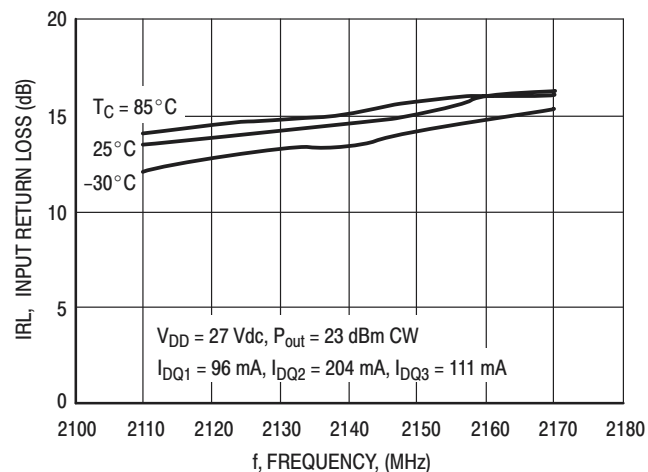


Figure 6. Input Return Loss versus Frequency

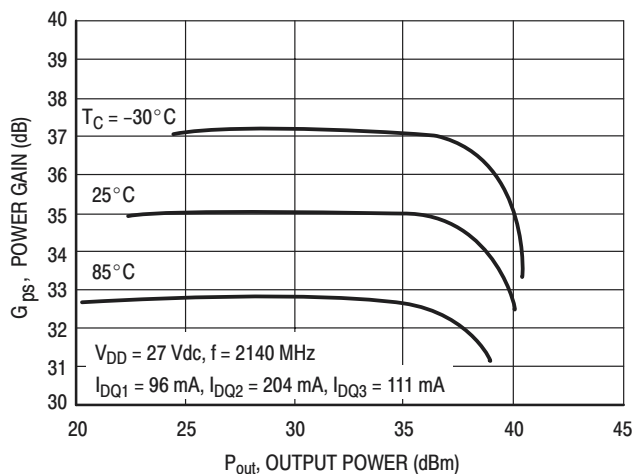


Figure 7. Power Gain versus Output Power

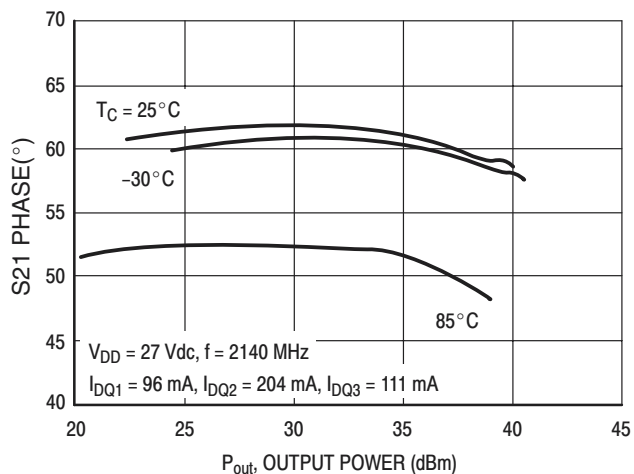


Figure 8. S21 Phase versus Output Power

TYPICAL CHARACTERISTICS

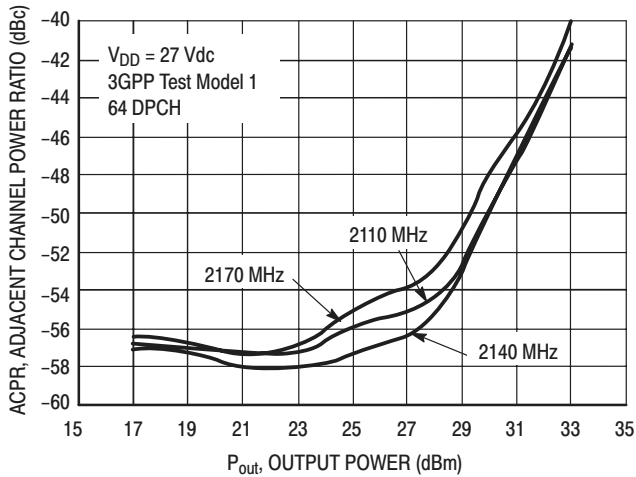


Figure 9. W-CDMA ACPR versus Output Power

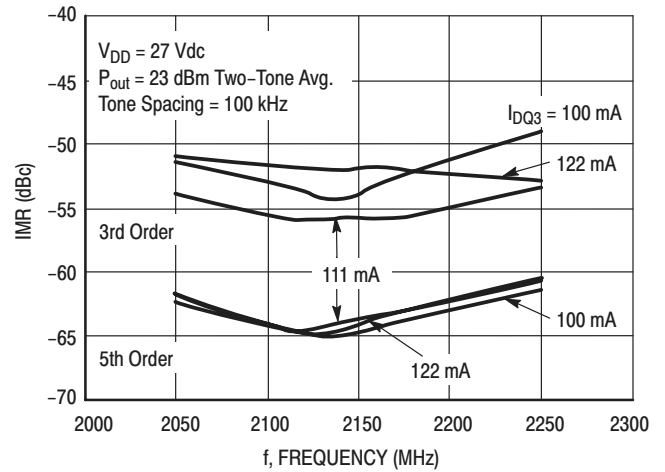


Figure 10. Two-Tone IMR versus Frequency

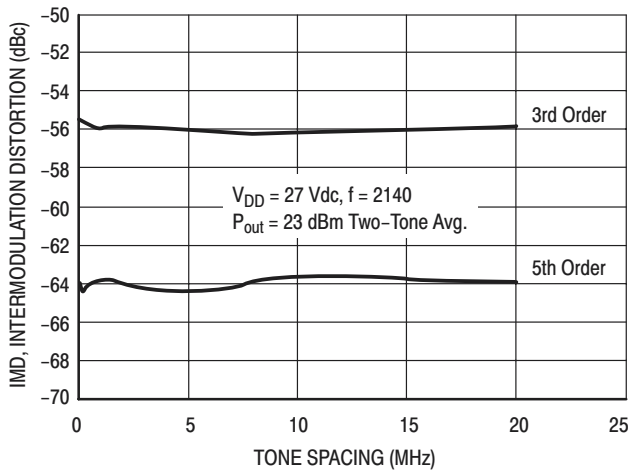


Figure 11. Two-Tone Broadband Performance

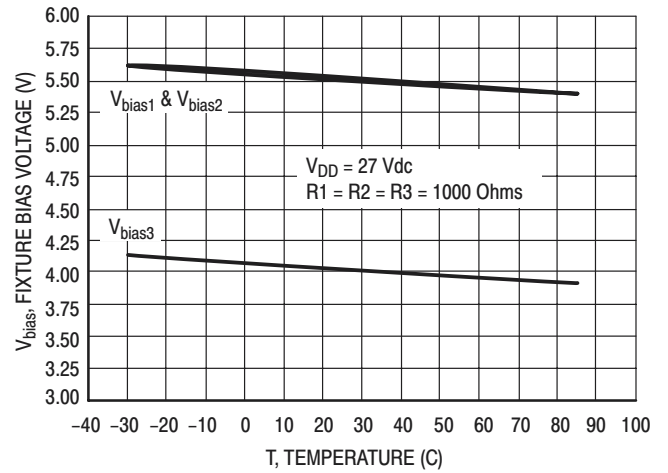


Figure 12. Fixture Bias versus Temperature

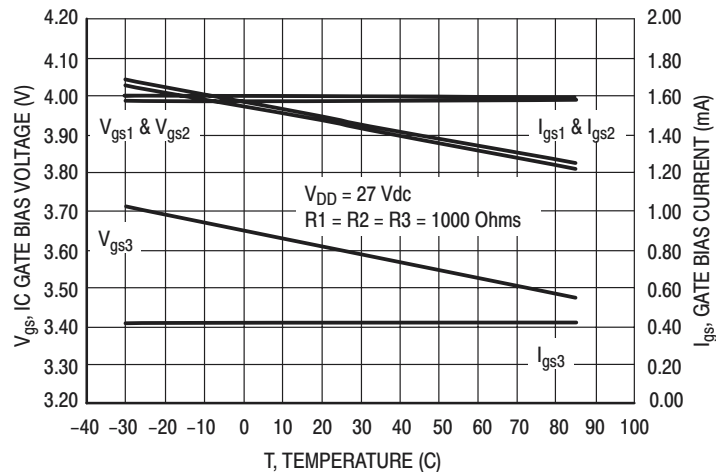
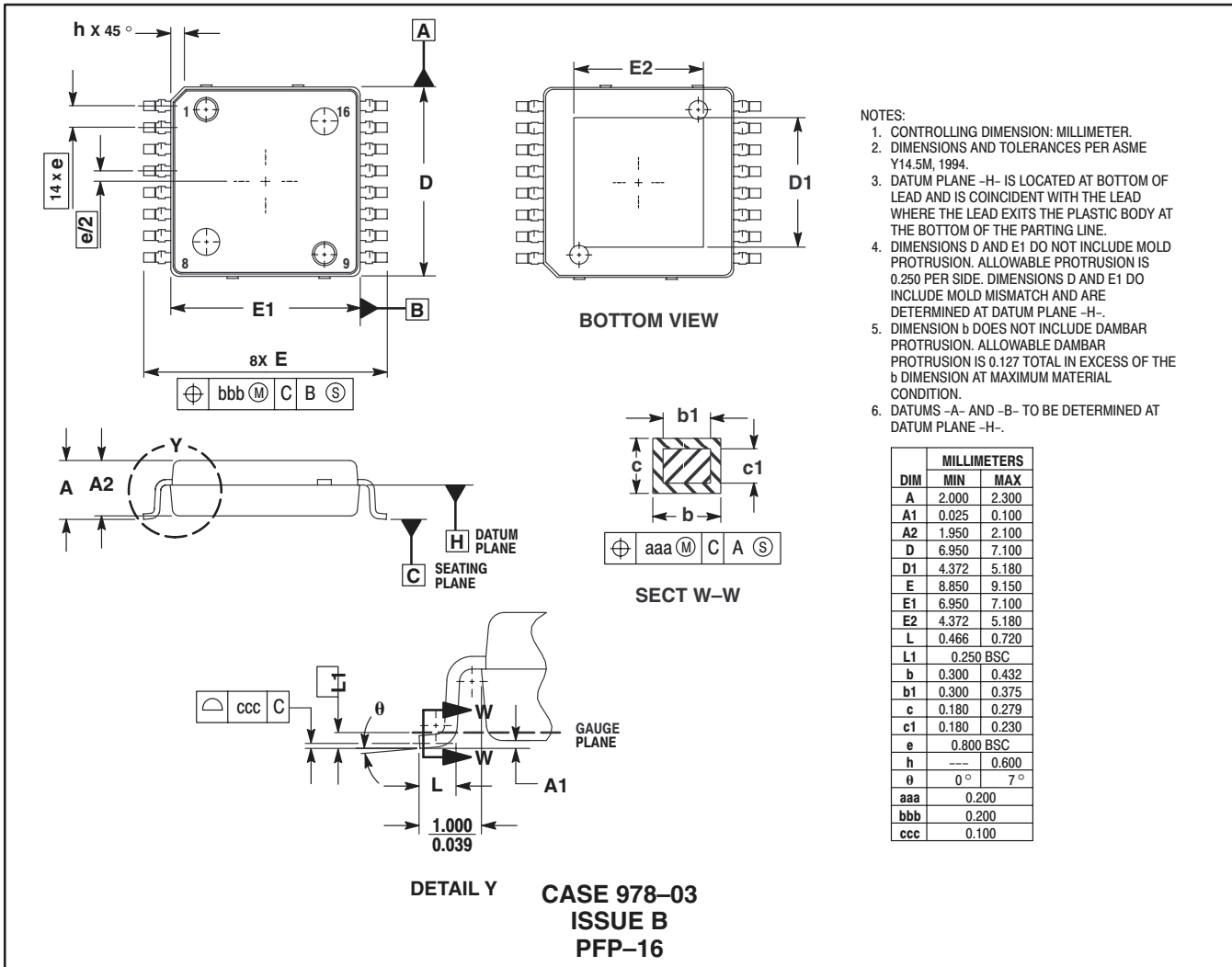


Figure 13. Gate Bias versus Temperature

NOTES

NOTES

PACKAGE DIMENSIONS



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