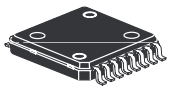
The RF Line

2.1–2.2 GHz SiFET RF Integrated Power Amplifier

MHVIC2115R2

2.2 GHz, 26 V, 23/34 dBm
W–CDMA
RF LDMOS INTEGRATED CIRCUIT



CASE 978–03
PFP–16

The MHVIC2115R2 is a 26 Volt integrated power amplifier designed for driver and output stage W–CDMA applications. The device is a three–stage amplifier with input matching using Motorola's high voltage LDMOS IC process. The device is packaged in a PFP–16 power flat pack package that provides excellent thermal performance through a solderable backside contact.

Driver Application

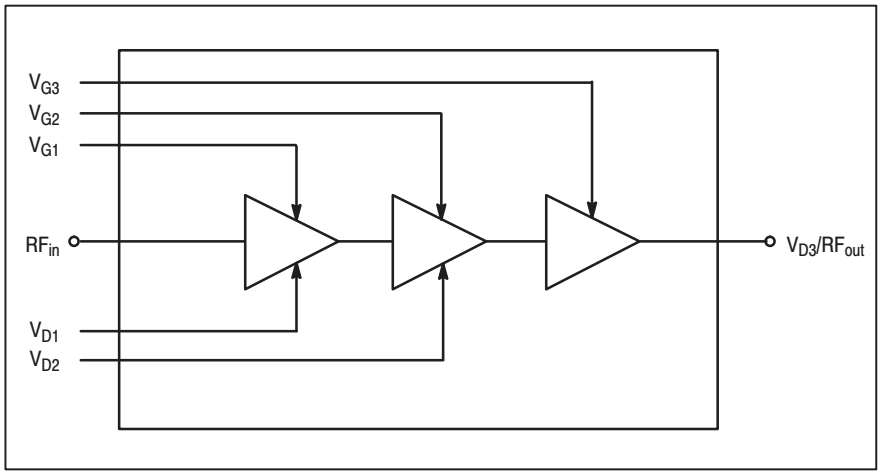
- Typical W–CDMA Performance: –53 dBc ACPR, 2.1–2.2 GHz, 26 Volts, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, 3GPP Test Model 1, Measured in a 3.84 MHz BW @ 5 MHz offset, 64 DTCH
  - Output Power — 23 dBm
  - Power Gain — 34 dB
- Gain Flatness = 0.3 dB from 2.1–2.17 GHz

Output Application

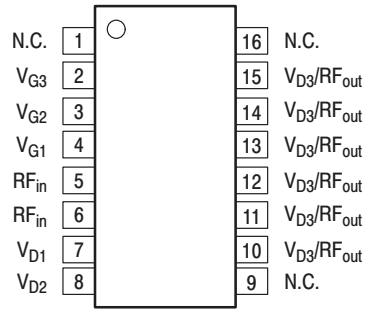
- Typical W–CDMA Performance: –45 dBc ACPR, 2.1–2.2 GHz, 27 Volts, I_{DQ1} = 56 mA, I_{DQ2} = 61 mA, I_{DQ3} = 117 mA, 3GPP Test Model 1, Measured in a 1.0 MHz BW @ 4 MHz offset, 64 DTCH
  - Output Power — 34 dBm
  - Power Gain — 30 dB
  - PAE = 16%
- P1dB = 15 Watts, Gain Flatness = 0.2 dB from 2.1 to 2.2 GHz
- On–Chip Input Matching to 50 Ohms Impedance
- High Gain and High Linearity
- Integrated ESD Protection
- Temperature Compensation Capability
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	150	°C



PIN CONNECTIONS



(Top View)

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THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = +0.2 W CW)	Stage 1, 26 Vdc, I_{DQ} = 96 mA Stage 2, 26 Vdc, I_{DQ} = 204 mA Stage 3, 26 Vdc, I_{DQ} = 111 mA		3.5	
Output Application (P_{out} = +2.5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 56 mA Stage 2, 27 Vdc, I_{DQ} = 61 mA Stage 3, 27 Vdc, I_{DQ} = 117 mA		2.7	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22–A113	3

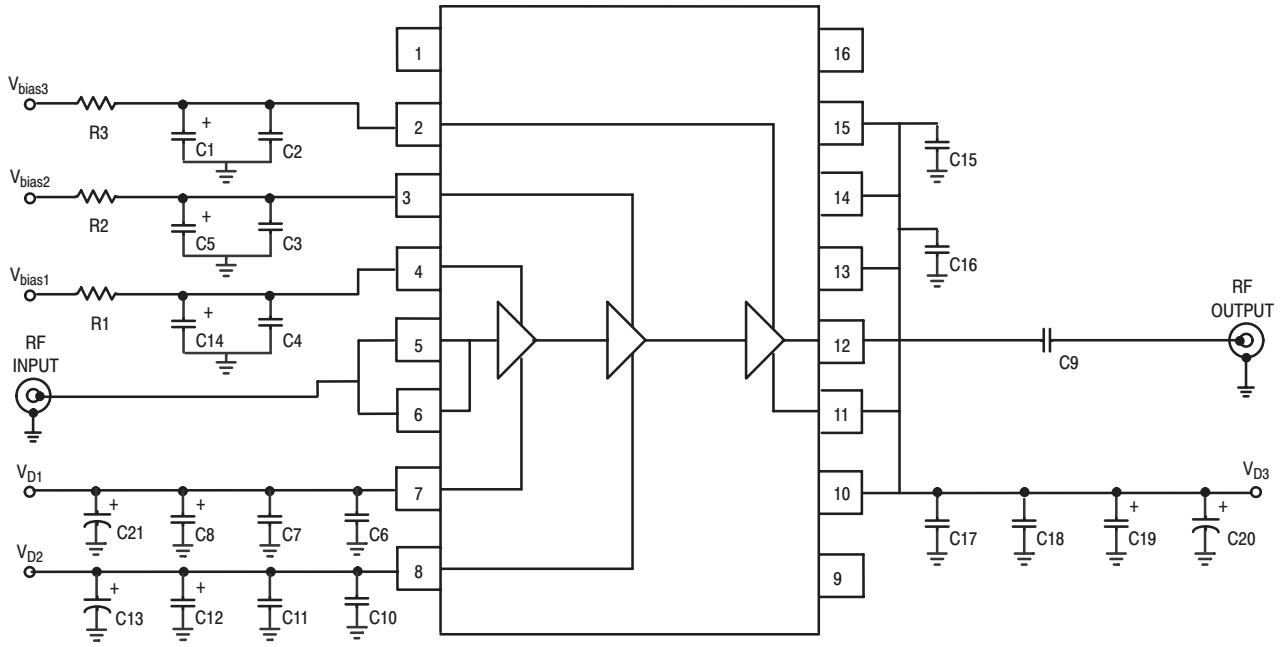
ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

W–CDMA CHARACTERISTICS (In Motorola Test Fixture) V_{DS} = 26 V, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, 2.11–2.17 GHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P_{out} = 23 dBm	G_{ps}	31	34	—	dB
Gain Flatness @ P_{out} = 23 dBm	G_F	—	0.3	0.5	dB
Input Return Loss @ P_{out} = 23 dBm	IRL	—	–12	–10	dB
Group Delay	—	—	1.7	—	ns
Phase Linearity	—	—	0.2	—	°
1–Carrier W–CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 23 dBm, 5 MHz Offset	ACPR	—	–53	–50	dBc
1–Carrier W–CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 28 dBm, 5 MHz Offset	ACPR	—	–50	—	dBc

W–CDMA CHARACTERISTICS (In Motorola Test Fixture) V_{DS} = 27 V, I_{DQ1} = 56 mA, I_{DQ2} = 61 mA, I_{DQ3} = 117 mA, 2.1–2.2 GHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ P_{out} = 34 dBm	G_{ps}	—	30	—	dB
Gain Flatness @ P_{out} = 34 dBm	G_F	—	0.2	—	dB
Input Return Loss @ P_{out} = 34 dBm	IRL	—	–12	—	dB
Power Added Efficiency @ P_{out} = 34 dBm	PAE	—	16	—	%
1–Carrier W–CDMA Conditions: Adjacent Channel Power Ratio @ P_{out} = 34 dBm, 4 MHz Offset	ACPR	—	–45	—	dBc



C1, C5, C8, C12, C14, C19	1 μF SMT Tantalum Chip Capacitors	C13, C20, C21	330 μF Electrolytic Capacitors (MCR35V337M10X16)
C2, C3, C4, C7, C11, C18	0.01 μF Chip Capacitors (0805C103K5RACTR)	R1, R2, R3	1 kΩ Chip Resistors (0805)
C6, C10, C17	6.8 pF Chip Capacitors, ACCU–P (AVX 08051J6R8BBT)	PCB	Arlon, 20 mils, ε_r = 2.55
C9, C15, C16	1.8 pF Chip Capacitors, ACCU–P (AVX 08051J1R8BBT)		

Figure 1. 2.2 GHz Demo Board Schematic

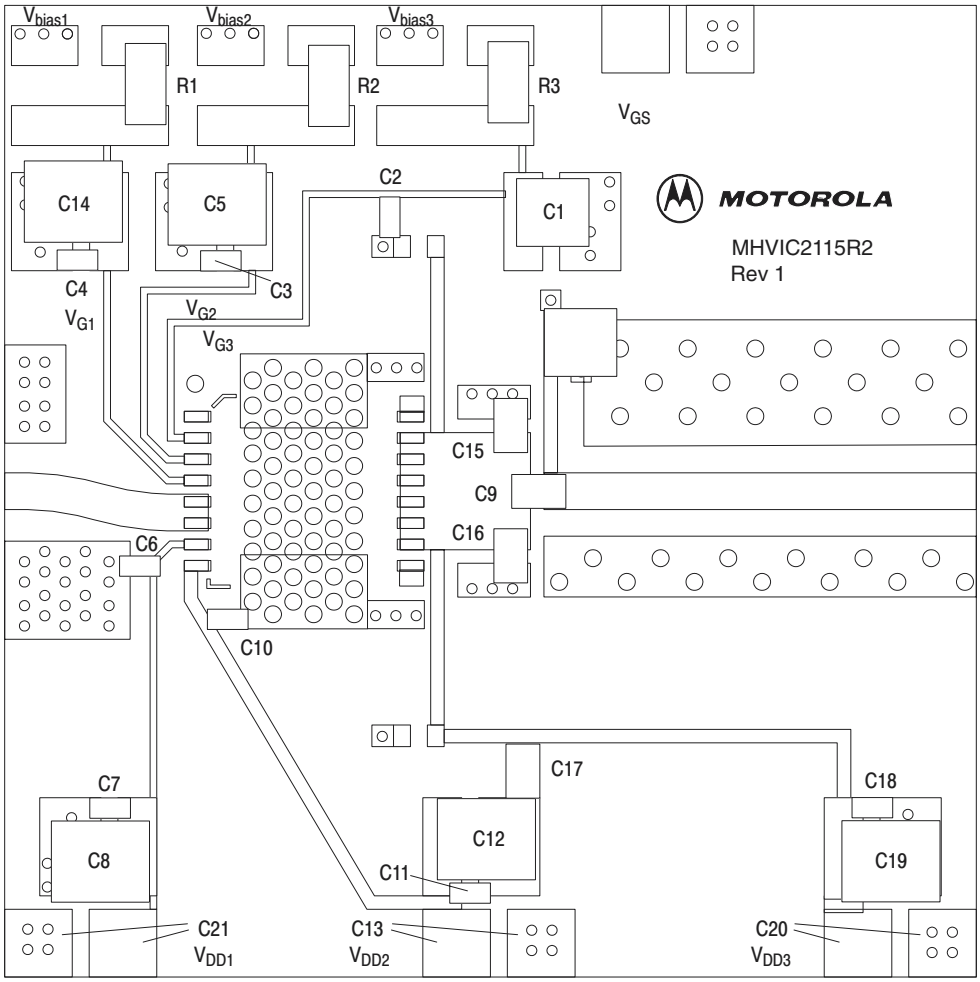


Figure 2. 2.2 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

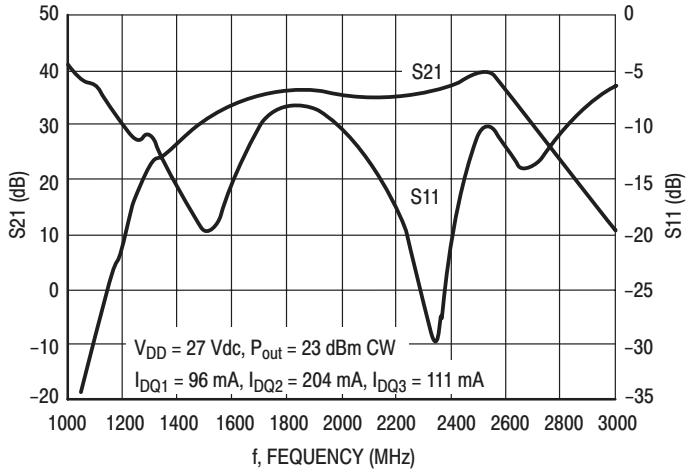


Figure 3. Broadband Frequency Response

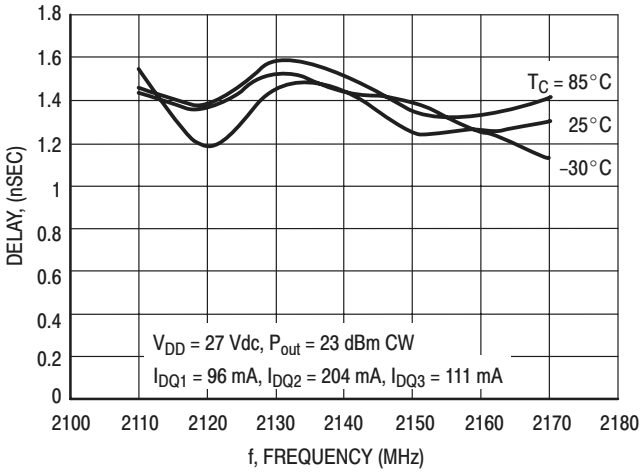


Figure 4. Delay versus Frequency

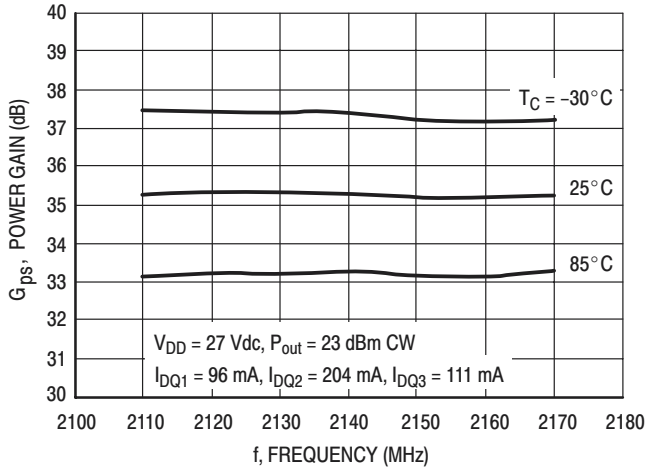


Figure 5. Power Gain versus Frequency

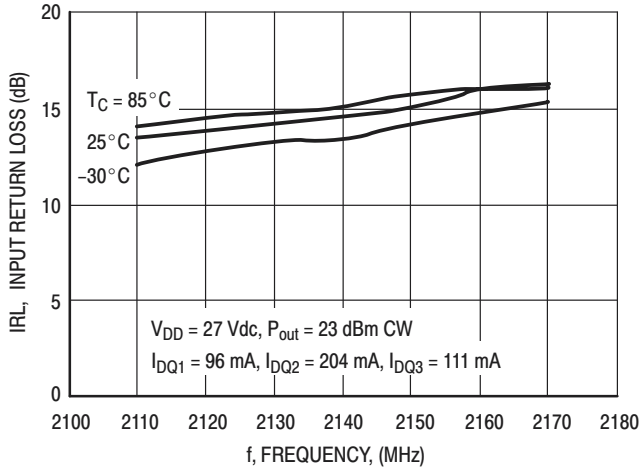


Figure 6. Input Return Loss versus Frequency

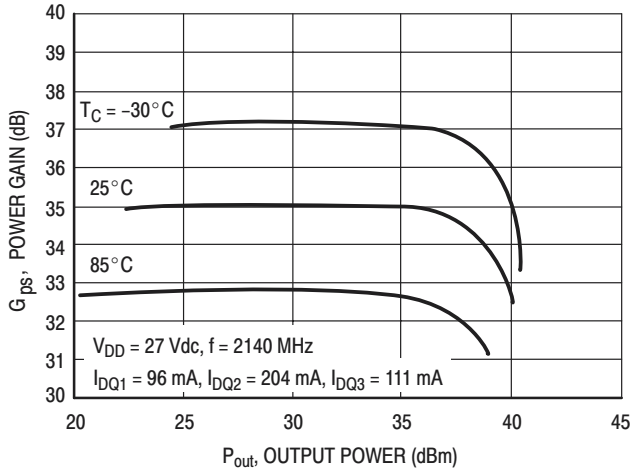


Figure 7. Power Gain versus Output Power

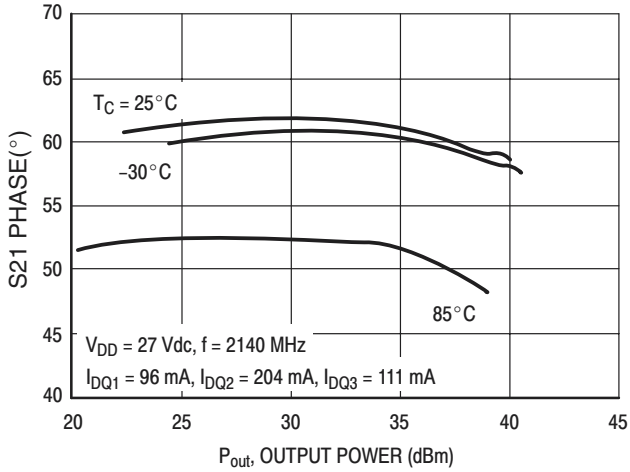


Figure 8. S21 Phase versus Output Power

TYPICAL CHARACTERISTICS

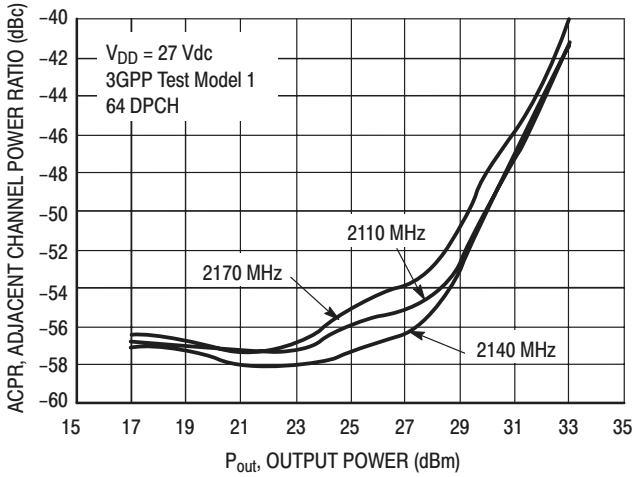


Figure 9. W–CDMA ACPR versus Output Power

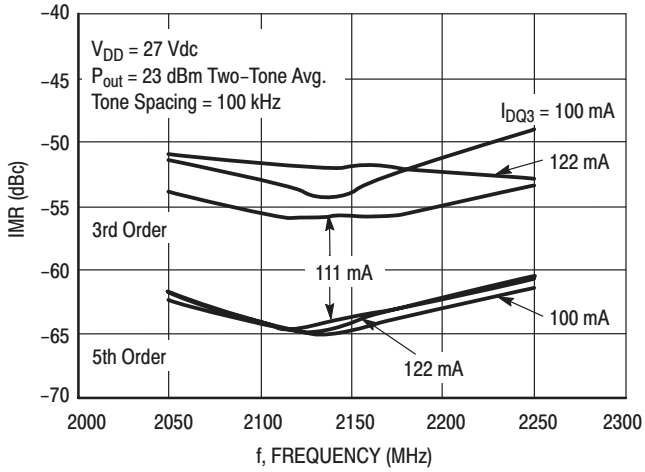


Figure 10. Two–Tone IMR versus Frequency

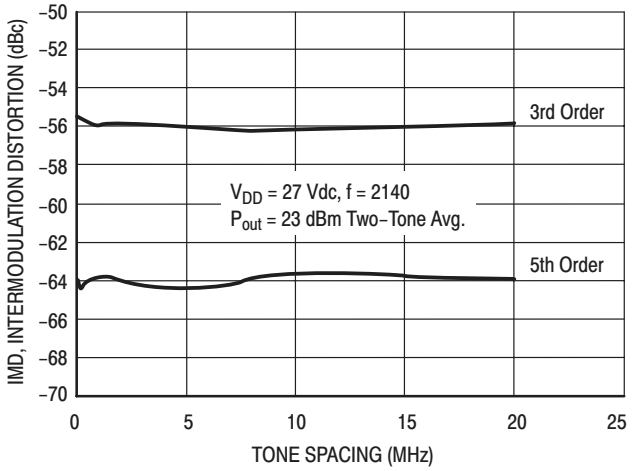


Figure 11. Two–Tone Broadband Performance

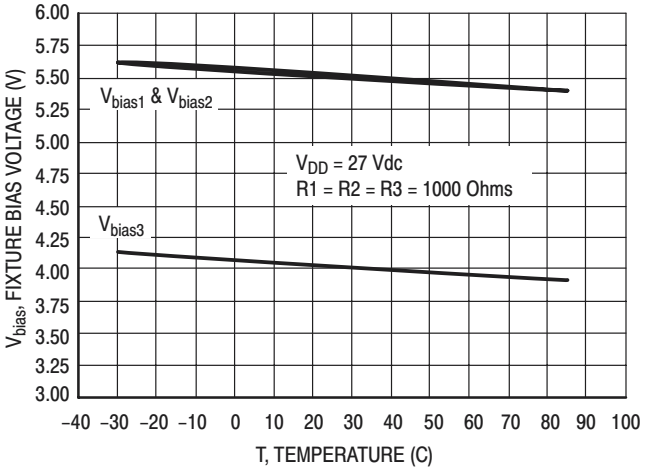


Figure 12. Fixture Bias versus Temperature

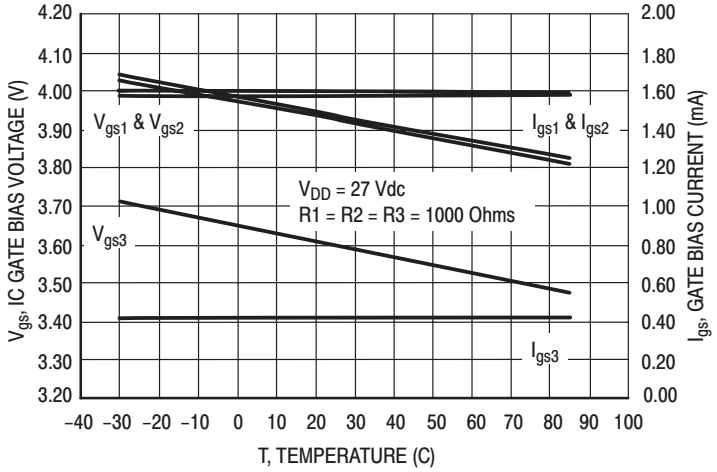
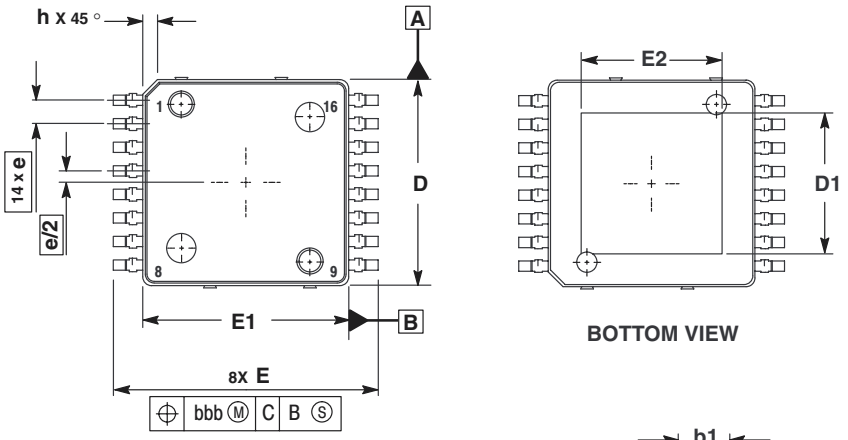


Figure 13. Gate Bias versus Temperature

NOTES

NOTES

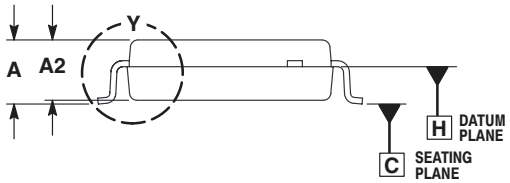
PACKAGE DIMENSIONS

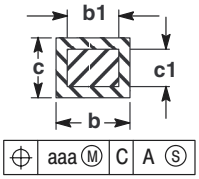


BOTTOM VIEW

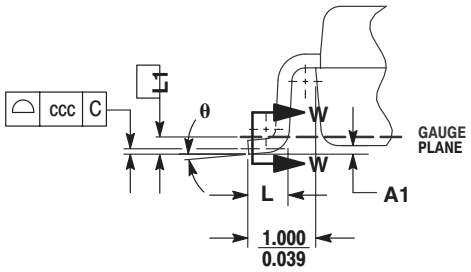
NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	





SECT W–W



DETAIL Y

CASE 978–03
ISSUE B
PFP–16

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