The RF Line

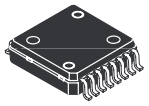
746-960 MHz RF LDMOS Wideband Integrated Power Amplifier

MHVIC915R2

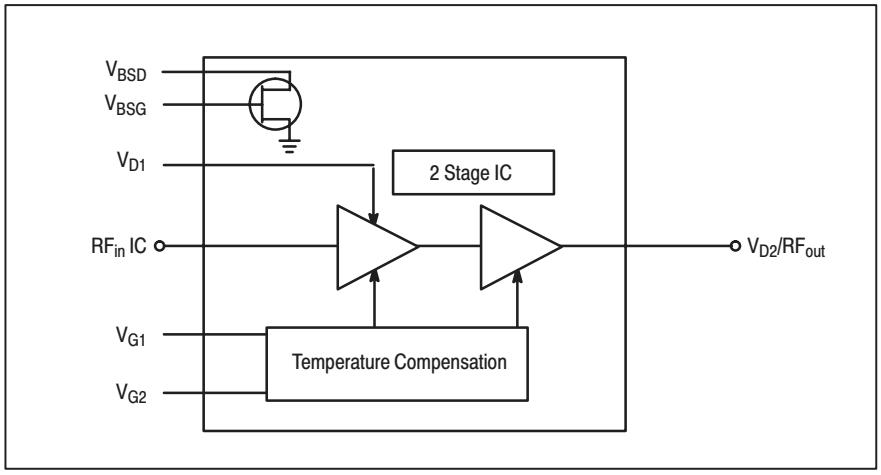
CDMA, GSM/GSM EDGE
746–960 MHz, 15 W, 27 V
RF LDMOS WIDEBAND
INTEGRATED AMPLIFIER

The MHVIC915R2 wideband integrated circuit is designed for CDMA and GSM/GSM EDGE applications. It uses Motorola's newest high voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi–stage structure. Its wideband On–Chip integral matching circuitry makes it usable from 746 to 960 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, and CDMA. The device is packaged in a PFP–16 flat pack package that provides excellent thermal performance through a solderable backside contact.

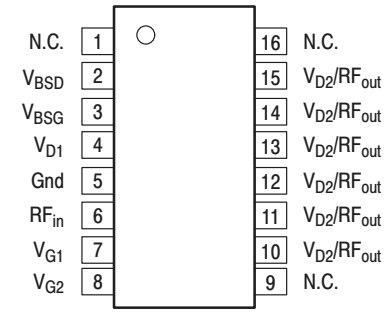
- Typical CDMA Performance: 869–894 MHz, 27 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, 1–Carrier N–CDMA, IS–95 CDMA 9–Channel Forward
  Driver Application
  Output Power — 23 dBm
  Power Gain — 31 dB
  Adjacent Channel Power Ratio —
  –60 dBc @ 750 kHz in a 30 kHz BW
  –66 dBc @ 1.98 MHz in a 30 kHz BW
  Output Application
  Output Power — 34 dBm
  PAE = 21%
  Adjacent Channel Power Ratio —
  –50 dBc @ 750 kHz in a 30 kHz BW
- Typical GSM Performance: 921–960 MHz, 26 Volts
  Output Power — 15 W P1dB
  Power Gain — 30 dB @ P1dB
  Drain Efficiency = 56% @ P1dB
- On–Chip Matching (50 Ohm Input, >9 Ohm Output)
- On–Chip Current Mirror g_m Sensing FET for Self Bias Application
- Integrated Temperature Compensation Capability
- Usable for SCPA and MCPA Architecture
- Integrated ESD Protection
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.



CASE 978–03
PFP–16
PLASTIC



PIN CONNECTIONS



(Top View)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = 0.2 W CW)	Stage 1, 27 Vdc, I_{DQ} = 80 mA Stage 2, 27 Vdc, I_{DQ} = 120 mA		5.07	
Output Application (P_{out} = 2.5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 80 mA Stage 2, 27 Vdc, I_{DQ} = 120 mA		3.73	
GSM Application (P_{out} = 15 W CW)	Stage 1, 26 Vdc, I_{DQ} = 50 mA Stage 2, 26 Vdc, I_{DQ} = 140 mA		3.41	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C4 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22–A113	3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
CDMA FUNCTIONAL TESTS (In Motorola CDMA Test Fixture, 50 ohm system) V_{DS} = 27 V, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, 880 MHz, 1–Carrier N–CDMA, IS–95 CDMA 9–Channel Forward					
Common–Source Amplifier Power Gain (P_{out} = 23 dBm)	G_{ps}	29	31	—	dB
Power Added Efficiency (P_{out} = 34 dBm)	η	—	21	—	%
Input Return Loss (P_{out} = 23 dBm)	IRL	—	–12	–9	dB
Adjacent Channel Power Ratio (P_{out} = 23 dBm) @ 750 kHz offset in 30 kHz BW	ACPR	—	–60	–55	dBc
Adjacent Channel Power Ratio (P_{out} = 34 dBm) @ 750 kHz offset in 30 kHz BW	ACPR	—	–50	—	dBc
Gain Flatness @ P_{out} = 23 dBm (865 MHz to 895 MHz)	G_F	—	0.2	0.4	dB
Bias Sense FET Drain Current V_{BSD} = 27 V $V_{BIAS\ BSG} = V_{BIAS2\ Q2}$ @ I_{DQ2} = 120 mA	I_{BSD}	0.8	1.2	1.6	mA

(continued)

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

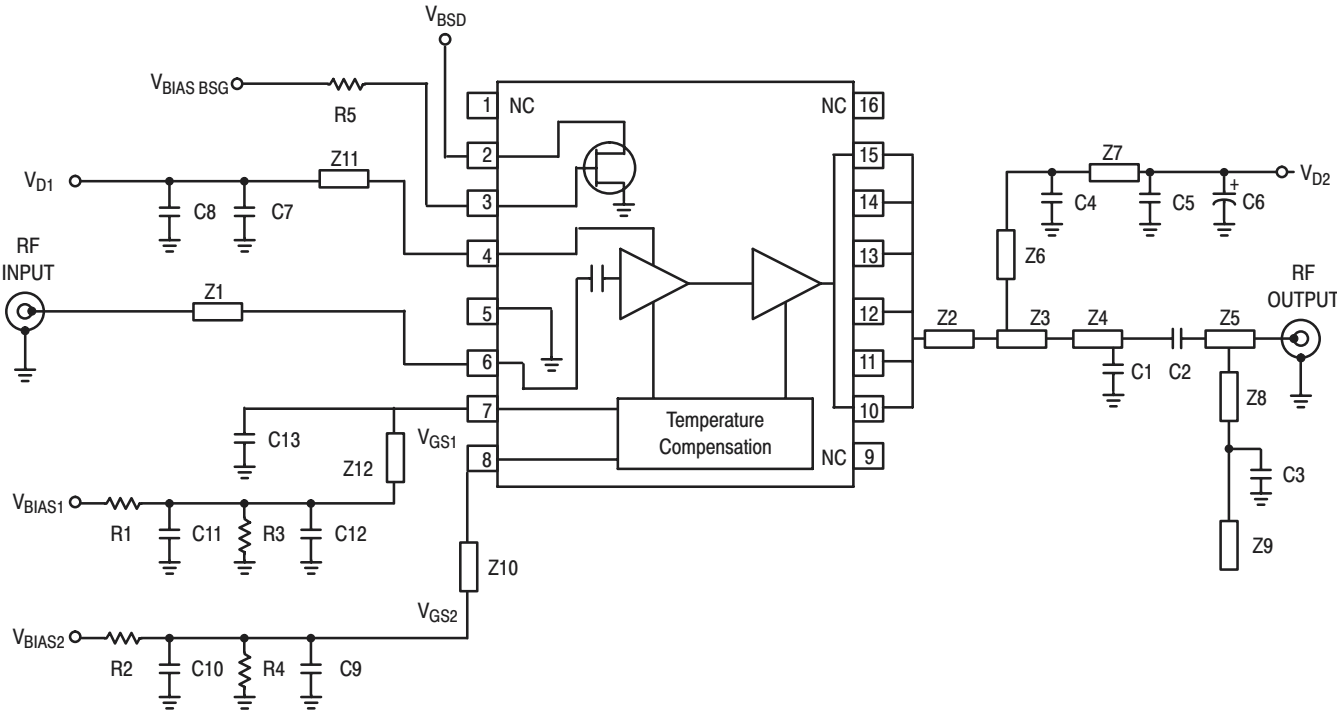
Characteristic	Symbol	Min	Typ	Max	Unit

PERFORMANCE TESTS (In Motorola Test Fixture, 50 ohm system) V_{DS} = 27 V, I_{DQ1} = 80 mA, I_{DQ2} = 120 mA, 865–895 MHz

Rating	Symbol	Min	Typ	Max	Unit
Quiescent Current Accuracy over Temperature (–10 to 85°C) at Nominal Value	ΔIqt	—	±5	—	%
Gain Flatness @ P_{out} = 23 dBm (800 MHz to 960 MHz)	G_F	—	0.20	—	dB
Deviation from Linear Phase @ P_{out} = 23 dBm	∅	—	±0.2	—	°
Group Delay @ P_{out} = 23 dBm	Delay	—	2.2	—	ns
Insertion Phase Window @ P_{out} = 23 dBm (part to part)	Δ∅	—	±10	—	°

GSM FUNCTIONAL TESTS (In Motorola GSM Test Fixture, 50 ohm system) V_{DS} = 26 V, I_{DQ1} = 50 mA, I_{DQ2} = 140 mA, 921–960 MHz, CW

Rating	Symbol	Min	Typ	Max	Unit
Output Power at 1dB Compression Point	P1dB	—	15	—	Watts
Common–Source Amplifier Power Gain @ P1dB	Gain	—	30	—	dB
Drain Efficiency @ P1dB	η	—	56	—	%
Input return Loss @ P1dB	IRL	—	–16	—	dB
EVM @ 5 W	—	—	0.9	—	%
Third Order Intermodulation Distortion (15 W PEP, 2 Tone 100 kHz spacing)	IMD3	—	–30	—	dBc
Drain Efficiency (15 W PEP, 2 Tone 100 kHz spacing)	η	—	35	—	%



Z1	0.0438″ x 0.400″ 50 Ω Microstrip	Z7	0.0504″ x 0.480″ Microstrip
Z2	0.1709″ x 0.1004″ Microstrip (not including IC pad length)	Z8	0.0252″ x 0.843″ Microstrip
		Z9	0.0252″ x 0.167″ Microstrip
Z3	0.1222″ x 0.1944″ Microstrip	Z10	0.040″ x 0.850″ Microstrip
Z4	0.0836″ x 0.3561″ Microstrip	Z11	0.025″ x 0.400″ Microstrip
Z5	0.0438″ x 0.2725″ Microstrip	Z12	0.020″ x 0.710″ Microstrip
Z6	0.0504″ x 0.3378″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 1. MHVIC915 746–960 MHz Test Circuit Schematic

Table 1. MHVIC915 746–960 MHz Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1, C2	4.7 pF High Q Capacitors (0603)	ATC600S4R7CW	ATC
C3, C4	47 pF NPO Capacitors (0805)	GRM40–001COG470J050BD	Murata
C5, C8, C10, C11	1 μF X7R Chip Capacitors (1214)	GRM42–2X7R105K050AL	Murata
C6	10 μF, 50 V Electrolytic Capacitor	ECEV1HA100SP	Panasonic
C7, C9, C12	0.01 μF X7R Chip Capacitors (0805)	GRM40X7R103J050BD	Murata
C13	8.2 pF NPO Chip Capacitor (0805)	GRM40–001COG8R2C050BD	Murata
R1, R2, R5	1 kΩ Chip Resistors (0603)	RM73B2AT102J	KOA Speer
R3, R4	100 kΩ Chip Resistors (0603)	RM73B2AT104J	KOA Speer

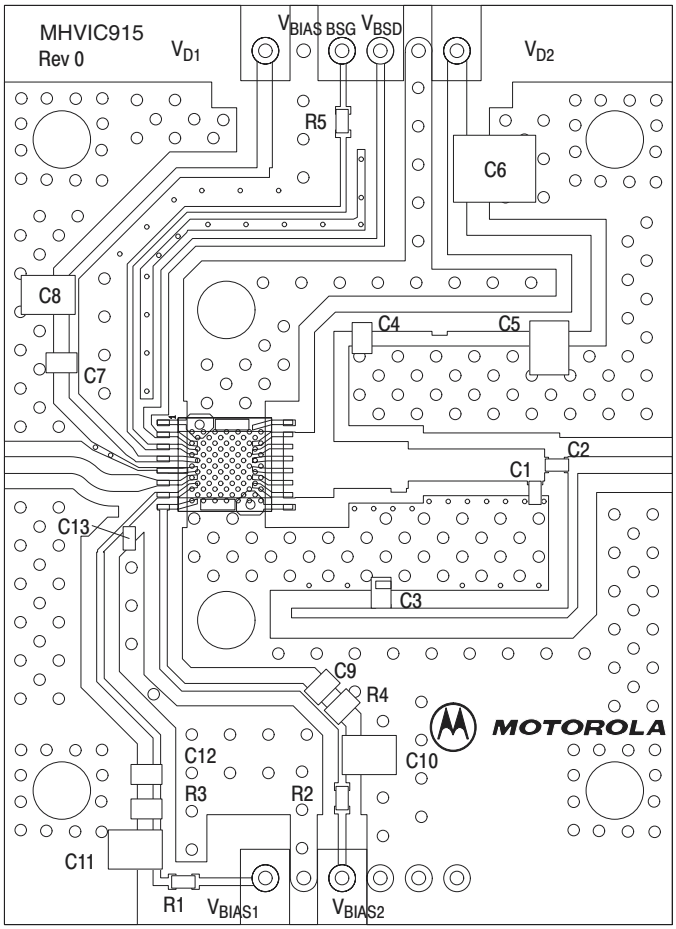


Figure 2. MHVIC915 746–960 MHz Test Circuit Component Layout

TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

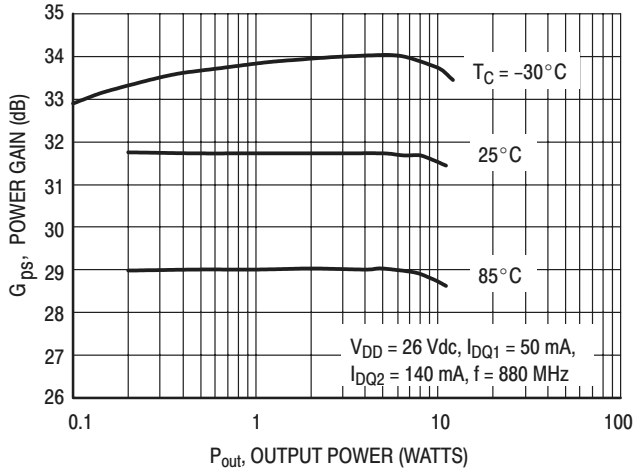


Figure 3. Power Gain versus Output Power

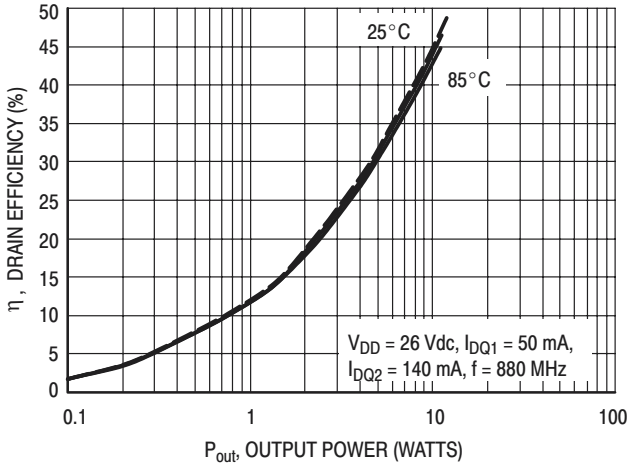


Figure 4. Drain Efficiency versus Output Power

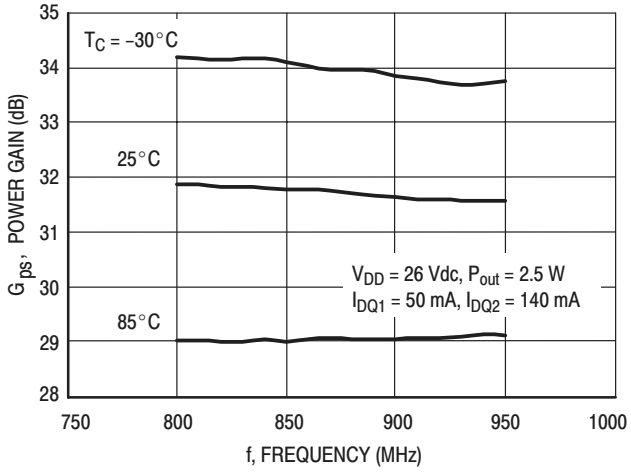


Figure 5. Power Gain versus Frequency

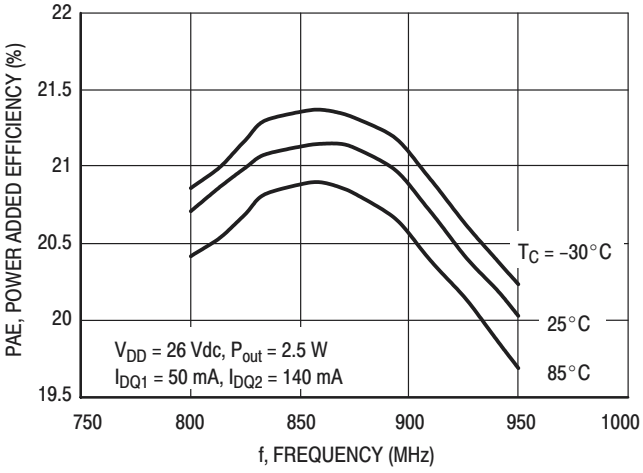


Figure 6. Power Added Efficiency versus Frequency

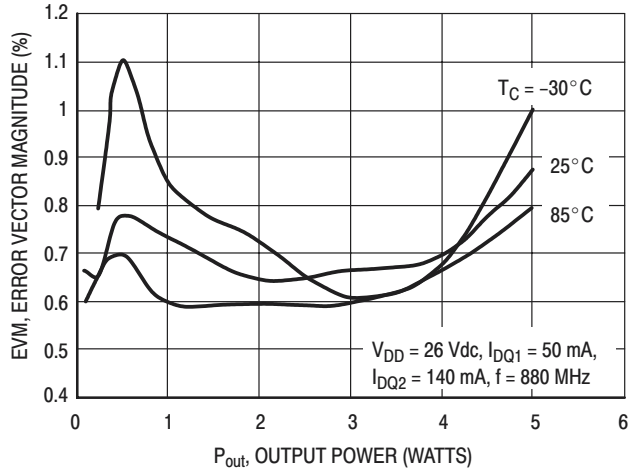


Figure 7. Error Vector Magnitude versus Output Power

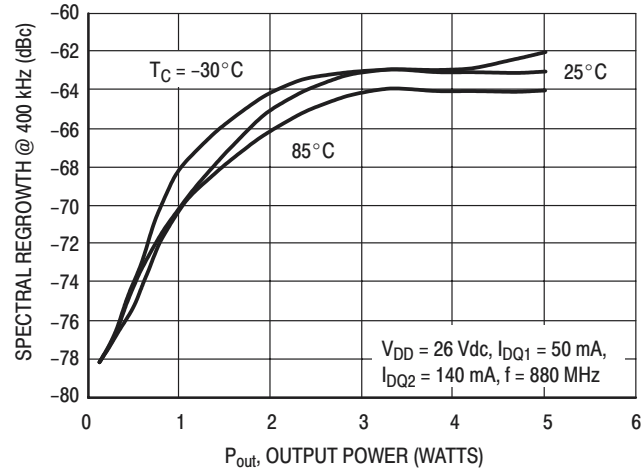


Figure 8. Spectral Regrowth @ 400 kHz versus Output Power

TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

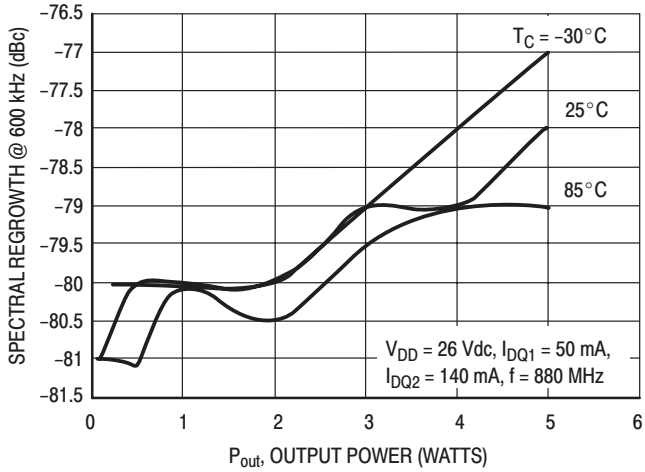


Figure 9. Spectral Regrowth @ 600 kHz versus Output Power

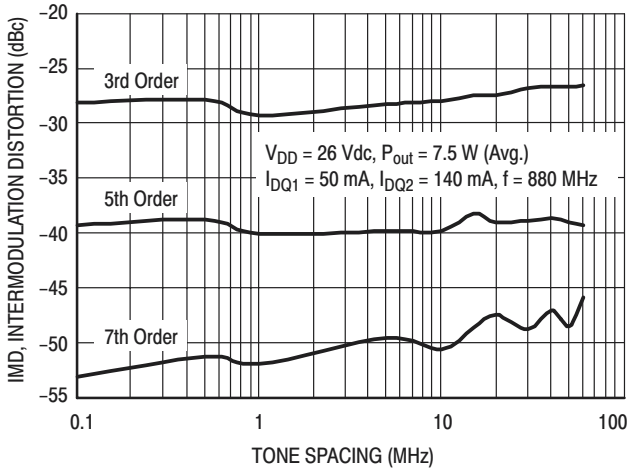


Figure 10. Two–Tone Broadband Performance

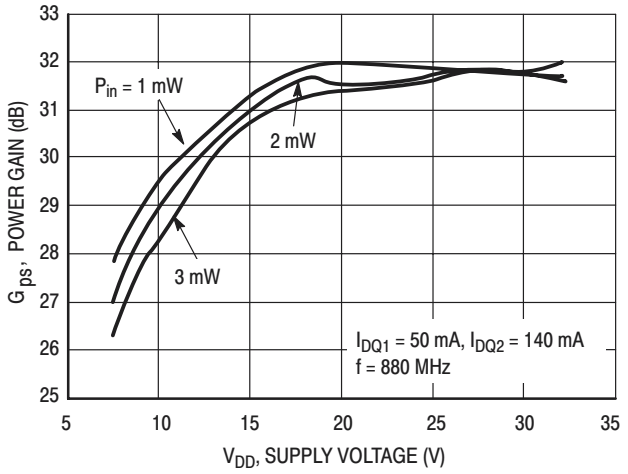


Figure 11. Power Gain versus Supply Voltage

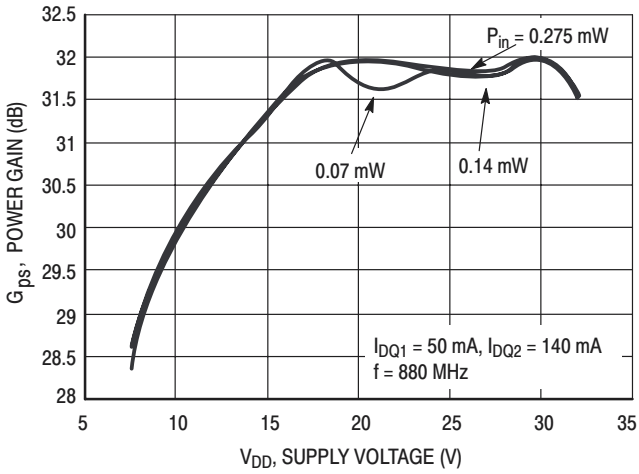


Figure 12. Power Gain versus Supply Voltage

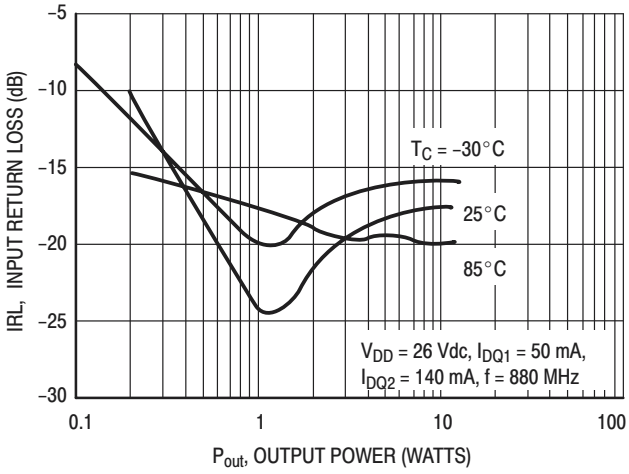


Figure 13. Input Return Loss versus Output Power

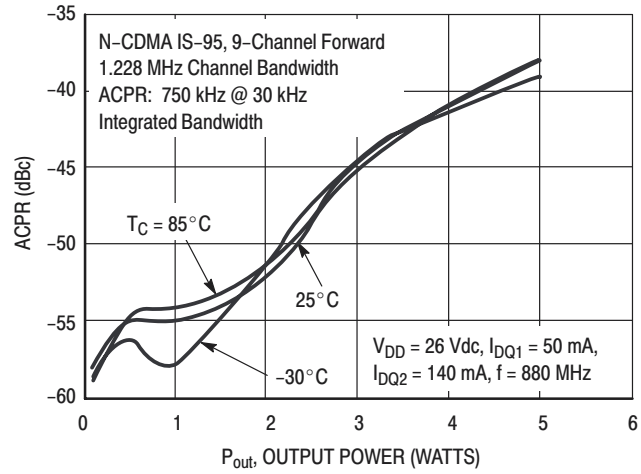
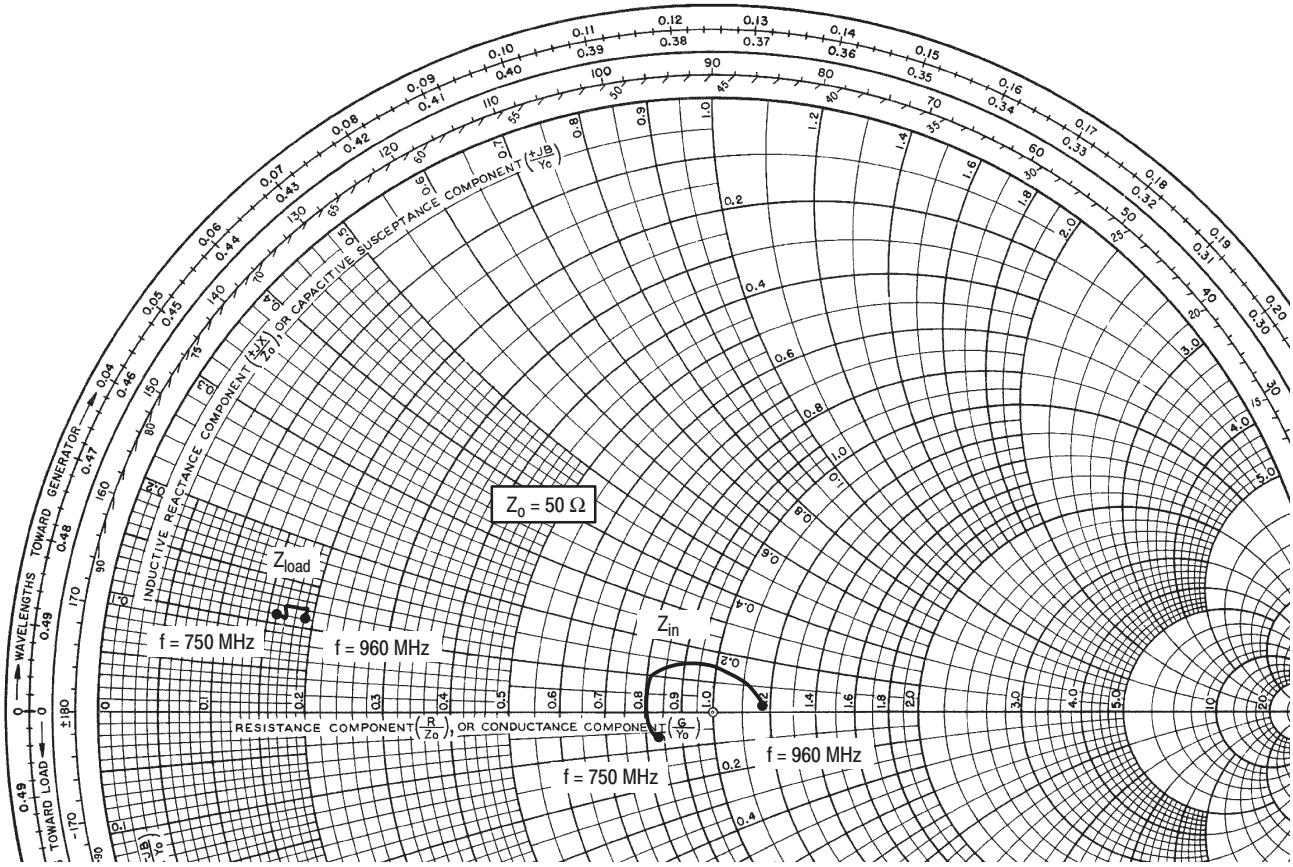


Figure 14. Adjacent Channel Power Ratio versus Output Power



V_{DD} = 26 Vdc, I_{DQ1} = 50 mA, I_{DQ2} = 140 mA, P_{out} = 1.25 W CW

f MHz	Z_{in} Ω	Z_{load} Ω
750	42.11 – j2.79	8.24 + j5.33
765	40.86 – j1.37	8.31 + j5.56
780	40.09 + j0.06	8.39 + j5.82
795	39.77 + j1.52	8.50 + j5.95
810	39.89 + j3.01	8.62 + j6.02
825	40.49 + j4.39	8.82 + j6.12
840	41.48 + j5.70	8.94 + j6.19
855	42.89 + j6.73	9.12 + j6.17
870	43.51 + j7.03	9.16 + j6.12
885	46.81 + j7.87	9.33 + j6.09
900	49.21 + j7.74	9.38 + j5.95
915	51.79 + j7.02	9.50 + j5.85
930	54.48 + j5.65	9.47 + j5.73
945	57.05 + j3.61	9.54 + j5.63
960	59.16 + j0.75	9.42 + j5.45

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

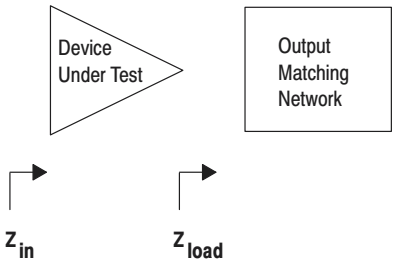


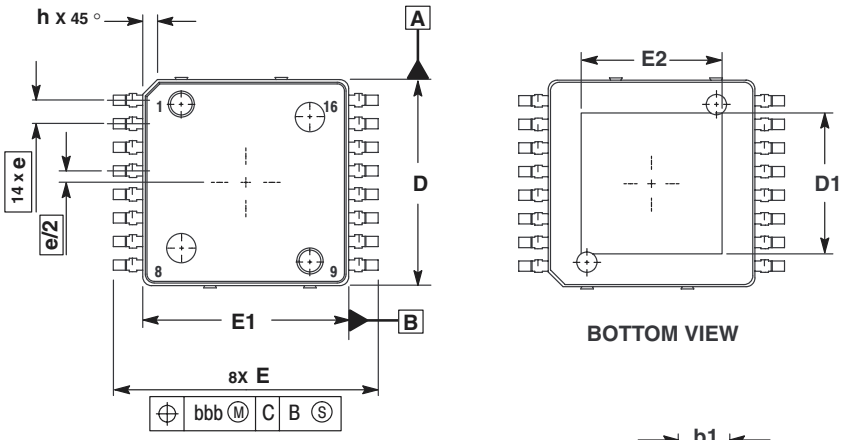
Figure 15. Series Equivalent Input and Output Impedance

NOTES

NOTES

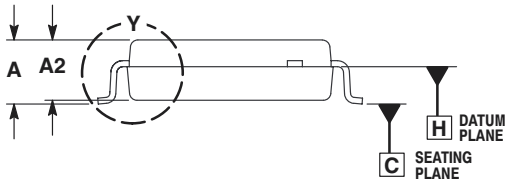
NOTES

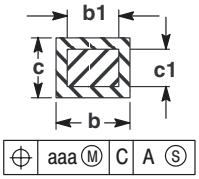
PACKAGE DIMENSIONS



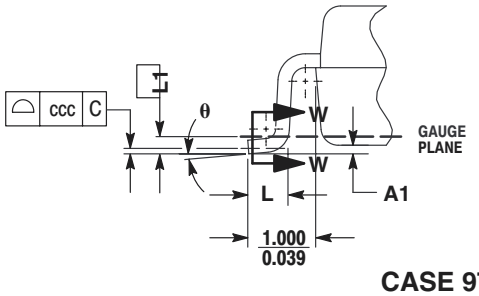
BOTTOM VIEW

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.





SECT W–W



DETAIL Y

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–03
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PFP–16
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