MOSTEK

MEMORY COMPONENTS

64K-Bit Read-Only Memory

MK36000(P/J/N) Series

FEATURES

- ☐ MK36000 8K x 8 Organization— "Edge Activated" * operation ($\overline{CE}$)
- ☐ Access Time/Cycle Time

P/N	Access	Cycle
MK36000-4	250 ns	375 ns
MK36000-5	300 ns	450 ns

- ☐ Single +5V ± 10% Power Supply
- ☐ Standard 24 pin DIP
- ☐ Low Power Dissipation - 220mW Max Active
- ☐ Low Standby Power Dissipation - 45mW Max, ($\overline{CE}$ High)
- ☐ On chip latches for addresses
- ☐ Inputs and three-state outputs - TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF
- ☐ MKB version screened to MIL-STD-883

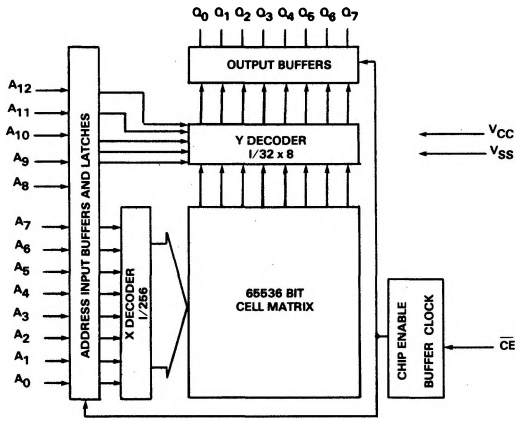
DESCRIPTION

The MK36000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

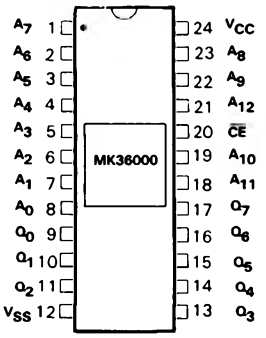
Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 45mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed.

FUNCTIONAL DIAGRAM (MK36000)



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	Address	V_{SS}	GND
Q_0-Q_7	Outputs	$\overline{CE}$	Chip Enable
V_{CC}	+5V		

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature - Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature - Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$) [6]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3 mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220 μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$)[6]

SYM	PARAMETER	-4		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10000	300	10000	ns	4
t_{AC}	$\overline{CE}$ Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_p	$\overline{CE}$ Precharge Time	125		150		ns	

NOTES:

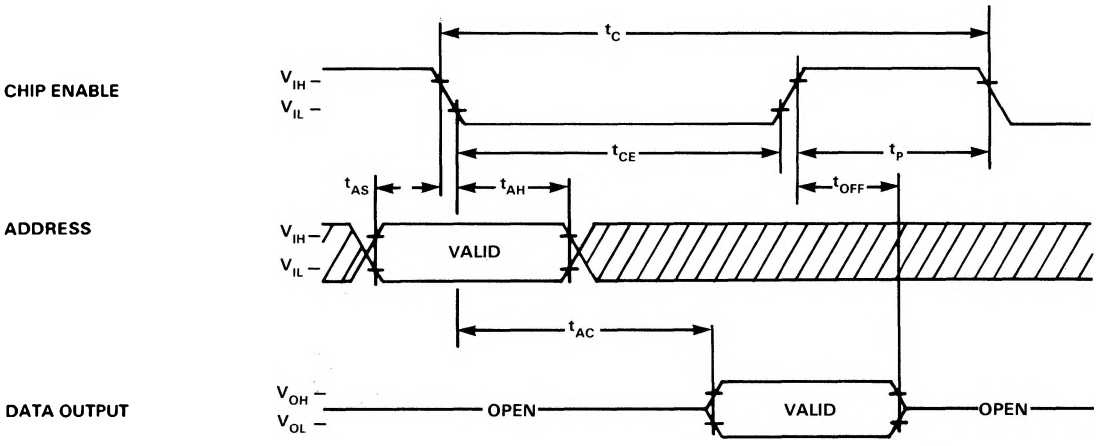
1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0 V to 5.5 V (V_{CC} = 5 V)
3. Device unselected; V_{OUT} = 0 V to 5.5 V
4. Measured with 2 TTL loads and 100 pF, transition times = 20 ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.

CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM



DESCRIPTION (Continued)

The MK36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MK36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The MK36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MK36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the on-chip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.