MOSTEK®

Z80 MICROCOMPUTER

Counter Timer Circuit

MK3882

FEATURES

- All inputs and outputs fully TTL compatible
- Each channel may be selected to operate in either Counter Mode or Timer Mode
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- Interrupts may be programmed to occur on the zero count condition in any channel
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic

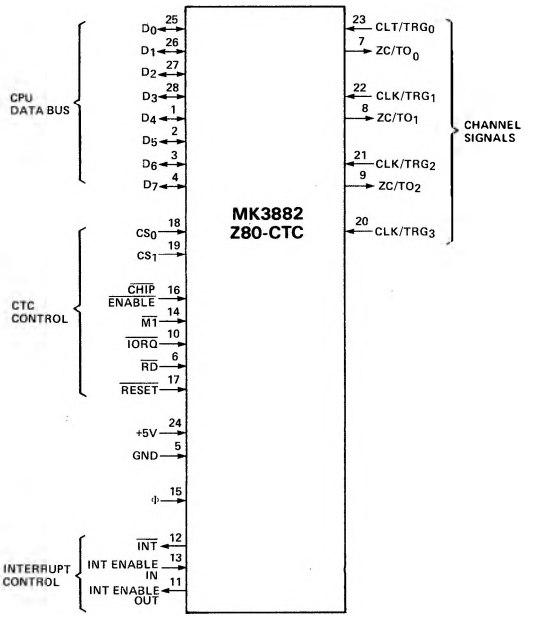
INTRODUCTION

The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

CTC PIN DESCRIPTION

A diagram of the Z80-CTC pin configuration is shown in Figure 1. This section describes the function of each pin.

Z80-CTC PIN CONFIGURATION
Figure 1



D_7-D_0 Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D_0 is the least significant.

CS1-CS0 Channel Select (input, active high)
These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O Write or Read (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

$\overline{CE}$ Chip Enable (input, active low)
A low level on this pin enables the CTC to accept control words, Interrupt Vectors, or time constant data words from the Z80 Data

Bus during an I/O Write cycle, or to transmit the contents of the Down Counter to the CPU during an I/O Read cycle. In most applications this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four Counter/Timer Channels.

Clock (Φ) — System Clock (input)
This single-phase clock is used by the CTC to synchronize certain signals internally.

$\overline{M1}$ — Machine Cycle One Signal from CPU (input, active low)
When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the CPU is fetching an instruction from memory. When $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt, alerting the CTC to place an Interrupt Vector on the Z80 Data Bus if it has daisy chain priority and one of its channels has requested an interrupt.

$\overline{IORQ}$ — Input/Output Request from CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the $\overline{CE}$ and $\overline{RD}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its Interrupt Vector on the Z80 Data Bus.

$\overline{RD}$ — Read Cycle Status from the CPU (input, active low)
The $\overline{RD}$ signal is used in conjunction with the $\overline{IORQ}$ and $\overline{CE}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus.

IEI — Interrupt Enable In (input, active high)
This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when more than one peripheral device in the system has interrupting capability. A high level on this pin indicates that no other interrupting devices of higher priority are being serviced by the Z80-CPU.

IEO — Interrupt Enable Out (output, active high)
The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IEO is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by the CPU.

$\overline{INT}$ — Interrupt Request (output, open drain, active low)
This signal goes true when any CTC channel which has been programmed to enable interrupts has a zero-count condition in its Down Counter.

$\overline{RESET}$ — Reset (input, active low)
This signal stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The ZC/TO and $\overline{INT}$ outputs go to their inactive states, IEO reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3-CLK/TRG0 — External Clock/Timer Trigger (input, user-selectable active high or low)
There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the Counter Mode, every active edge on this pin decrements the Down Counter. In the Timer Mode, an active edge on this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2—ZC/TO0 — Zero Count/Timeout (output, active high)
There are three ZC/TO pins, corresponding to CTC channels 2 through 0. (Due to package pin limitations channel 3 has no ZC/TO pin.) In either Counter Mode or Timer Mode, when the Down Counter decrements to zero an active high going pulse appears at this pin.

For further details on this device, please consult the CTC MK3882 Technical Manual, included in Section IV.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified operating range
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect To Ground ..... -0.3 V to +7 V
Power Dissipation ..... 0.8 W

All ac parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage (1)	V_{CC} -.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 400 nsec**
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V

**T_C = 250 nsec for MK3882-4

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_Φ	Clock Capacitance	20	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	38823882-4 MIN	38823882-4 MAX	MIN	MAX	UNIT	COMMENTS
Φ	t_C	Clock Period	400	(1)	250	(1)	ns	
	t_W(ΦH)	Clock Pulse Width, Clock High	170	2000	105	2000	ns	
	t_W(ΦL)	Clock Pulse Width, Clock Low	170	2000	105	2000		
	t_r, t_f	Clock Rise and Fall Times		30		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		0		ns	
CS, $\overline{CE}$, etc.	t_SΦ(CS)	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	160		145		ns	
	t_DΦ(D)	Data Output Delay from Rising Edge of Φ During Read Cycle		240		200	ns	(2)
	t_SΦ(D)	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	60		50		ns	
D_0 - D_7	t_{DI}(D)	Data Output Delay from Falling Edge of $\overline{IORQ}$ During INTA Cycle		340		160	ns	(2)
	t_F(D)	Delay to Floating Bus (Output Buffer Disable Time)		230		110	ns	
IEI	t_S(IEI)	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	200		140		ns	
	t_{DH}(IO)	IEO Delay Time from Rising Edge of IEI		220		160	ns	(3)
	t_{DL}(IO)	IEO Delay Time from Falling Edge of IEI		190		130	ns	(3)
IEO	t_{DM}(IO)	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		300		190	ns	(3)
$\overline{IORQ}$	t_SΦ(IR)	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	250		115		ns	
$\overline{M1}$	t_SΦ(M1)	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle	210		90		ns	
$\overline{RD}$	t_SΦ(RD)	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		115		ns	
$\overline{INT}$	t_DΦ(IT)	$\overline{INT}$ Delay from Rising Edge of Φ		t_C(Φ) + 200		t_C(Φ) + 140		(7)
	t_C(CK)	Clock Period	2t_C(Φ)		2t_C(Φ)			(5)
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		50	ns	
	t_S(CK)	Clock Setup Time to Rising Edge of Φ for Immediate Count	210		130		ns	(5)
	t_S(TR)	Trigger Setup Time to Rising Edge of Φ for Enabling of Prescaler on Following Rising Edge of Φ	210		130		ns	(6)
CLK/ TRG_{0-3}	t_W(CTH)	Clock and Trigger High Pulse Width	200		120		ns	(7)
	t_W(CTL)	Clock and Trigger Low Pulse Width	200		120		ns	(7)

A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC (Cont'd)

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

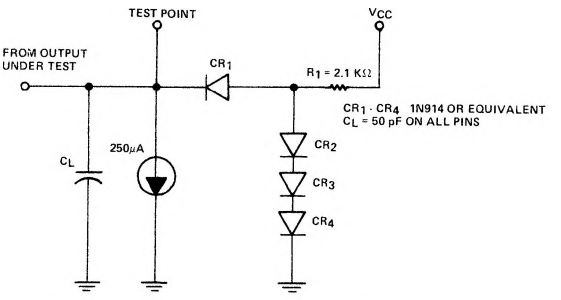
SIGNAL	SYMBOL	PARAMETER	3882 MIN	3882 MAX	3882-4 MIN	3882-4 MAX	UNIT	COMMENTS
ZC/ TO_{0-2}	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		120	ns	(7)
	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		120	ns	(7)

NOTES:

1. $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
2. Increase delay by 10 nsec for each 50 pF increase in loading 200 pF maximum for data lines and 100 pF for control lines.
3. Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum.
4. $\overline{\text{RESET}}$ must be active for a minimum of 3 clock cycles.
5. Counter mode
6. Timer mode
7. Counter and Timer mode

OUTPUT LOAD CIRCUIT

Figure 2

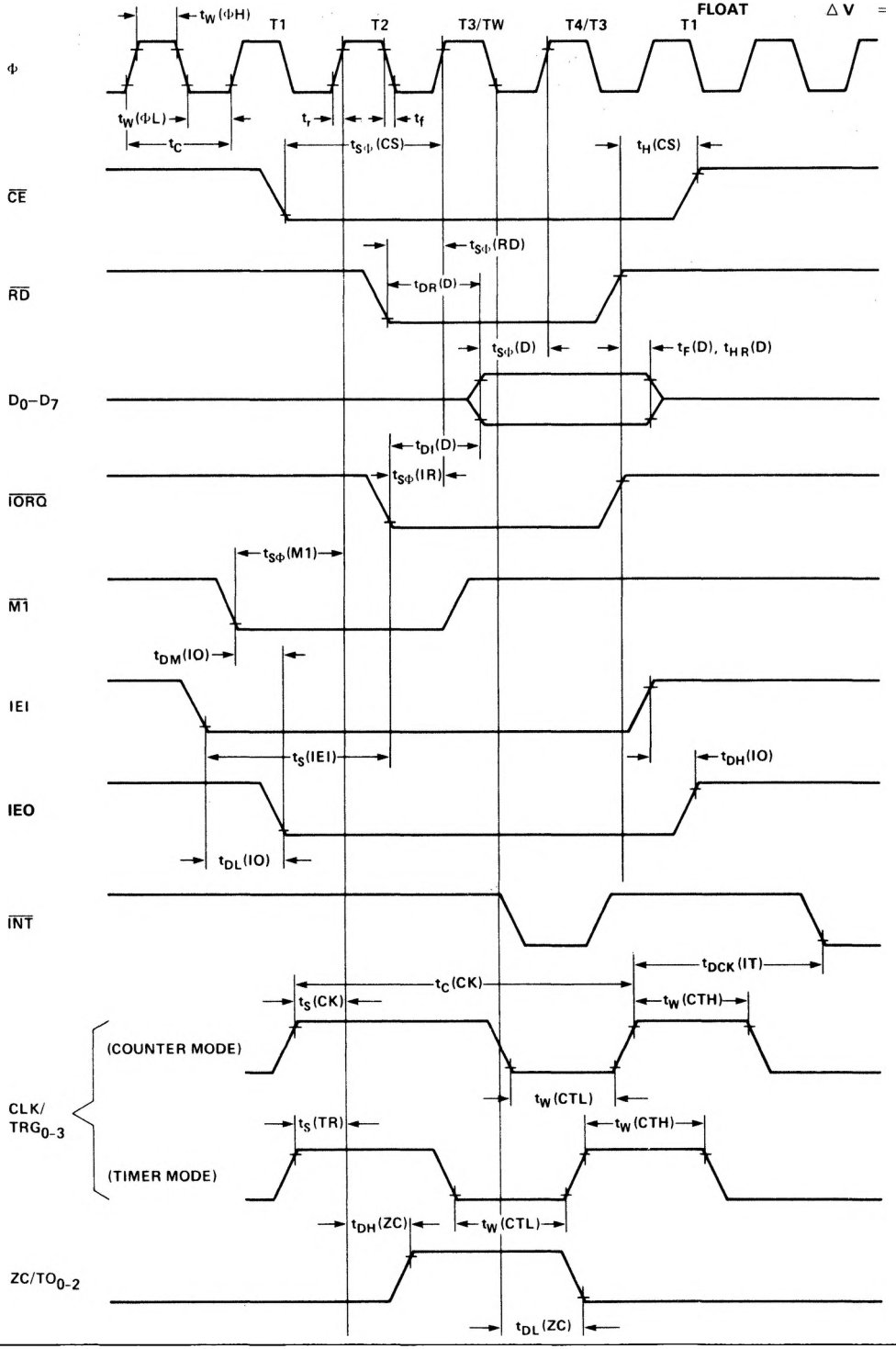


TIMING DIAGRAM

Figure 3

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	4.2 V	0.8 V
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	△ V =	0.5 V



ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3882N	Z80-CTC	Plastic	2.5 MHz	0° to 70°C
MK3882P	Z80-CTC	Ceramic	2.5 MHz	
MK3882N-4	Z80A-CTC	Plastic	4.0 MHz	
MK3882P-4	Z80A-CTC	Ceramic	4.0 MHz	
MK3882P-10	Z80-CTC	Ceramic	4.0 MHz	–40° to +85°C