MOSTEK

Z80 MICROCOMPUTER

Serial Input/Output Controller

MK3884/5/7/SIO/9

FEATURES

- One full-duplex channel, with separate control and status lines for modems or other devices
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (MK3884/5/7 Z80 SIO/9), or 0 to 800K bits/second with a 4.0 MHz clock (MK3884/5/7-4 Z80 SIO/9)
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/-checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

DESCRIPTION

The MK3884/5/7 Z80 SIO/9 Serial Input/Output Controller is a single channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications. Functionally, this device is identical to the MK3884 Z80 SIO, except that it operates in one channel only (Channel A).

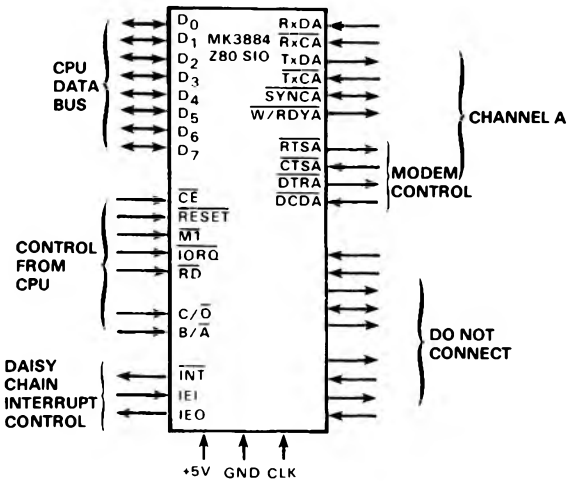
The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on one fully-independent channel, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

The Z80 SIO/9 is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a

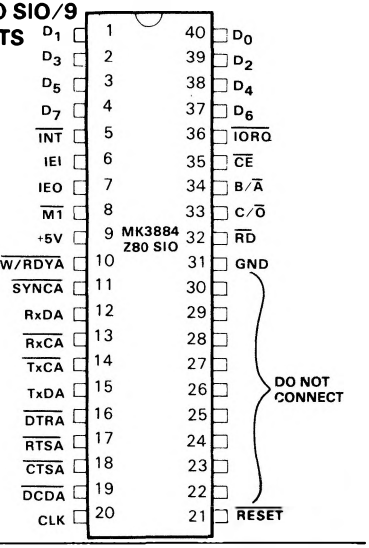
MK3884/5/7 Z80 SIO/9 PIN FUNCTIONS

Figure 1



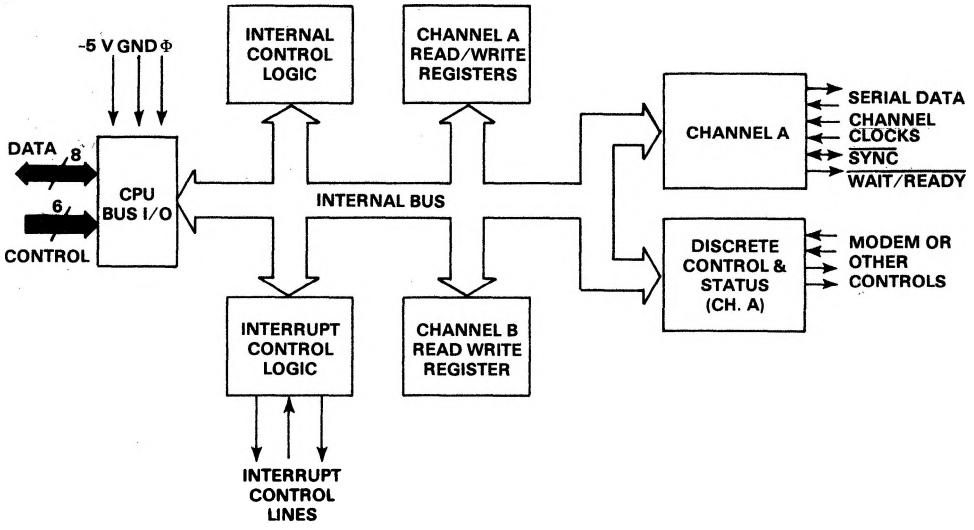
MK3884/5/7 Z80 SIO/9 PIN ASSIGNMENTS

Figure 2



Z80-SIO/9 BLOCK DIAGRAM

Figure 3



single +5V power supply and the standard Z80 family single-phase clock.

Refer to the MK3884/5/7 SIO Data Sheet and the MK3884/5/7 SIO Technical Manual for detailed functional and electrical descriptions. All functional and electrical descriptions in these publications are applicable to the SIO/9, except that Channel B cannot be used for data input or output and that pins 22 through 30 must not be connected.

Write Register 2 (Interrupt Vector) and the Status Affects Vector bit in Write Register 1 are, however, still programmed by selecting Channel B with the B/A input. All other bits in Write Register 1 or Channel B must be programmed to 0.

ORDERING INFORMATION

PART NO.	ZILOG DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3884N SIO/9	Z80 SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3884P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3884N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3884P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C
MK3885N SIO/9	Z80-SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3885P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3885N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3885P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C
MK3887N SIO/9	Z80-SIO/9	Plastic	2.5 MHz	0°C to +70°C
MK3887P SIO/9	Z80-SIO/9	Ceramic	2.5 MHz	0°C to +70°C
MK3887N-4 SIO/9	Z80A-SIO/9	Plastic	4 MHz	0°C to +70°C
MK3887P-4 SIO/9	Z80A-SIO/9	Ceramic	4 MHz	0°C to +70°C

NOTE: Refer to the section on pin descriptions for explanation of the differences between the MK3884, MK3885, and MK3887 SIO/9.