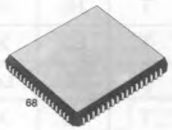
SGS-THOMSON MICROELECTRONICS

MK4202(Q)-20

2048 × 20 CMOS TAGRAM™

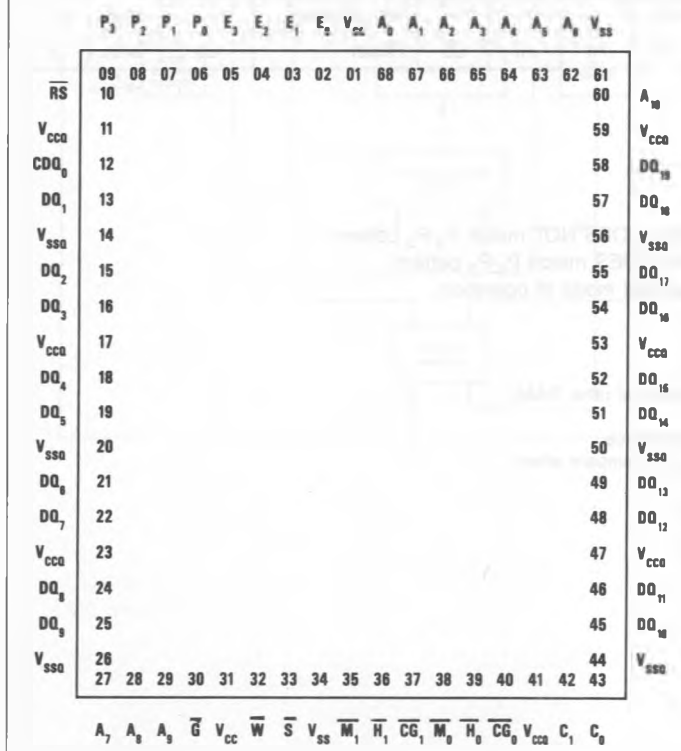
ADVANCED DATA

- 2048 x 20 CMOS SRAM WITH ONBOARD COMPARATOR
- MATCH ACCESS TIME = 20ns (MAX)
- READ ACCESS TIME = 25ns (MAX)
- RESET CYCLE = 25ns (MAX)
- I_{CC} (OUTPUTS DESELECTED) = 225mA (MAX)
- STANDBY = 70mA (MAX)
- FLASH CLEAR VALID BIT FUNCTION
- TARGET APPLICATION: 68020-25, 68030-33 AND 80386 CACHE



Q
PLCC68
(Plastic Chip Carrier)

FIGURE 1. PINOUT FOR 68 PIN PLCC PACKAGE (PRELIMINARY)



PIN NAMES

V_{CC}, V_{SS}	+5 Volt Supply, Ground
V_{CCQ}, V_{SSQ}	+5 Volt Output Supply, Output Ground
A_0-A_{10}	Index Address Input
CDQ_0	Clearable Tag Data I/O
DQ_1-DQ_{19}	Tag Data I/O
E_0-E_3	Chip Enable (Programmable Active Low or High)
P_0-P_3	Chip Enable Program Inputs
$\overline{RS}$	Reset Input (Active Low)
$\overline{S}$	Chip Select Input (Active Low)
$\overline{W}$	Write Enable (Active Low)
$\overline{G}$	Data Output Enable (Active Low)
C_0	Compare 0 Output (3-State) Hit = High, Miss = Low
C_1	Compare 1 Output (3-State) Hit = High, Miss = Low
$\overline{H_0}$	Force Hit 0 Input (Active Low)
$\overline{H_1}$	Force Hit 1 Input (Active Low)
$\overline{M_0}$	Force Miss 0 Input (Active Low)
$\overline{M_1}$	Force Miss 1 Input (Active Low)
$\overline{CG_0}$	Compare 0 Output Enable (Active Low)
$\overline{CG_1}$	Compare 1 Output Enable (Active Low)

TRUTH TABLE

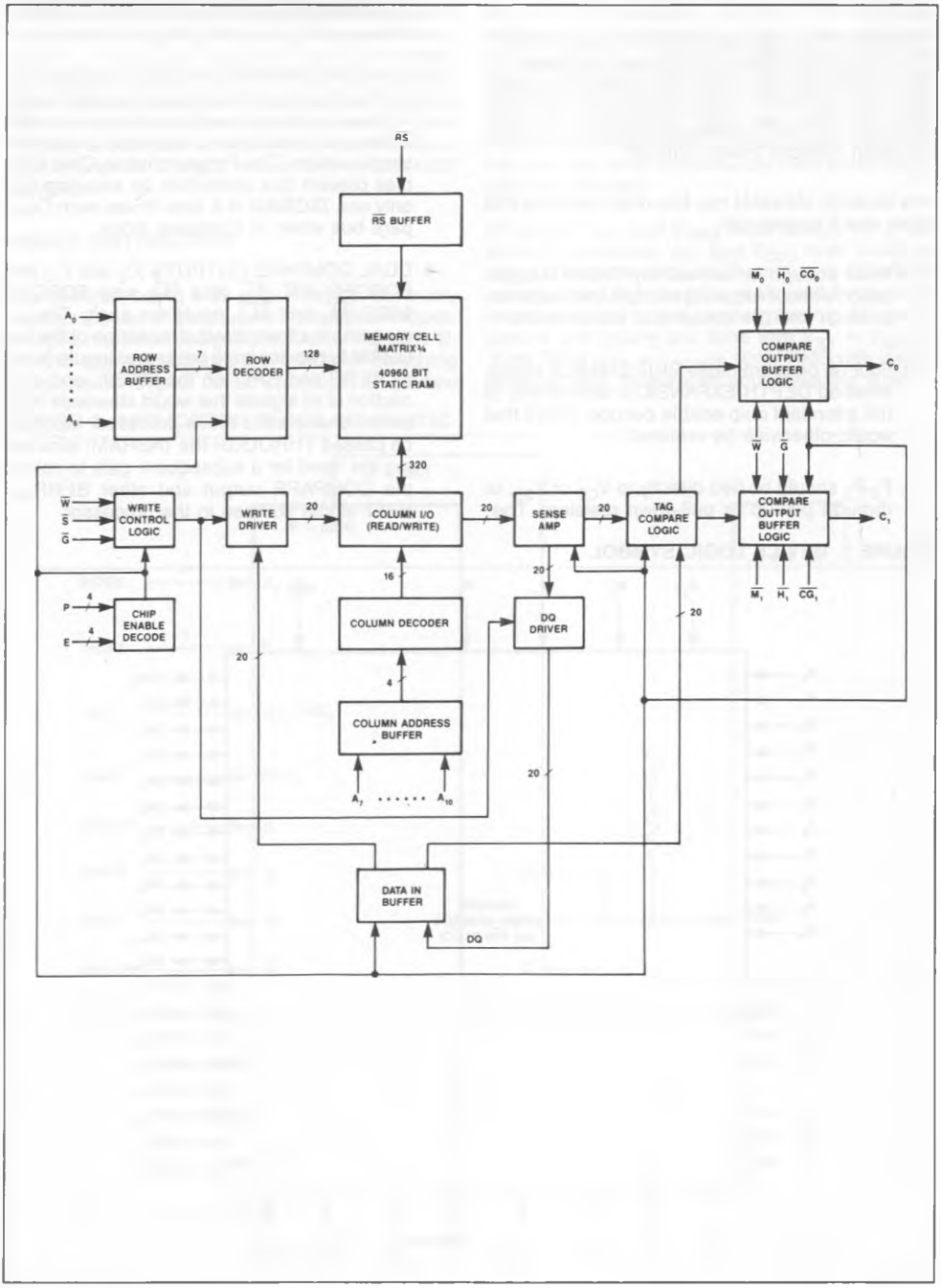
$\overline{RS}$	$\overline{S}$	E	$\overline{W}$	$\overline{G}$	$\overline{M_X}$	$\overline{H_X}$	$\overline{CG_X}$	MODE	C_X	DQ	NOTES
Hi	—	X	—	—	Lo	X	X	Force Miss	Low	—	1
Hi	—	X	—	—	Hi	Lo	X	Force Hit	High	—	1
Hi	—	X	—	—	Hi	Hi	Hi	Comp Disable	Hi-Z	—	1
Hi	X	F	X	X	Hi	Hi	X	Standby	Hi-Z	Hi-Z	
Hi	X	T	Hi	Hi	Hi	Hi	Hi	Compare	Hi-Z	D in	
Hi	X	T	Hi	Hi	Hi	Hi	Lo	Compare	Hi or Lo	D in	
Hi	Hi	T	Lo	X	Hi	Hi	Lo	Hit	High	Hi-Z	
Hi	Hi	T	X	Lo	Hi	Hi	Lo	Hit	High	Hi-Z	
Hi	Lo	T	Lo	X	Hi	Hi	Lo	Write	High	D in	
Hi	Lo	T	Hi	Lo	Hi	Hi	Lo	Read	High	D Out	
Lo	Hi	X	X	X	—	—	—	Reset	—	Hi-Z	
Lo	X	F	X	X	—	—	—	Reset	—	Hi-Z	
Lo	X	X	Hi	Hi	—	—	—	Reset	—	Hi-Z	
Lo	X	X	Hi	Lo	—	—	—	Reset	—	Lo-Z	
Lo	Lo	T	Lo	X	—	—	—	Not Allowed	—	Hi-Z	2
Lo	X	T	Hi	Hi	Hi	Hi	Lo	Reset	Lo	D in	3

Key: X = Don't Care
$\overline{H_X}$ = $\overline{H_0}$ or $\overline{H_1}$
$\overline{M_X}$ = $\overline{M_0}$ or $\overline{M_1}$
$\overline{CG_X}$ = $\overline{CG_0}$ or $\overline{CG_1}$
F = (False) E_0-E_3 pattern DOES NOT match P_0-P_3 pattern.
T = (True) E_0-E_3 pattern DOES match P_0-P_3 pattern.
— = Not related to identified mode of operation.

NOTES

1. Force hit/miss operations independent of other RAM operations.
2. May disrupt Reset, will not damage device.
3. Reset will force C_X low during a valid compare when CDQ_0 is D in = Hi.

FIGURE 2. MK4202 BLOCK DIAGRAM



DEVICE DESCRIPTION AND FEATURES

The MK4202 is designed to be connected DIRECTLY to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting HIT or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.

The MK4202 TAGRAM has four major features that allow direct connection:

1. Wide enough for almost any TAGRAM application without requiring multiple chip width expansion and the delays that would result.

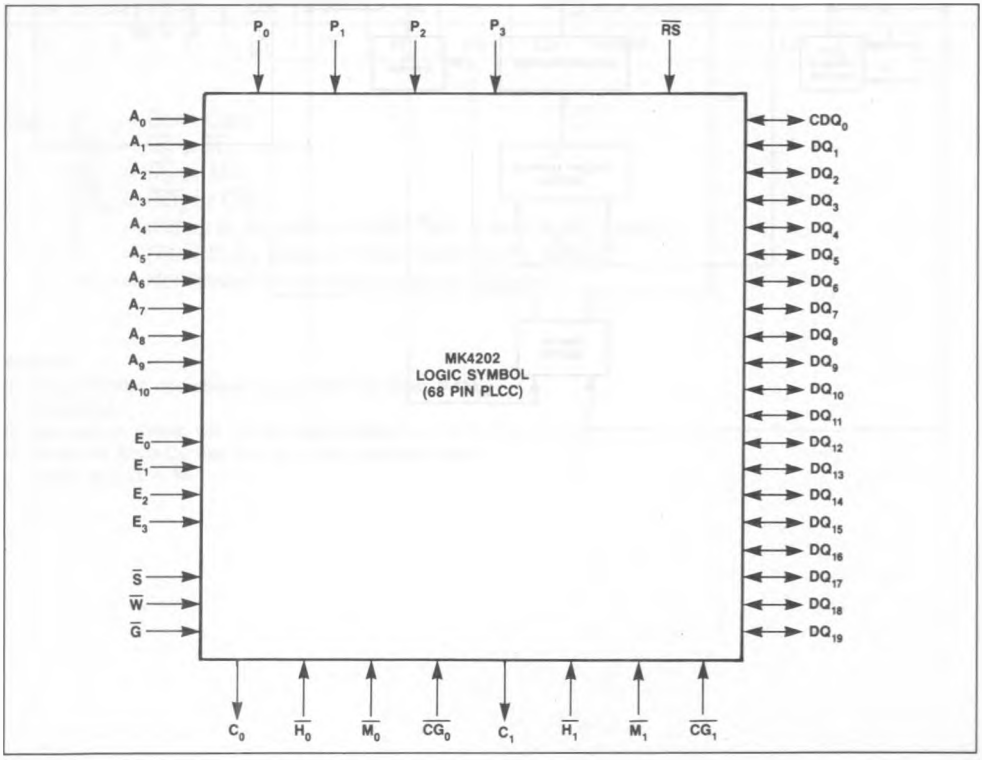
2. Four (4) programmable CHIP ENABLE inputs, allowing DEPTH EXPANSION without any of the attendant chip enable decode delays that would otherwise be required.

   P_0-P_3 should be tied directly to V_{CC} or V_{SS}, or through pull-up or pull-down resistors. The MK4202 is selected when E_0-E_3 equals P_0-P_3 in a binary match.
   (Example: E_0-E_1 = 0110, P_0-P_3 = 0110.)

3. 3-STATE COMPARE OUTPUTS, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The Programmable Chip Enables prevent bus contention by assuring that only one TAGRAM at a time drives each Compare bus when in Compare mode.

4. DUAL COMPARE OUTPUTS (C_0 and C_1) and FORCED HIT ($\overline{H_0}$ and $\overline{H_1}$) and FORCED MISS ($\overline{M_0}$ and $\overline{M_1}$) inputs for each. The arrangement allows direct connection of the TAGRAM to two separate processor inputs (such as BERR and HALT on the 68030), and connection of all signals that would otherwise have been connected to those processor inputs to be passed THROUGH the TAGRAM; eliminating the need for a subsequent gate to collect the COMPARE output and other BERR or HALT signal sources to the processor.

FIGURE 3. DEVICE LOGIC SYMBOL



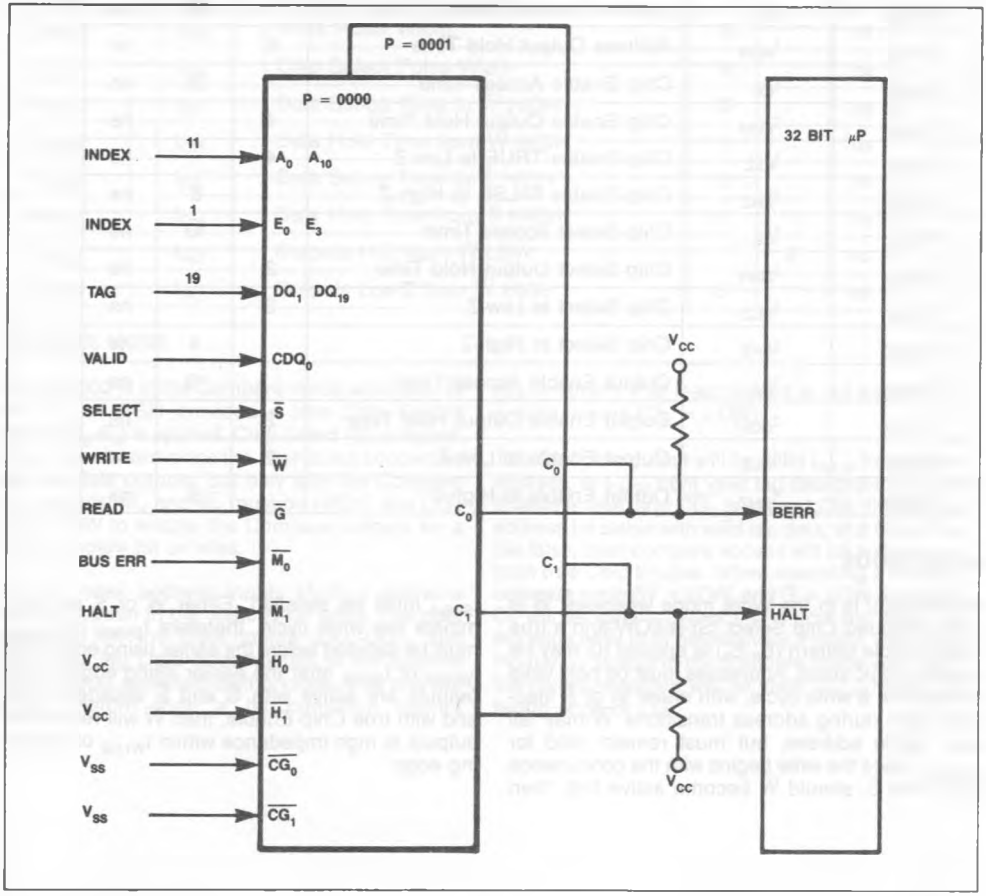
The net effect is that the Address-to-Compare access time demonstrated by the MK4202 is all of the delay the user must consider. The alternative approach, using narrow TAGRAMs with open collector outputs or narrow TAGRAMs with 2-state outputs and a 10ns programmable logic device, requires that the narrow TAGRAMs demonstrate a 10ns Address-to-Compare access time to yield the same performance in a user's system that the MK4202 provides.

POWER DISTRIBUTION

The MK4202, being a 20 output device, obviously requires the use of good power bussing techniques. MK4202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and V_{SS} lines to the output drivers. The advantage provided by these separate power pins,, designated V_{CCQ} and V_{SSQ}, is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particularly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course V_{SS} and V_{SSQ} must always be at the same DC potential. V_{CC} and V_{CCQ} must match as well. Differences between them due to AC effects are expected, but must be minimized through the use of adequate bussing and bypassing. All specifications and testing are done with $V_{SS} = V_{SSQ} \pm$ 10mV RMS, $V_{CC} = V_{CCQ} \pm$ 10mV RMS with instantaneous peak differences not exceeding 50mV.

FIGURE 4. APPLICATION BLOCK SCHEMATIC



READ MODE

The MK4202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied. The 11 address inputs (A_0-A_{10}) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will be measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E_0-E_3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

READ CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVAV}	t_C	Cycle Time	25		ns	
t_{AVQV}	t_{AA}	Address Access Time		25	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		ns	
t_{EVQV}	t_{EA}	Chip Enable Access Time		25	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		ns	
t_{ELQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		ns	
t_{EHQZ}	t_{EHZ}	Chip Enable FALSE to High-Z		8	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		10	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		10	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to High-Z		5	ns	

WRITE MODE

TheMK4202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable address, but must remain valid for t_{WLWH}. Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge, and t_{WHDX} or t_{SHDX} after the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLHZ} of its falling edge.

WRITE CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVAV}	t_C	Cycle Time	25		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time to $\overline{S}$ LOW	0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	5		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	5		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold Time to $\overline{S}$ HIGH	0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	15		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	10		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	10		ns	
t_{SHDX}	t_{DH}	Data Hold Time from $\overline{S}$ HIGH	0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW		8	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5		ns	

COMPARE MODE

The MK4202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable pattern (E_0-E_3) is applied. Chip Select ($\overline{S}$) is regarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C_X) outputs. $\overline{M}_X$ and $\overline{H}_X$ must be HIGH, and CG_X active LOW to enable the Compare outputs for a valid compare hit or miss.

The 11 index address inputs (A_0-A_{10}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_1-DQ_{19} and CDQ_0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C_X = HIGH). If at least one bit is not equal, then a miss occurs (C_X = LOW).

The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and $\overline{CG}_X$ is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), C_X will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively. Finally, when gating the C_X output in the compare mode with $\overline{CG}_X$, the compare output will be valid $t_{CGL\text{-}CV}$ from the falling edge of $\overline{CG}_X$.

COMPARE CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVCV}	t_{ACA}	Address Compare Access Time		20	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Access Time		16	ns	
t_{DXCX}	t_{DCH}	Tag Data Compare Hold Time	2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10	ns	
t_{WHCX}	t_{WCOH}	$\overline{W}$ Compare Output Hold Time	3		ns	
t_{WLCX}	t_{WCLZ}	$\overline{W}$ to Compare Low-Z	3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		8	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ LOW to Compare HIGH		10	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	3		ns	
t_{GLCX}	t_{GCLZ}	$\overline{G}$ to Compare Low-Z	3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		8	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		20	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare High-Z		8	ns	
t_{CGL-CV}	t_{CGA}	$\overline{CG_X}$ to Compare Access Time		8	ns	
t_{CGH-CX}	t_{CGOH}	$\overline{CG_X}$ Compare Hold Time	2		ns	
t_{CGL-CX}	t_{CGLZ}	$\overline{CG_X}$ LOW to Compare Low-Z	2		ns	
t_{CGH-CZ}	t_{CGHZ}	$\overline{CG_X}$ HIGH to Compare High-Z		8	ns	

NOTE: E = Enable Inputs (E_0-E_3).

RESET MODE

The MK4202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ_0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to ensure a valid compare miss or hit condition. It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins: Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic (1), then $\overline{C_X}$ will go LOW at t_{RSL-CL} from the falling edge of $\overline{RS}$.

RESET CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$t_{RLSL-AV}$	t_{RSC}	Reset Cycle Time	25		ns	
$t_{RSL-RSH}$	t_{RSW}	Reset Pulse Width	25		ns	
t_{RSL-CL}	t_{RSCL}	$\overline{RS}$ LOW to Compare Output LOW		25	ns	
t_{RSH-AV}	t_{RSR}	Address Recovery Time	0		ns	
t_{RSH-EV}	t_{RSR}	Chip Enable Recovery Time	0		ns	

FORCE HIT AND FORCE MISS

The MK4202 can force either a miss or hit condition on the C_X output by asserting $\overline{M_X}$ or $\overline{H_X}$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enable ($\overline{CG_X}$) (see truth table). The C_X output will go HIGH within t_{HLCH} from the falling edge of $\overline{H_X}$, or C_X will go LOW within t_{MLCL} from the falling edge of $\overline{M_X}$. All $\overline{M_X}$ and $\overline{H_X}$ inputs must be HIGH during a valid compare cycle.

FORCE HIT OR MISS CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{HLCH}	t_{HA}	$\overline{H_X}$ to Force Hit Access Time		8	ns	
t_{HHCZ}	t_{HHZ}	$\overline{H_X}$ to Compare High-Z		5	ns	
t_{HL-CGX}	t_{HS}	Force Hit to $\overline{CG_X}$ Don't Care	2		ns	
t_{HH-CGH}	t_{HR}	Force Hit to $\overline{CG_X}$ Recognized	2		ns	
t_{MLCL}	t_{MA}	$\overline{M_X}$ to Force Miss Access Time		8	ns	
t_{MHCZ}	t_{MHZ}	$\overline{M_X}$ to Compare to High-Z		5	ns	
t_{ML-CGX}	t_{MS}	Force Miss to $\overline{CG_X}$ Don't Care		2	ns	
t_{MH-CGH}	t_{MR}	Force Miss to $\overline{CG_X}$ Recognized	2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{H_X}$ Don't Care	2		ns	
t_{MHHH}	t_{MHR}	Force Miss To $\overline{H_X}$ Recognized	2		ns	

FIGURE 5. $\overline{W}$ WRITE CYCLE

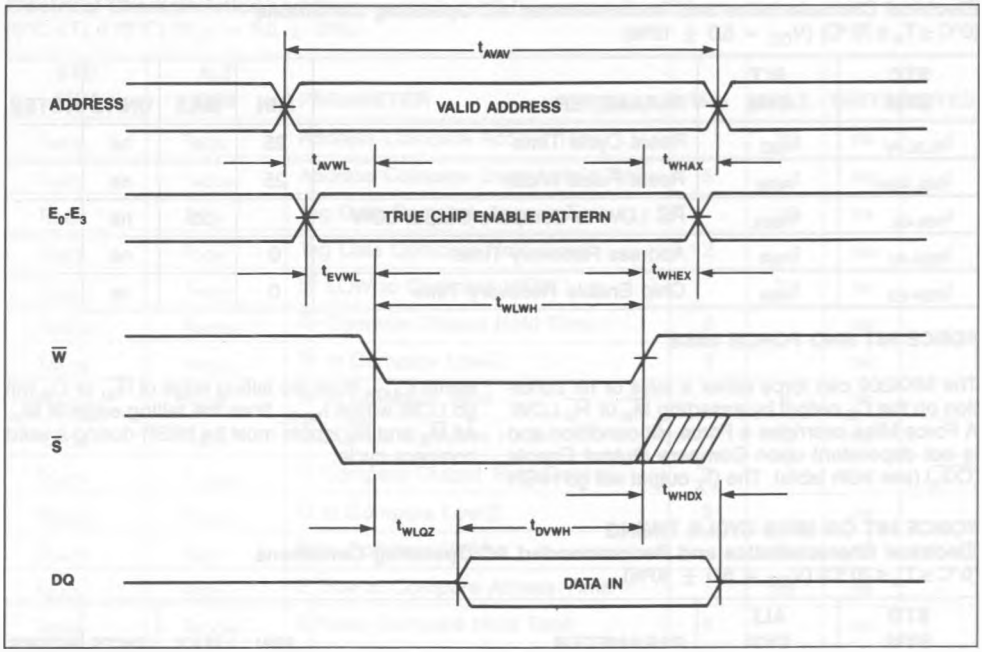


FIGURE 6. $\overline{S}$ WRITE CYCLE

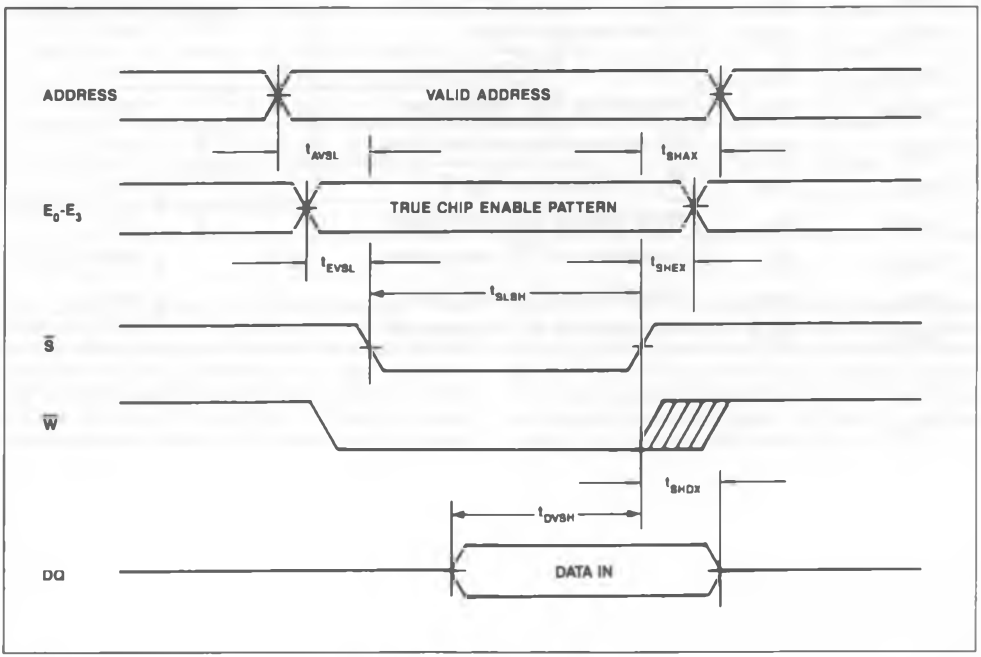


FIGURE 7. READ CYCLE

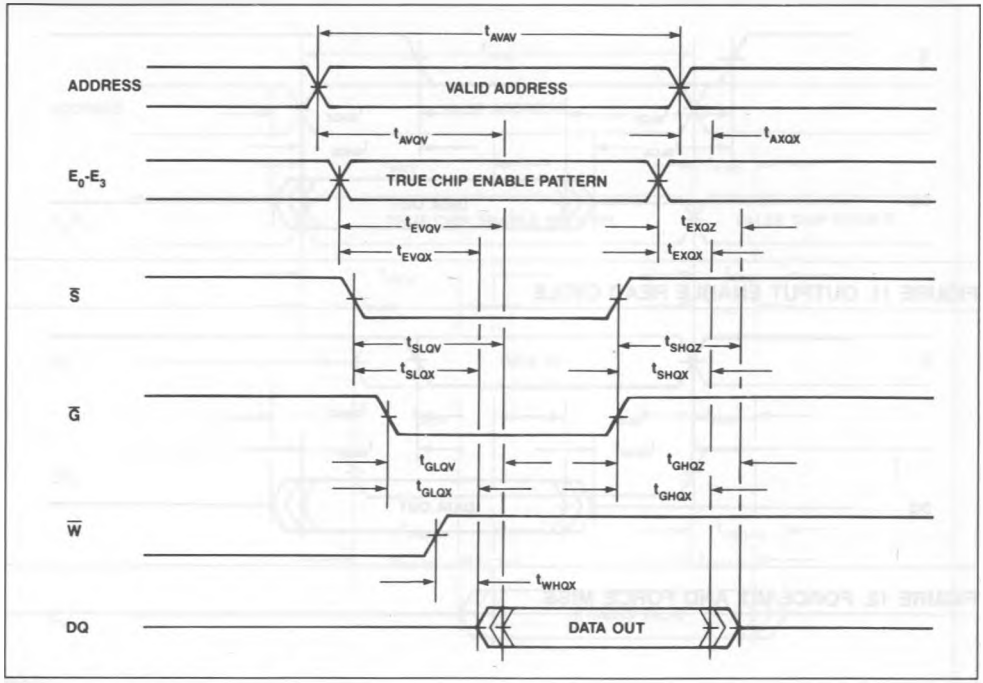


FIGURE 8. ADDRESS READ CYCLE

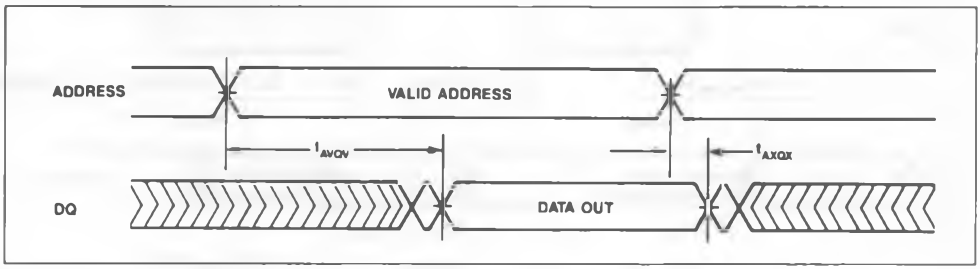


FIGURE 9. CHIP ENABLE READ CYCLE

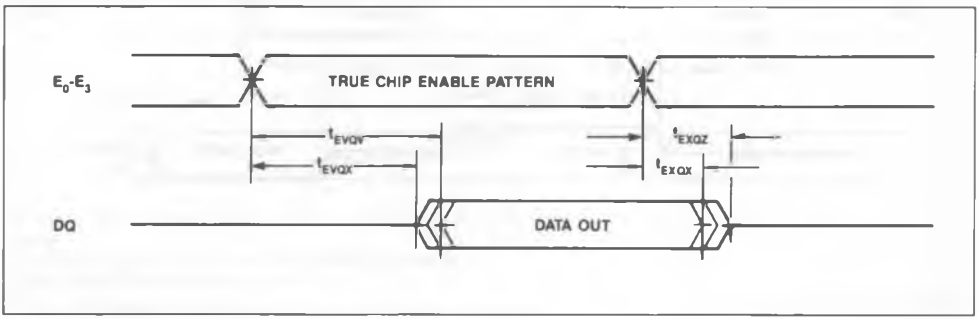


FIGURE 10. CHIP SELECT READ CYCLE

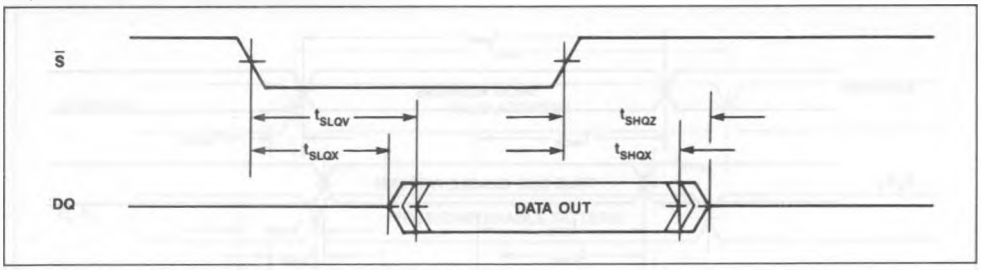


FIGURE 11. OUTPUT ENABLE READ CYCLE

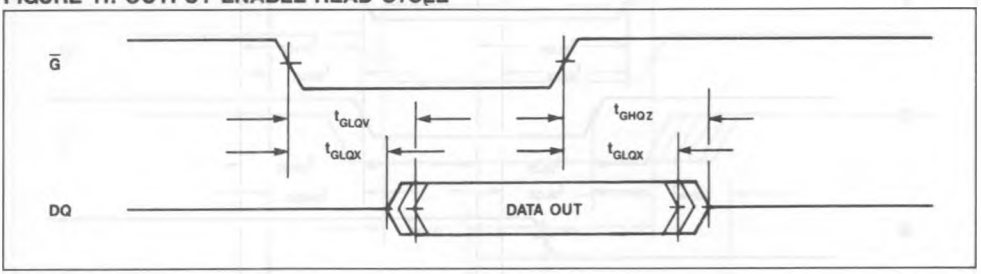


FIGURE 12. FORCE HIT AND FORCE MISS

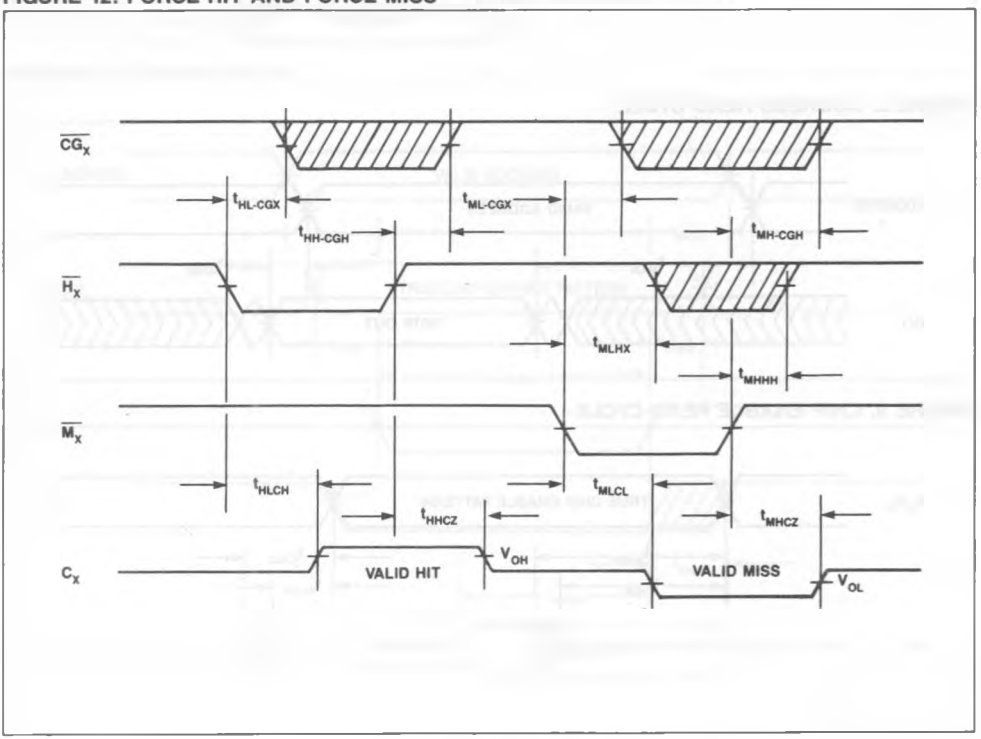
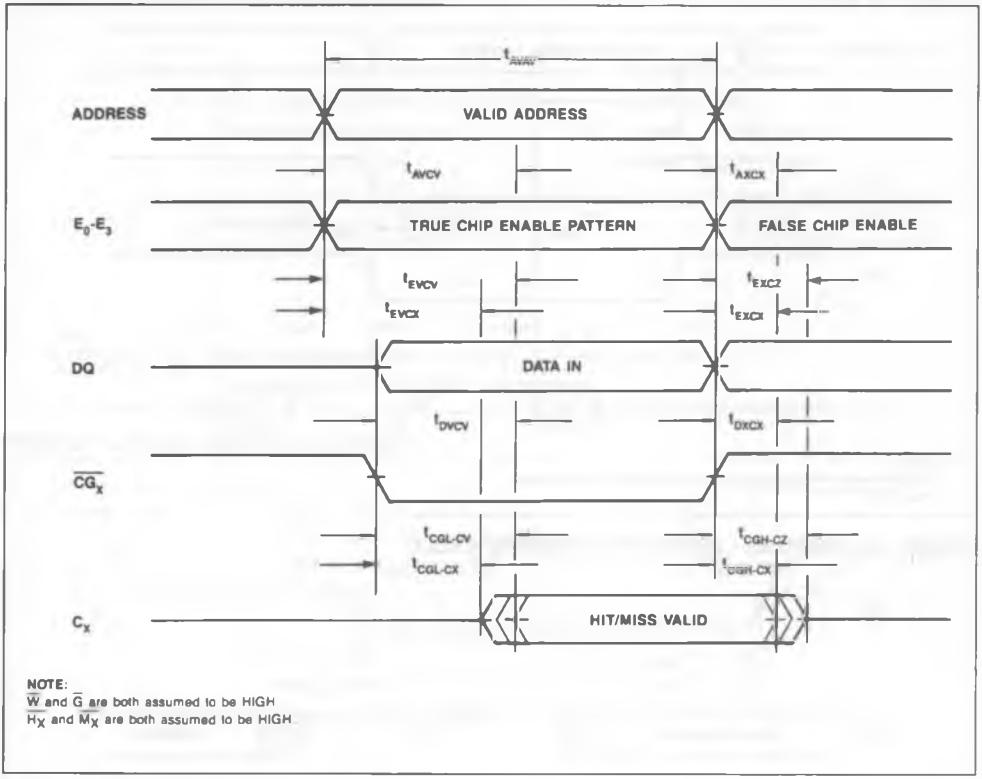
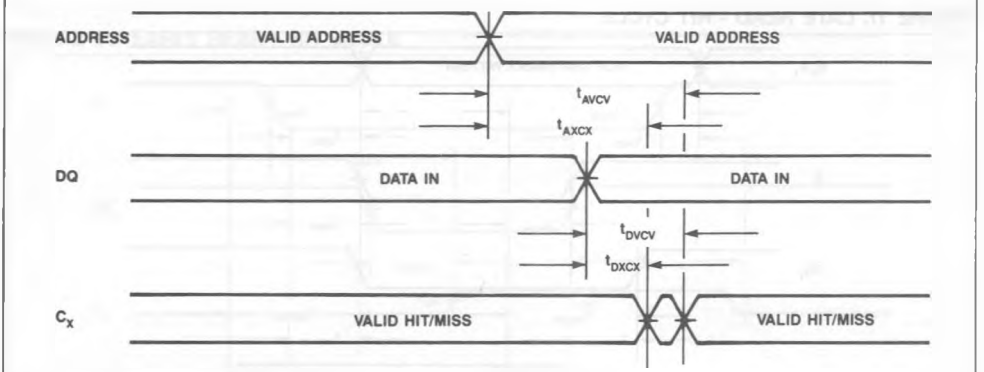


FIGURE 13. SUMMARY COMPARE CYCLE



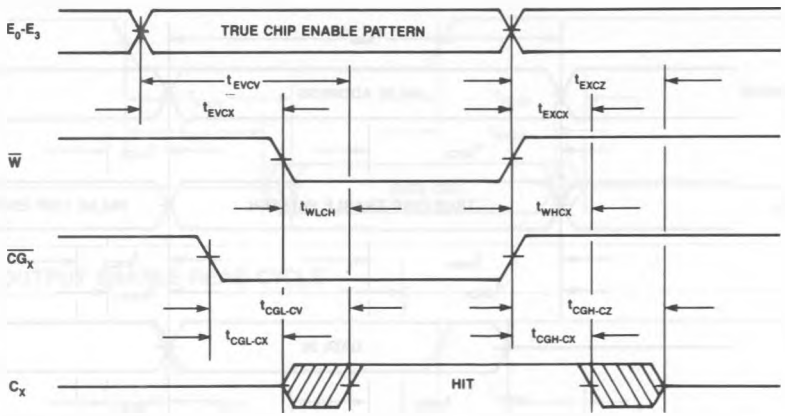
NOTE:
$\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.
H_X and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 14. COMPARE CYCLE



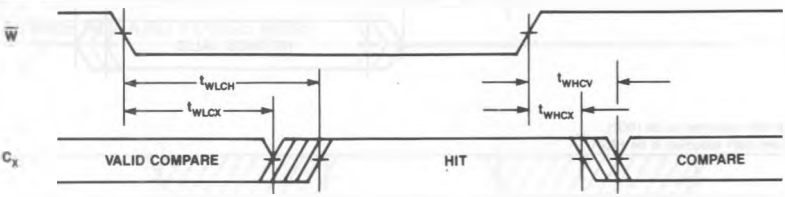
NOTE:
$\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CG_X}$ is LOW, and a true Chip Enable pattern is present. H_X and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 15. LATE WRITE - HIT CYCLE



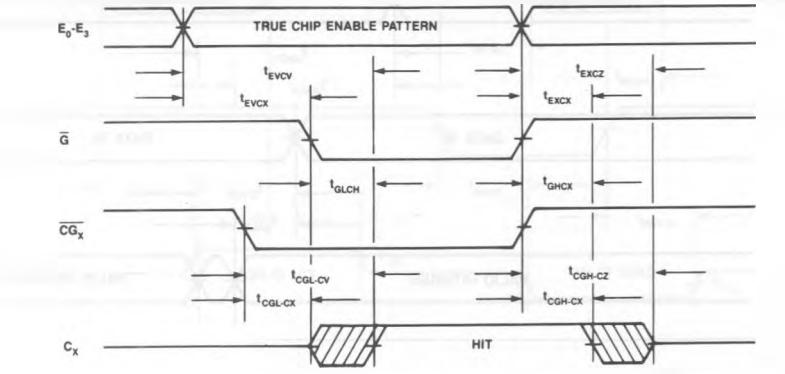
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 16. COMPARE - WRITE HIT - COMPARE CYCLE



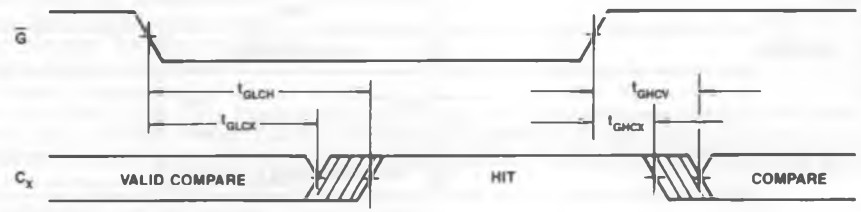
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH, with $\overline{CG_X}$ LOW

FIGURE 17. LATE READ - HIT CYCLE



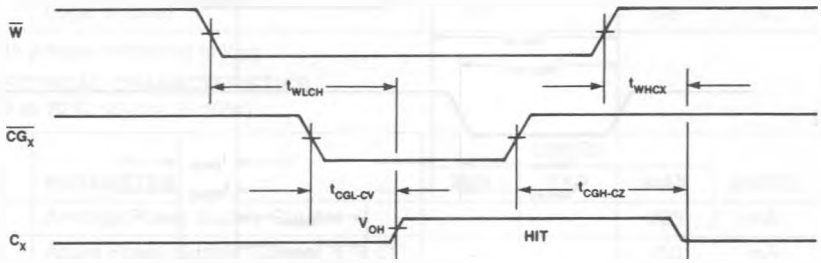
NOTE:
$\overline{W}$ is HIGH and a Valid Address is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH

FIGURE 18. COMPARE - READ HIT - COMPARE CYCLE



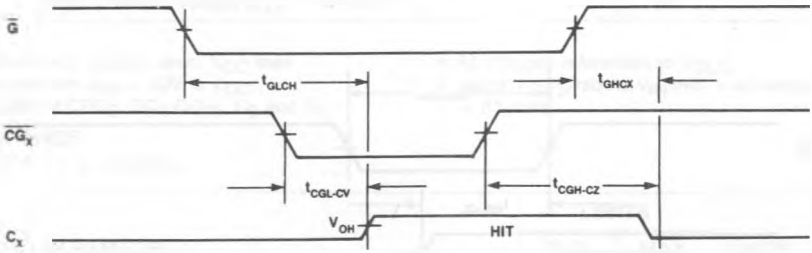
NOTE:
$\overline{W}$ is HIGH and a Valid Address is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH with $\overline{CG_X}$ LOW

FIGURE 19. EARLY WRITE - HIT CYCLE



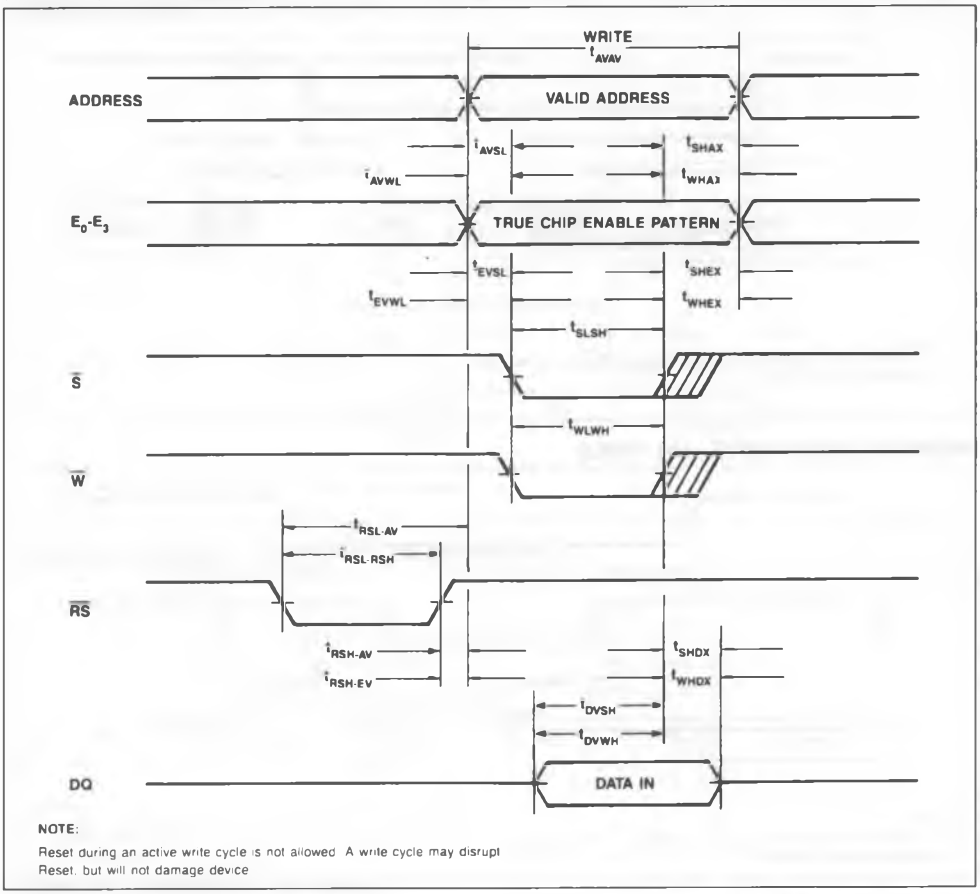
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present with (E_0-E_3) True $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH

FIGURE 20. EARLY READ - HIT CYCLE



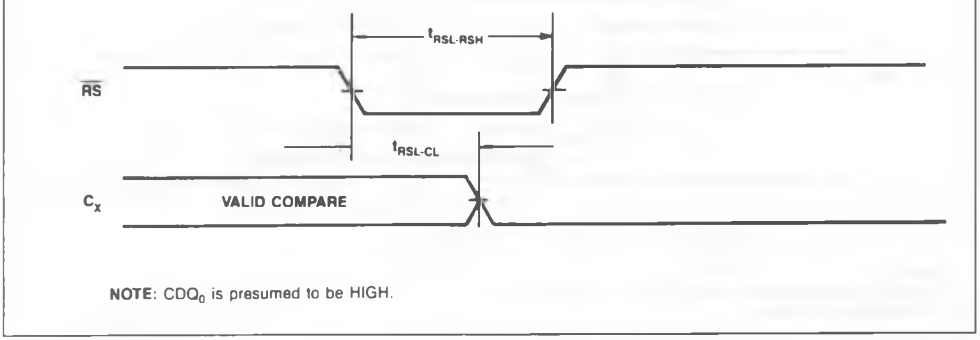
NOTE:
$\overline{W}$ is HIGH and a Valid Address is present, with (E_0-E_3) = True $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 21. RESET CYCLE



NOTE:
Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage device

FIGURE 22. VALID COMPARE - RESET



NOTE: CDQ_0 is presumed to be HIGH.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1.5 to 7.0 volts
Ambient Operating Temperature (T_A) . . . . . 0 to 70°C
Ambient Temperature under Bias . . . . . −55°C to 125°C
Ambient Storage Temperature (Plastic) . . . . . −55°C to 125°C
Total Device Power Dissipation . . . . . 2.5 Watts
RMS Output Current per Pin 25mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Input	2.2		V_{CC}+0.3	V	5
V_{IL}	Logic 0 Input	−0.3		0.8	V	5

NOTE: All voltages referenced to V_{SS}.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = ± 10%)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
I_{CC}	Average Power Supply Current			225	mA	1
I_{CCA}	Active Power Supply Current (f = 0)			150	mA	1
I_{CCD}	Dynamic Power Supply Current per MHz			1.2	mA/MHz	1
I_{SB1}	TTL Standby Current			70	mA	1
I_{IL}	Input Leakage Current	−1		+1	µA	2
I_{OL}	Output Leakage Current	−10		+10	µA	3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = −4mA)	2.4			V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)			0.4	V	4

NOTES

1. Measured with outputs open. V_{CC} max.
2. Measured with V_{IN} = 0.0V to V_{CC}.
3. Measured at CDQ_0, DQ_1-DQ_{19}, C_0 and C_1.
4. All voltages referenced to V_{SSQ}.
5. Inputs (P_0-P_3) require V_{IH} min. = 4.5 volts and V_{IL} max. = 0.5 volts.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	LIMITS		UNITS	NOTE
		TYP	MAX		
C_I	Input Capacitance	4	4	pf	1
C_O	Output Capacitance	8	10	pf	1,2

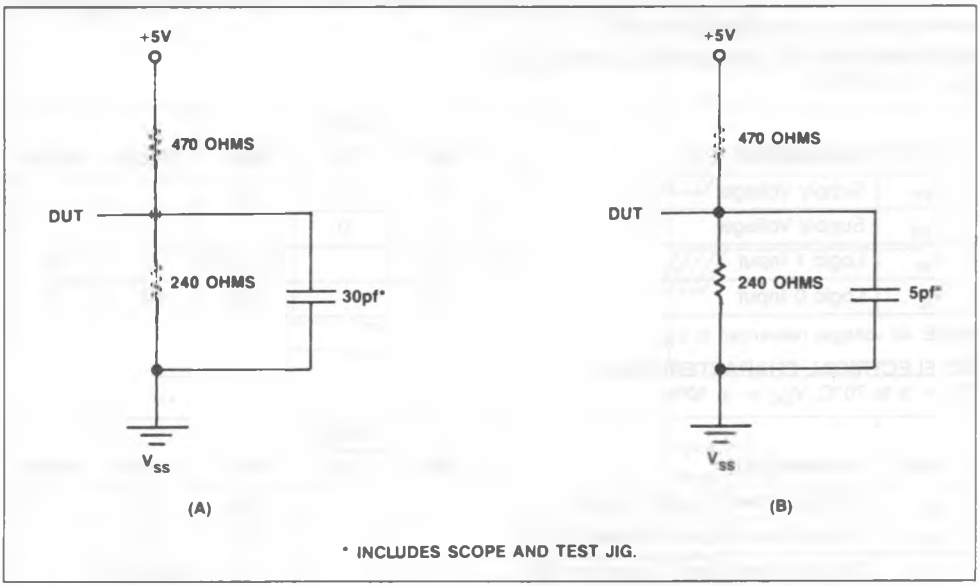
NOTES

1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data I/O's, C0 and C1.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0° to 70°C
V_{CC}	5.0 Volts ± 10%

FIGURE 23. EQUIVALENT OUTPUT LOAD CIRCUIT



ORDERING INFORMATION

PART NUMBER	ACCESS TIME	CYCLE TIME	PACKAGE TYPE	TEMPERATURE
MK4202(Q)-20	20ns	25ns	68 pin PLCC	0°C to 70°C

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