SGS-THOMSON MICROELECTRONICS

MK44S80(N,X) -15/17/20

65,536-BIT FAST CMOS 16 K X 4 CACHE TAGRAM™

ADVANCE DATA

FEATURES

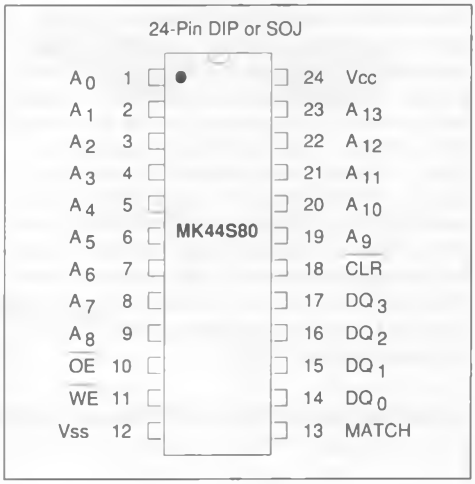
- 16K x 4 FAST CMOS CACHE TAGRAM
- 15,17,20ns ADDRESS TO COMPARE ACCESS
- 10,12,14ns TAG DATA TO COMPARE ACCESS
- EQUAL ACCESS, READ/WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 24-PIN 300 MIL STANDARD PLASTIC DIP

DESCRIPTION

The MK44S80 is a 65,536-bit CMOS Static TAGRAM, organized as 16Kx4 using SGS-THOMSON Microelectronics' advanced fast HCMOS process technology. This device is functionally compatible with the industry standard MK41S80 4Kx4 TAGRAM. All inputs and outputs are TTL compatible using a single 5V supply.

The MK44S80 provides full static operation, requiring no external clocks or refresh operations, and features a MATCH output for indicating either a cache hit or miss condition. The on-board 4-bit comparator compares RAM contents with current input (tag) data. The result on the MATCH pin is an active high match ("hit"), or active low for a "miss" condition. The MK44S80 offers a totem-pole MATCH output design for fast access times, allowing the MATCH pins of several devices to be gated together to provide an enable or acknowledge to the data cache or cache control logic (refer to Figure 2).

PIN CONNECTION



MK44S80 TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Compare
L	X	H	Invalid	Write
H	L	H	Invalid	Read
X	X	L	Invalid	Clear

PIN NAMES

A_0-A_{13}	Address Inputs
DQ_0-DQ_3	Data I/O_{0-3}
MATCH	Comparator Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CLR}$	Ram Flash Clear
Vcc,Vss	+5V, GND

TAGRAM FUNCTION

The MK44S80 is an SRAM based Cache Tag directory (hence the name TAGRAM). Figure 2 shows a general block diagram using a cache tag directory (TAGRAM) in a cache subsystem application. The system must detect whether the requested data resides in the cache data RAM, or if extended read cycles to main memory are necessary.

The MK44S80 features four modes of operation: Write, Read, Compare, and Clear. The MK44S80 incorporates an on-board 4 bit comparator that compares internal RAM contents with current (tag) input data. If the device is in the compare mode, and the comparator detects a "match", then the MATCH pin will go high for a hit condition. If a match is not detected by the comparator, then the MATCH pin drives low to denote a "miss" condition. Standard write/read operations are performed with Write ($\overline{WE}$) and Output ($\overline{OE}$) Enable inputs. Additionally, the device provides a Flash Clear operation via the $\overline{CLR}$ pin.

When a low level (V_{IL}) is applied to the $\overline{CLR}$ input pin for the specified t_{CLP} time, all RAM bits are set to a logic zero.

Compare data (internal RAM) can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0 - DQ_3).

GENERAL CACHE SUB SYSTEM BLOCK DIAGRAM