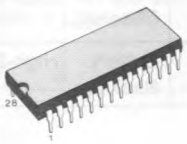
SGS-THOMSON MICROELECTRONICS

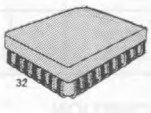
MK48C02A/12A(K,N) -15/20/25

2K × 8 ZEROPOWER™ RAM

- LOW CURRENT (1 μA @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440 mW ACTIVE; 5.5 mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48C02A $4.75V \geq V_{PFD} \geq 4.50V$
  MK48C12A $4.50V \geq V_{PFD} \geq 4.20V$
- POWER FAIL INTERRUPT OUTPUT



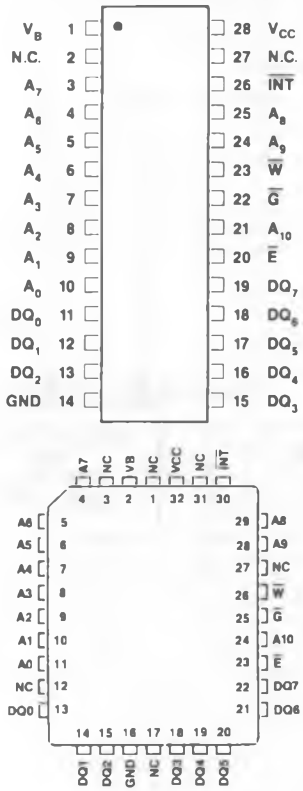
N
DIP-28
(Plastic Package)



K
PLCC32
(Plastic Chip Carrier)

Part Number	Access Time	R/W Cycle Time
MK48CX2A-15	150 ns	150 ns
MK48CX2A-20	200 ns	200 ns
MK48CX2A-25	250 ns	250 ns

FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{10} Address Inputs	V_{CC} System Power (+5 V)
$\overline{E}$ Chip Enable	$\overline{W}$ Write Enable
GND Ground	$\overline{G}$ Output Enable
DQ_0-DQ_7 Data In/Data Out	V_B Battery Input
$\overline{INT}$ Power Fail Interrupt (Open Drain Type)	
NC No Connection	

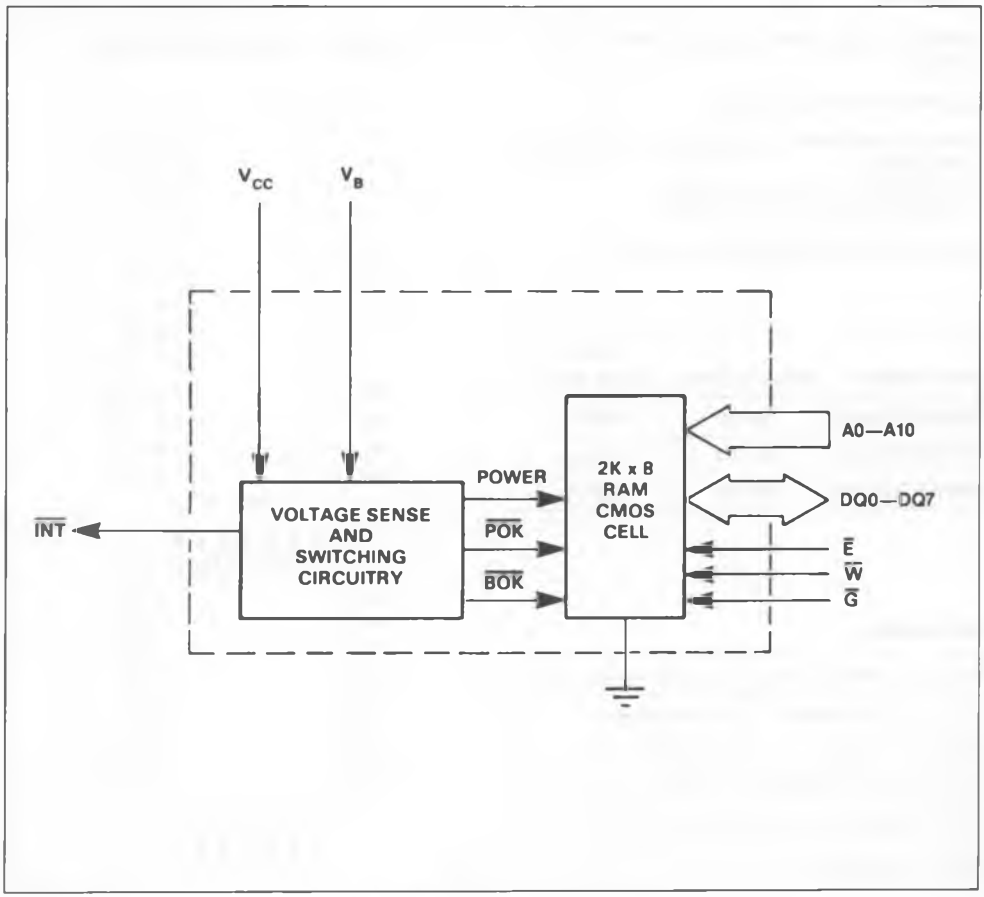
TRUTH TABLE (MK48C02A/12A)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
	V_{IH}	X	X	Deselect	High-Z
$<V_{CC}$ (Max)	V_{IL}	X	V_{IL}	Write	D_{IN}
$>V_{CC}$ (Min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD}$ (Min) $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

DESCRIPTION

The MK48C02A/12A is a CMOS RAM with internal power fail support circuitry for battery backup applications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V_{CC} falls out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V_{CC} below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5na) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

FIGURE 2. BLOCK DIAGRAM



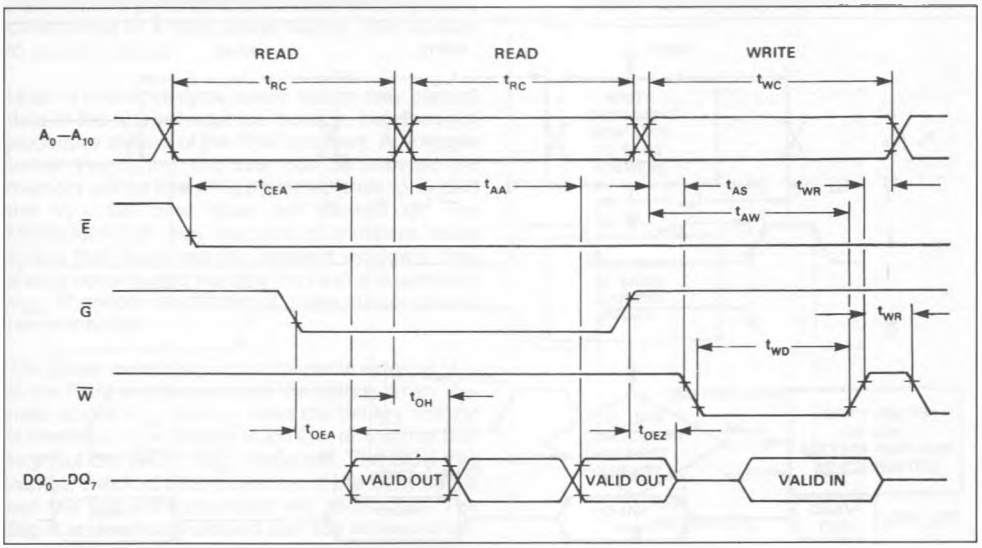
OPERATION

Read Mode

The MK48C02A/12A is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

NOTE
1. Measured using the Output Load Diagram shown in Figure 7.

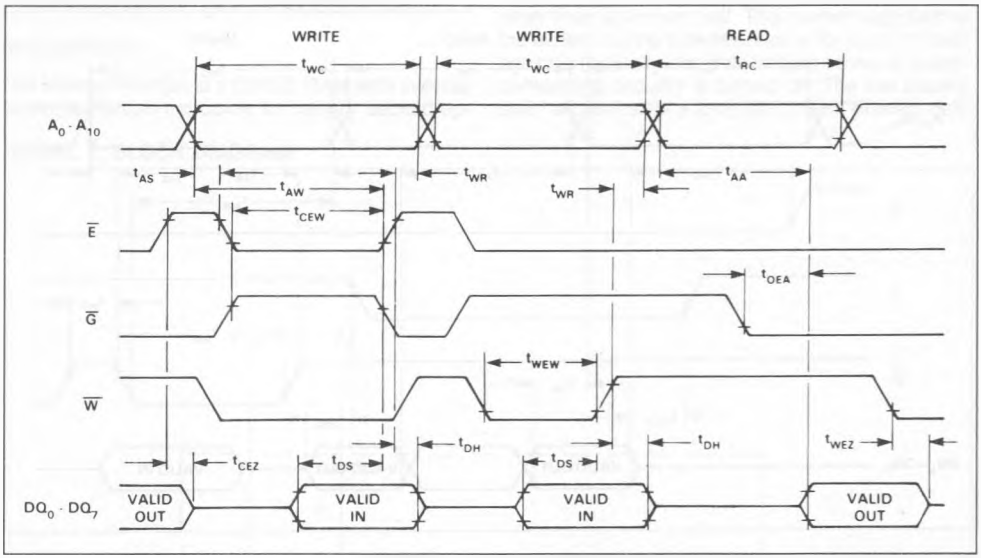
WRITE MODE

The MK48C02A/12A is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48C02A/12A $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48C02A/12A operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48C02A has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

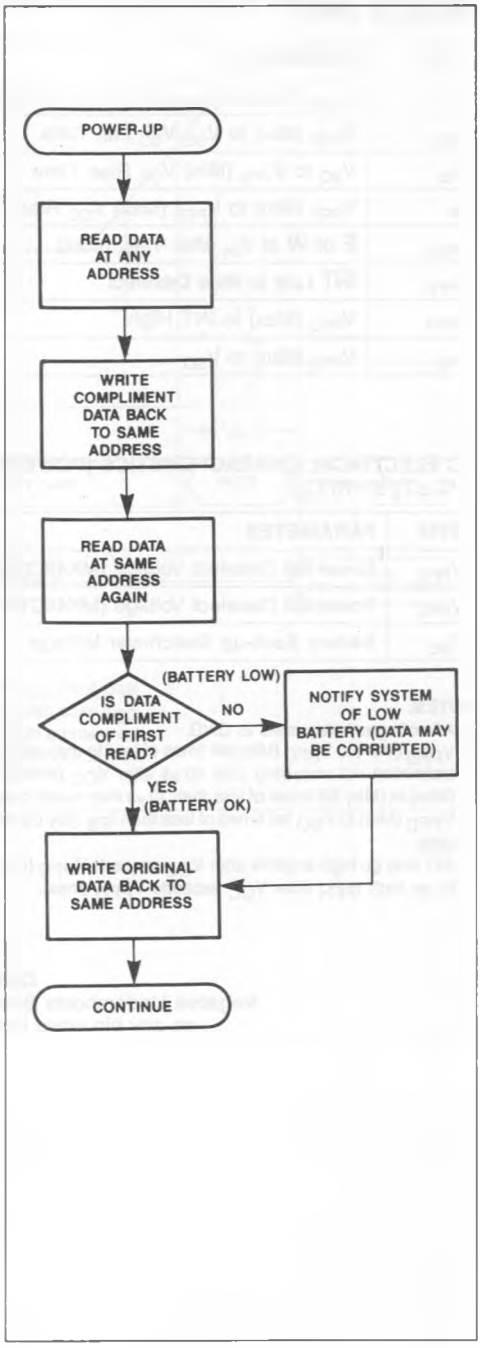
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10 μs to 40 μs advanced warning of an impending power-fail write protect.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS



AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after V_{PFD} (max)	120		µs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µs	4
t_{FB}	V_{PFD} (Min) to V_{SO}	10		µs	

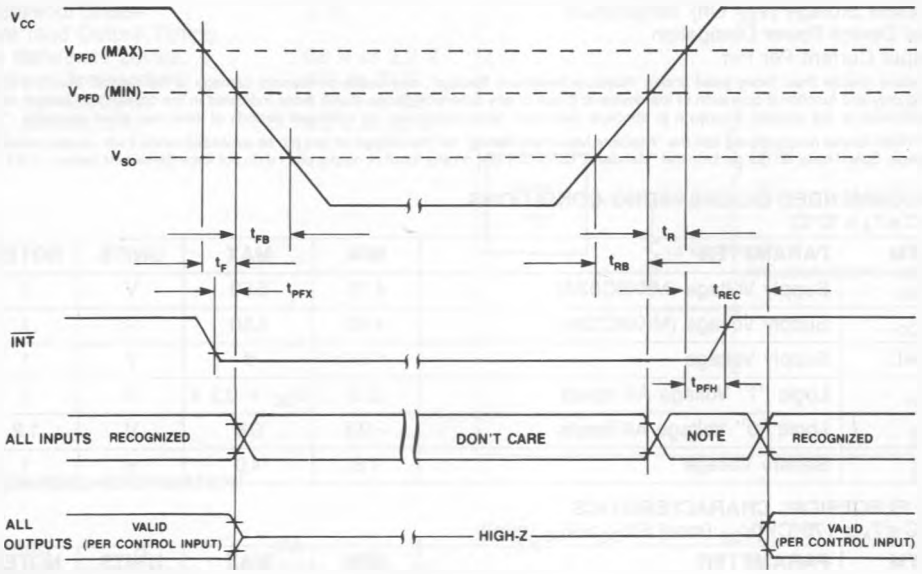
DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48C02A)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48C12A)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

NOTES:
1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION
Negative Undershoots Below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

FIGURE 6. POWER DOWN/POWER-UP TIMING



NOTE:
Inputs may or may not be recognized at this time.
Caution should be taken to keep $\overline{E}$ or $\overline{W}$ in the high state V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND . . . . . −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . . 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature . . . . . −55°C to +125°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current Per Pin . . . . . 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48C02A)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48C12A)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2
V_B	Battery Voltage	1.8	4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (max) ≥ V_{CC} ≥ V_{CC} (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{OL}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	
V_{PFL}	INT Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	
I_{BATT}	Battery Backup Current V_B = 4.0 V		1	μA	
I_{CHG}	Battery Charging Current V_{CC} = 5.5 V	−5	+5	nA	
V_{LB}	Battery OK Flag	1.8	2.6	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins and $\overline{INT}$	10 pF	4,5

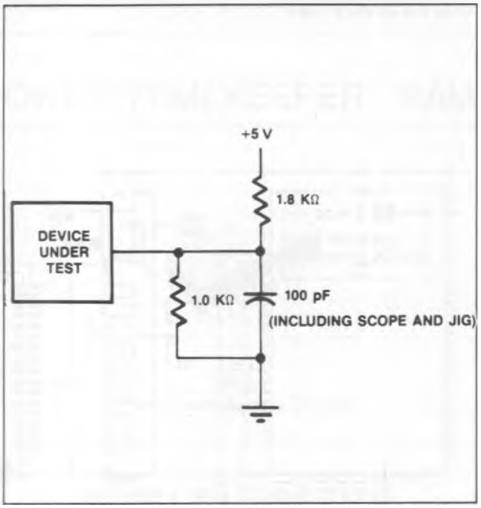
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48C02A)	4.75 V to 5.5 V
V_{CC} (MK48C12A)	4.5 V to 5.5 V

FIGURE 7. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

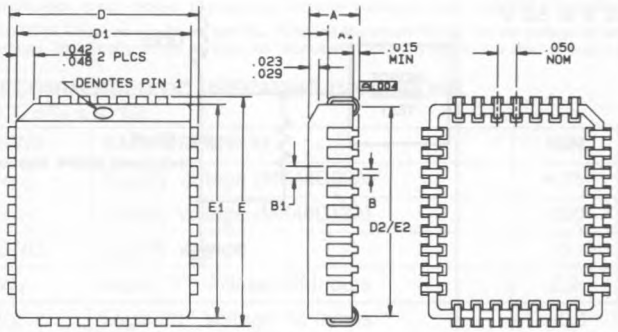
MK48C	X	2A	X	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

K 32 PIN PLCC
N 28 PIN DIP

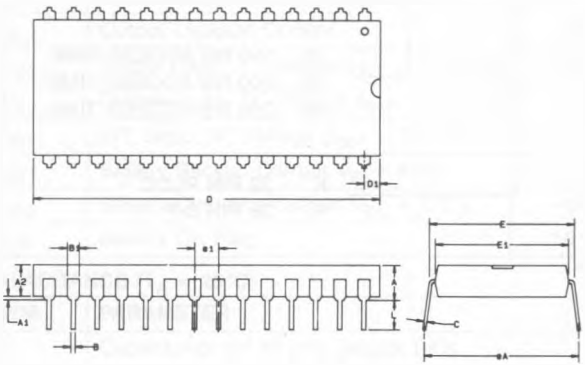
0 +10%/−5%
1 +10%/−10%

FIGURE 8. MK48C02A/12A PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

FIGURE 9. MK48C02A/12A PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.