SGS-THOMSON MICROELECTRONICS

MK48H89(N) -20/25/35

73,728-BIT 8K X 9 CMOS FAST SRAM

ADVANCE DATA

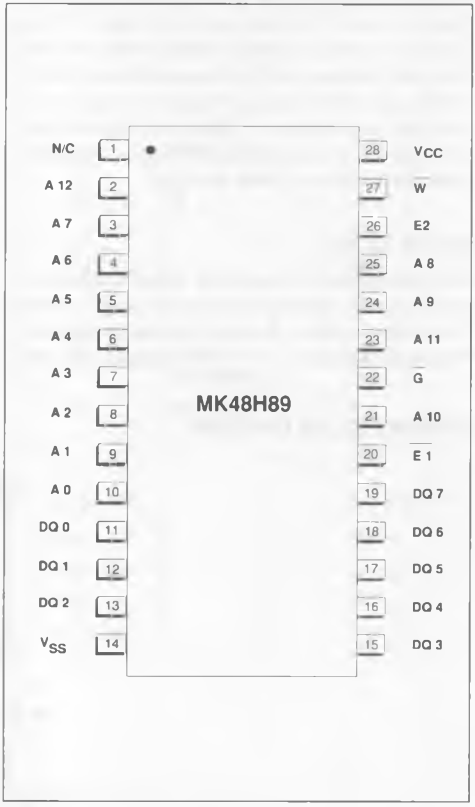
- BYTEWYDE 8K X 9 CMOS FSRAM
- FAST ACCESS TIMES, 20,25,35NS MAX.
- EQUAL ACCESS AND CYCLE TIMES
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 300 MIL PLASTIC DIP

DESCRIPTION

The MK48H89 is a 73,728-bit static RAM, organized as 8K X 9 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single + 5V ± 10% supply, and all inputs and outputs are TTL compatible.

The MK48H89 has a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E}_1$ goes high or E_2 goes low). An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E}_1$ and E_2, as summarized in the truth table.

PIN CONNECTION



PIN NAMES

A_0-A_{12}	Address Inputs
DQ_0-DQ_8	Data I/O_{0-8}
$\overline{E}_1$	Chip Enable 1, Active Low
E_2	Chip Enable 2, Active High
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/read Enable
V_{CC}, V_{SS}	+5V, GND

MK48H89 TRUTH TABLE

$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	Hi-Z	Standby
X	X	L	X	Deselect	Hi-Z	Standby
H	L	H	H	Read	Hi-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

READ MODE

The MK48H89 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables ($\overline{E1}$ and E2) are active. This provides access to data from nine of 73,728 locations in the static memory array, specified by the 13 address inputs . Valid data will be available at the nine Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, $\overline{E_1}$ is low, and E_2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The MK48H89 is in the Write mode whenever the $\overline{W}$ and $\overline{E_1}$ pins are low, with E_2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E_1}$, $\overline{W}$, or the falling edge of E_2.

If the Output is enabled ($\overline{E_1}$ = low, E_2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E_1}$ or the falling edge of E_2, whichever occurs first, and remain valid t_{WHDX} .

MK48H89 BLOCK DIAGRAM