SGS-THOMSON MICROELECTRONICS

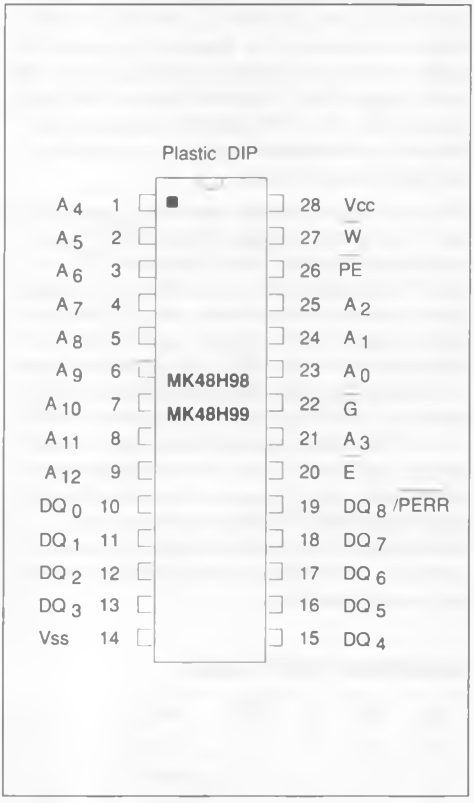
MK48H98/99(N) -20/30/40

73,728-BIT 8 K X 8/9 CMOS PARITY SRAM

ADVANCE DATA

- BYTEWYDE 8K x 9 CMOS STATIC RAM
- CONFIGURABLE: x9/ or x8 plus PARITY
- 20,30,40ns DATA ACCESS TIMES
- 25,35,45ns PARITY ERROR ACCESS TIMES
- FAST CYCLE TIMES = 25,35,45ns
- 28-PIN 300 MIL PLASTIC DIP

PIN CONNECTION



DESCRIPTION

The MK48H98/99 is a 73,728-bit CMOS Parity SRAM, organized 8K x 9 using SGS-THOMSON Microelectronics' advanced HCMOS process technology. The MK48H98/99 has a Chip Enable power down feature which sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provides a fast high impedance control, allowing fast read/write cycles to be achieved with the common-I/O data bus.

This device offers a high performance CMOS static RAM with a parity generator/checker option on chip. The $\overline{PE}$ input allows the device to be configured with or without the parity function. When parity is enabled, true parity is generated and stored internally during write operations. Parity data is accessed and checked during read operations. The MK48H98 employs an internal **even** parity scheme, while the MK48H99 employs an **odd** parity scheme. The $\overline{PERR}$ pin is an open-collector output for parity error detection, and easy wired-OR system implementation. If parity is disabled, then DQ_8 is simply another data I/O buffer with a totem-pole configuration. The Parity SRAM requires a single +5 volt supply ± 10%, and all inputs and outputs are TTL compatible.

PIN NAMES

A_0-A_{12}	Address Inputs
DQ_0-DQ_7	Data I/O_{0-7}
$DQ_8/\overline{PERR}$	Data I/O_8, Parity Error
$\overline{E_1}$	Chip Enable
$\overline{PE}$	Parity Enable
$\overline{G}$	(OE) Output Enable
$\overline{W}$	Write/read Enable
V_{CC},V_{SS}	+5V, GND

MODES OF OPERATION

As previously mentioned, the $\overline{PE}$ input can configure the MK48H98/99 to internally generate and check true parity. When the $\overline{PE}$ input is a logic zero (V_{IL}), the parity function (parity generator/checker) is enabled. If $\overline{PE}$ is a logic one (V_{IH}), the device is configured as a standard 8K x 9 SRAM. The device configuration can be accomplished by tying the $\overline{PE}$ input either high or low, depending upon the desired mode of operation. For diagnostic purposes, a parity error can be forced by writing a false parity bit pattern ($\overline{PE}$= V_{IH}), and reading with parity true ($\overline{PE}$= V_{IL}). This defines a dynamic approach for **mix-mode** operation in addition to the basic device modes.

The mix-mode operation allows the parity function to be enabled while Writing ($\overline{PE}$ = V_{IL}), and disabled during Read operations ($\overline{PE}$ = V_{IH}). This provides the user with self-generated parity from the Parity SRAM, with an external system parity bit. Conversely, parity can be disabled while Writing ($\overline{PE}$ = V_{IH}), and true parity checked internally with a device parity error detection ($\overline{PERR}$) during Read operations ($\overline{PE}$ = V_{IL}). This mode allows the device to check system generated parity without designing external parity logic. However, transceiver logic is required for $DQ_8/\overline{PERR}$ in this mode. The MK48H98/99 Truth table depicts all modes of operation. This includes either static or dynamic mode operations.

MK48H98/99 TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{PE}$	MODE	DQ
H	X	X	X	Standby	Hi-Z
L	L	X	H	Write X 9(1)	D_{IN}
L	H	L	H	Read X 9(1)	D_{OUT}
L	H	H	H	Read X 9(1)	Hi-Z
L	L	X	L	Write X 8(2)	D_{IN}
L	H	L	L	Read X 8(2)	D_{OUT}
L	H	H	L	Read X 8(2)	Hi-Z

NOTES :

(1) Operation and configuration as an 8K X 9 SRAM ($\overline{PE}$= High)

(2) Generate and store true parity during Write Cycles; $\overline{PERR}$ enabled and valid during Read Cycles ($\overline{PE}$= Low)

READ MODE

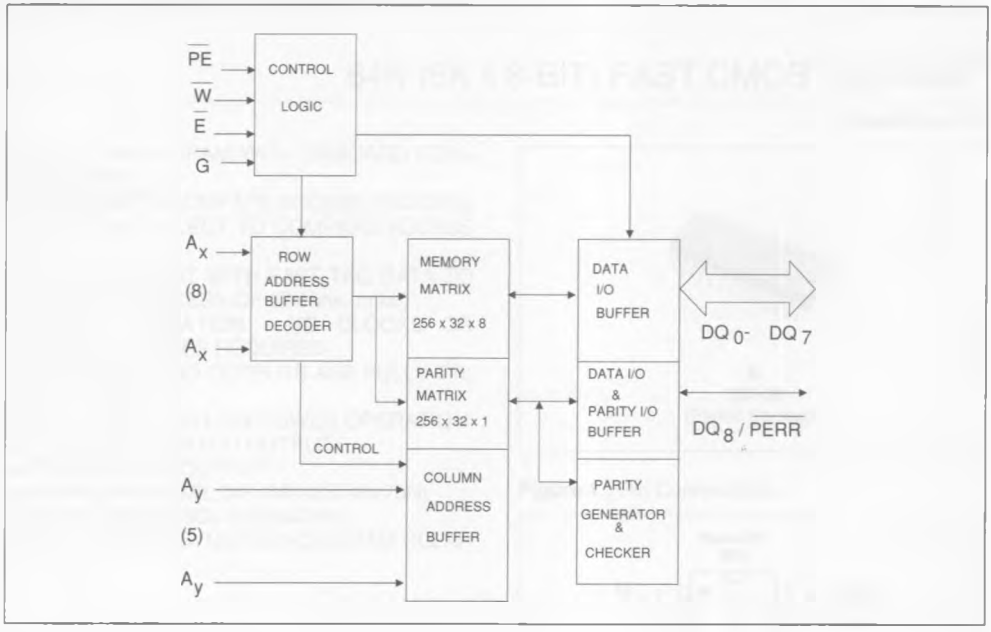
The MK48H98/99 is in the Read mode whenever Write Enable ($\overline{W}$) is high and Chip Enable ($\overline{E}$) is low. This provides access to data from nine of 73,728 locations in the static memory array. If Parity Enable ($\overline{PE}$) is high, data is accessed as a 9-bit word; if $\overline{PE}$ is low data is accessed as an 8-bit word plus parity error ($\overline{PERR}$). The unique address is specified by the 13 address inputs. Valid data will be available at the DQ Output pins within t_{AVQV} after the last stable address, and $\overline{PERR}$ will be valid within t_{AVPV} of the last stable address providing $\overline{G}$, $\overline{E}$, and $\overline{PE}$ are low (see truth table for logic options). If $\overline{E}$, $\overline{PE}$, or $\overline{G}$ access times are not met, data access and parity error access times will be measured from the limiting parameter t_{ELQV}, t_{ELPV}, t_{PELPV}, t_{PEHQV}, t_{GLQV}, or t_{GLPV} rather than the address.

WRITE MODE

The MK48H98/99 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either $\overline{E}$ or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of $\overline{E}$ and $\overline{W}$ being active low. Therefore, address setup times are referenced to $\overline{W}$, $\overline{E}$, and/or $\overline{PE}$ as t_{AVWL}, t_{AVEL} and t_{AVPEL} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of Write Enable or Chip Enable. Parity Enable ($\overline{PE}$) allows the on-board parity function to generate true parity if active low, but cannot terminate a write cycle by going high.

If the Output is enabled ($\overline{E}$ = low, and $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of $\overline{W}$, $\overline{E}$ or $\overline{PE}$, whichever occurs first, and remain valid t_{WHDX}.

MK48H98/99 BLOCK DIAGRAM N°. 1



BLOCK DIAGRAM N°. 2