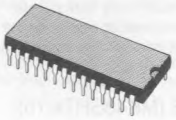
SGS-THOMSON MICROELECTRONICS

MK48S74(N,X)-20/22/25
MK48S75(N)-20/22/25

64K (8K x 8-BIT) FAST CMOS TAGRAM™

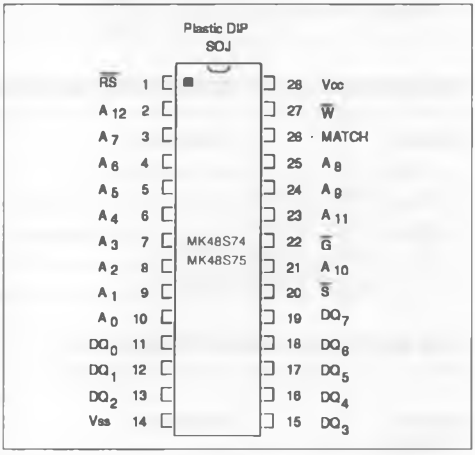
ADVANCE DATA

- 8K x 8 CMOS SRAM WITH ONBOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS 20/22/25ns
- FAST CHIP SELECT TO COMPARE ACCESS 15ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 12/15ns (max.)
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- OPEN DRAIN MATCH OUTPUT
- THREE-STATE OUTPUT
- 28 PIN 300/600 MIL DIP (MK48S74N/75N)
- 28 PIN 330 MIL SOJ (MK48X74S)
- HIGH SPEED ASYNCHRONOUS RAM CLEAR



N
DIP-28
(Plastic Package)

Figure 1 : Pin Connections.



DESCRIPTION

The MK48S74/75 are a 65,636-bit fast static cache TAGRAM organized as 8K x 8 bits. It is fabricated using SGS-THOMSON Microelectronics low power, high performance, CMOS technology. The MK48S74/75 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The device requires a single + 5V ± 10 percent supply, and is fully TTL compatible.

The MK48S74/75 has a fast Chip Select control for high speed operation to Match Compare valid, and device select/deselect operations. Additionally, the MK48S74/75 provides a Reset Clear, and Match compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open-drain for wired OR operation. During a match compare cycle, an onboard 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A_0-A_{12}) to the internal RAM data. If a match exists, the MATCH output issues a HIGH match valid signal. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

PIN NAMES

A_0 - A_{12}	– Address Inputs
DQ_0 - DQ_7	– Data Input/output
$\overline{S}$	– Chip Select
$\overline{W}$	– Write Enable
$\overline{G}$	– Output Enable
V_{CC}	– + 5V
V_{SS}	– Ground
$\overline{RS}$	Reset Flash Clear
MATCH	Match Output

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Voltage on any Pin Relative to GND	– 1.0 to 7.0	V
Ambient Operating Temperature (T_A)	0 to + 70	°C
Ambient Storage Temperature (plastic)	– 55 to + 125	°C
Ambient Storage Temperature (ceramic)	– 65 to + 150	°C
Total Device Power Dissipation	1	Watt
Output Current per Pin	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TRUTH TABLE (MK48SH74/75)

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	High-Z
X	H	X	H	Deselect	High-Z	High-Z
H	L	H	H	Miss-NOmatch	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High-Z
H	L	L	H	Read	Q_{OUT}	High-Z
L	L	X	H	Write	D_{IN}	High-Z

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq + 70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
V_{SS}	Supply Voltage	0	0	0	V	4
V_{IH}	Logic 1 Voltage, all Inputs	2.2		V_{CC} + 0.3	V	4
V_{IL}	Logic 0 Voltage, all Inputs	– 0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq + 70°C$) ($V_{CC} = 5.0 \pm 10$ percent)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{CC1}	Average Power Supply Current f = min Cycle			150	mA	5
I_{CC2}	Average Power Supply Current f = 0			110	mA	6
I_{IL}	Input Leakage Current (any input pin)	– 1		+ 1	µA	7
I_{OL}	Output Leakage Current (any Q output pin)	– 5		+ 5	µA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = – 4mA)	2.4			V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = + 8mA)			0.4	V	4
V_{OL}	Match Output Logic 0 Voltage (I_{OUT} = 18mA)			0.4	V	4

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

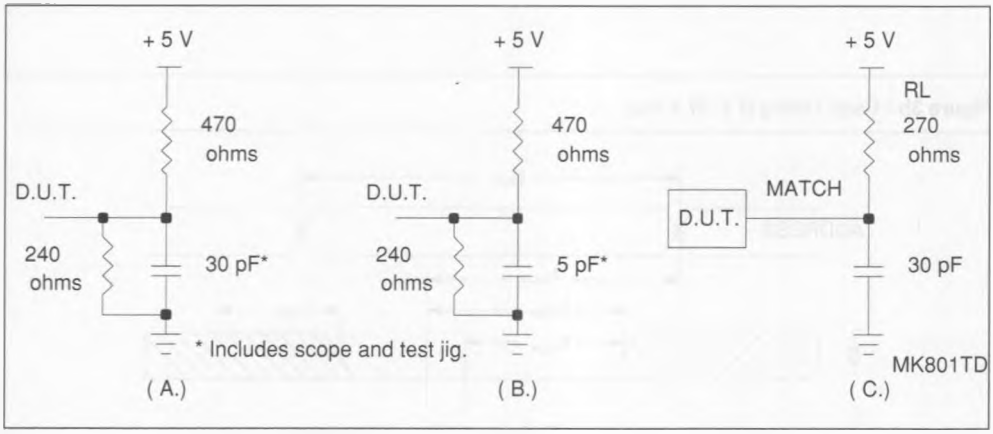
Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Capacitance on Input Pins	4		5	pF	9
C_2	Capacitance on DQ Pins	8		10	pF	9

Notes : 1. Measured with load shown in figure 2(A).
2. Measured with load shown in figure 2(B).
3. Measured with load shown in figure 2(C).
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. I_{CC2} is measured with outputs open circuit.
7. Input leakage current specifications are valid for all V_{IN} such that 0V< V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0V< V_{OUT} < V_{CC}, $\overline{S}$ = V_{IH}, and V_{CC} in valid operating range.

AC TEST CONDITIONS

Input Levels..... GND to 3.0V
Transition Times..... 5ns
Input and Output Signal Timing Reference Level 1.5V
Ambient Temperature..... 0°C to 70°C
V_{CC}..... 5.0V ± 10 percent

Figure 2 : Output Load Circuits.



OPERATIONS

READ MODE

The MK48S74/75 are in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Select or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 3a : Read Timing N°1 (address access).

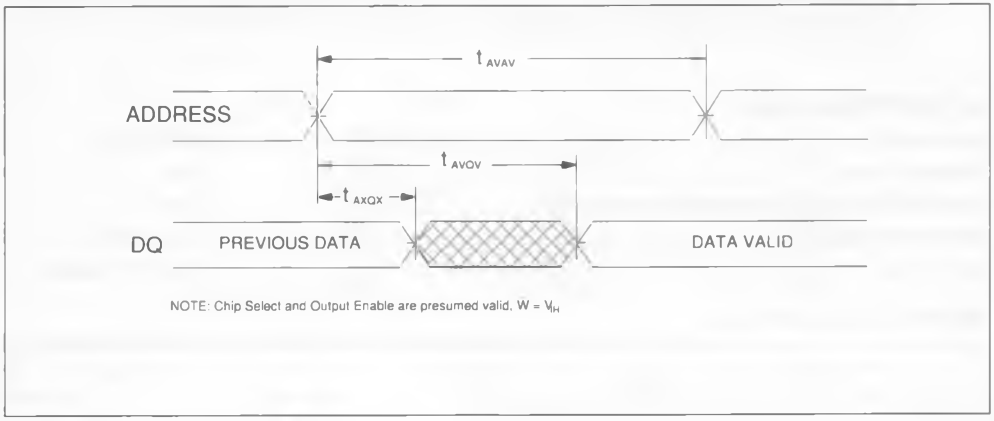
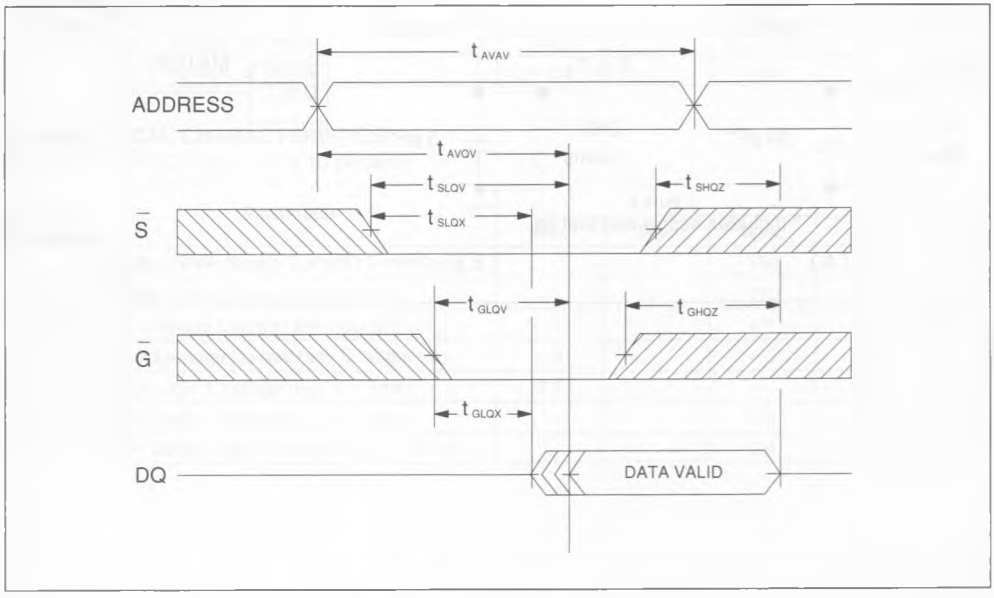


Figure 3b : Read Timing N°2 ($\overline{W}$ = V_{IH}).



AC ELECTRICAL CHARACTERISTICS (read cycle timing)

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	t_{AVAV}	Read Cycle Time	20		25		25		ns	
t_{AA}	t_{AVQV}	Address Access Time		20		25		25	ns	1
t_{CSA}	t_{SLQV}	Chip Select Access Time		15		15		15	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		10		12		15	ns	1
t_{CSL}	t_{SLQX}	Chip Select to Output Low-Z	0		0		0		ns	
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		0		ns	
t_{CSZ}	t_{SHQZ}	Chip Select to High-Z	0	10	0	10	0	10	ns	
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		10		12		15	ns	2
t_{OH}	t_{AXQX}	Output Hold from Address Change	3		3		3		ns	1

WRITE MODE

The MK48S74/75 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$.

If the Output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

Figure 4a : Writing Timing N°1 ($\overline{W}$ control).

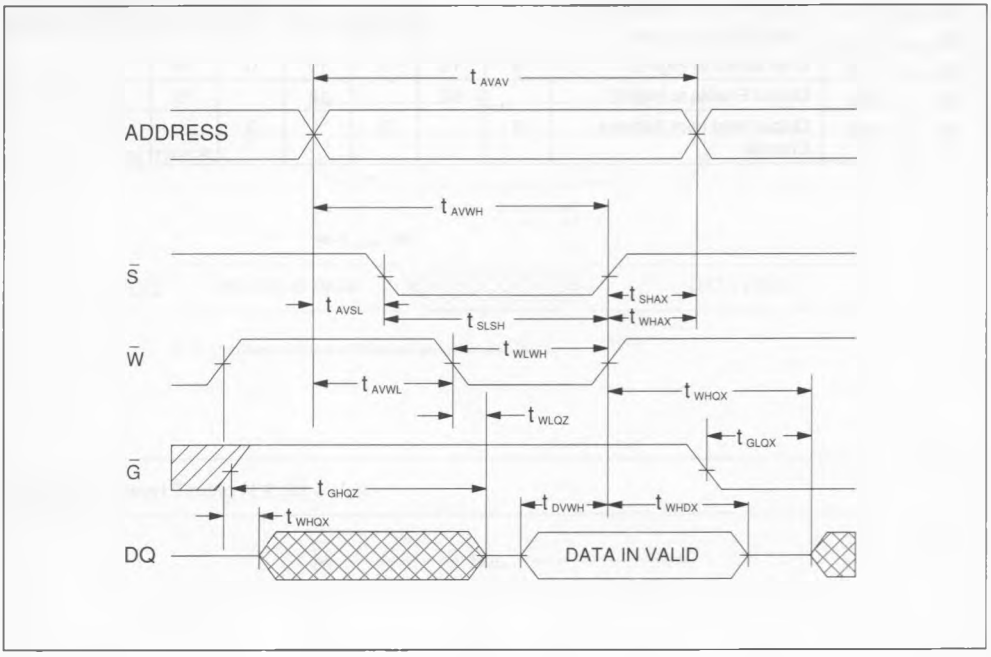
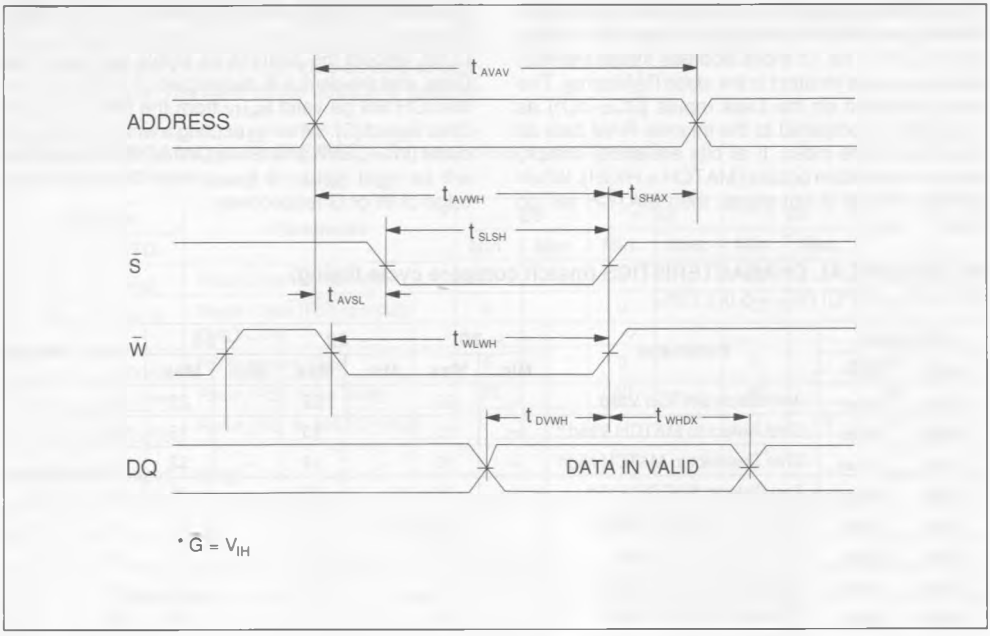


Figure 4b : Write Timing N°2 ($\overline{S}$ control).



AC ELECTRICAL CHARACTERISTICS (write cycle timing)
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	t_{AVAV}	Write Cycle Time	20		25		25		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		0		ns	
t_{AS}	t_{AVSL}	Address Set-up Time to Chip Select	0		0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	15		20		20		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	15		20		20		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		0		ns	
t_{CSW}	t_{SLSH}	Chip Select to End of Write	15		20		20		ns	
t_{WR}	t_{SHAX}	Write Recovery Time to Chip Deselect	0		0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	10		13		30		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (active)	0		0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		5		7		7	ns	2

COMPARE MODE

The MK48S74/75 are in the Compare mode whenever W and G are HIGH provided Chip Select (S) is active LOW. The 13 index address inputs (A_0-A_{12}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition.

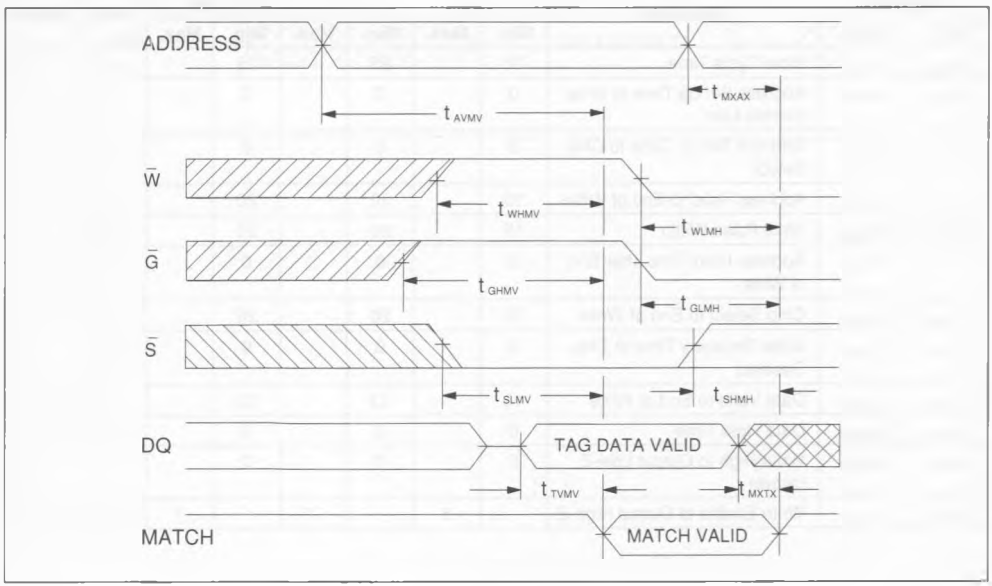
The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when S is LOW. Should the address be stable with valid Tag Data, and the device is deselected (S = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select (S). When executing a write-to-compare cycle (W = LOW, and G = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of W or G respectively.

AC ELECTRICAL CHARACTERISTICS (match compare cycle timing)

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 ± 10%)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AMA}	t_{AVMV}	Address to MATCH Valid	–	20	–	22	-	25	ns	2
t_{CSM}	t_{SLMV}	Chip Select to MATCH Valid	–	15	–	15	–	15	ns	2
t_{CSMH}	t_{SHMH}	Chip Deselect to MATCH High	–	10	–	12	–	12	ns	2
t_{DMA}	t_{TVMV}	Tag Data to MATCH Valid	–	12	–	15	–	15	ns	2
t_{OEM}	t_{GHMV}	$\overline{G}$ High to MATCH Valid	–	15	–	15	–	15	ns	3
t_{OEMH}	t_{GLMH}	$\overline{G}$ Low to MATCH High	–	10	–	12	–	12	ns	3
t_{WEM}	t_{WHMV}	$\overline{W}$ High to MATCH Valid	–	15	–	15	–	20	ns	3
t_{WEMH}	t_{WLMH}	$\overline{W}$ Low to MATCH High	–	12	–	12	–	15	ns	3
t_{MHA}	t_{AHMV}	MATCH Hold from Address	3	–	3	–	3	–	ns	3
t_{MHD}	t_{DHMV}	MATCH Hold from Tag Data	0	–	0	–	0	–	ns	3

Figure 5 : Match Compare Timing.



RESET MODE

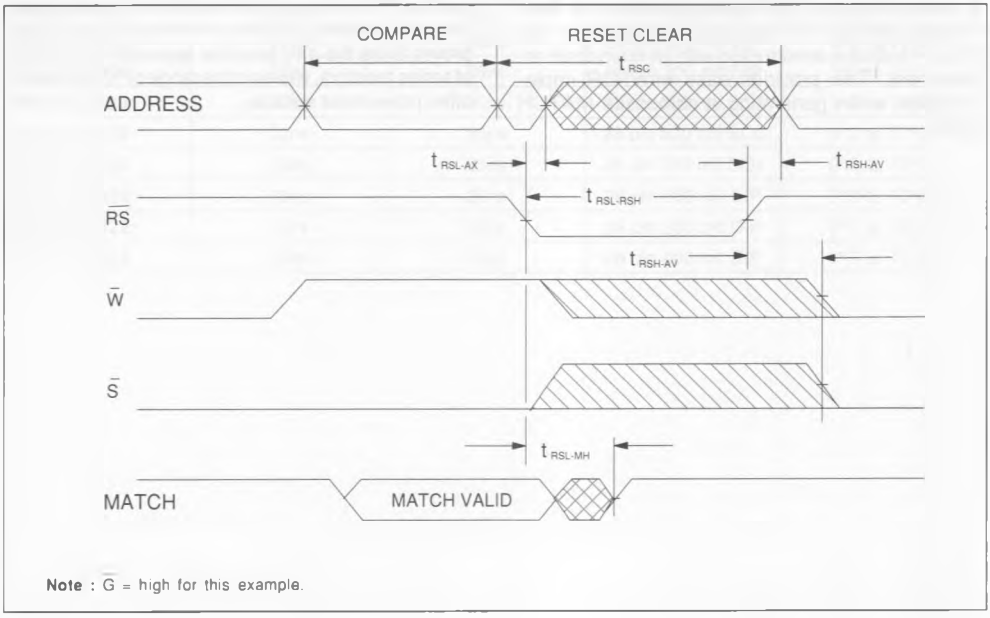
The MK48S74/75 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see truth table). The MATCH output will go HIGH t_{RSL-MH} from the falling edge of $\overline{RS}$, and all inputs will not be recognized until t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

AC ELECTRICAL CHARACTERISTICS (reset clear cycle timing)

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

Symbols		Parameter	– 20		– 22		– 25		Unit	Notes
ALT.	STD.		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	t_{RSC}	Flash Clear Cycle Time	40		0		50		ns	
t_{RSX}	t_{RSL-AX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSV}	t_{RSH-AV}	$\overline{RS}$ to Inputs Valid	5		5		5		ns	
t_{RSP}	$t_{RSL-RSH}$	Reset ($\overline{RS}$) Pulse Width	35		40		40		ns	
t_{RSM}	t_{RSL-MH}	Reset ($\overline{RS}$) to MATCH High		15		15		15	ns	

Figure 6 : Reset Timing.



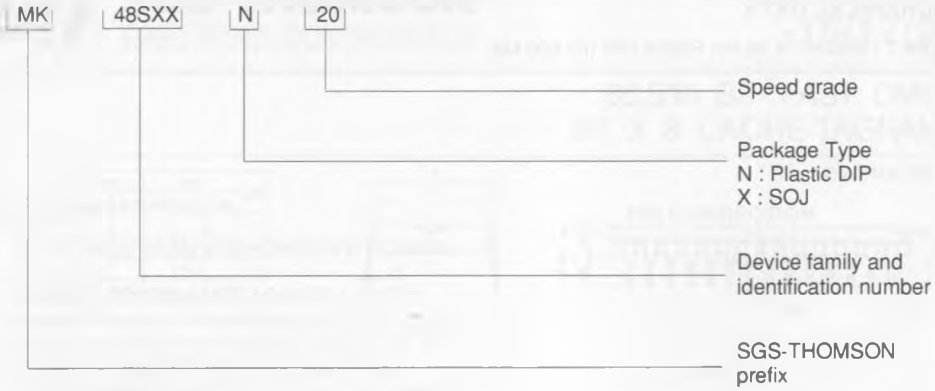
Note : $\overline{G}$ = high for this example.

APPLICATION

The MK48S74/75 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48S74/75 can also interface to 5 volt CMOS on all inputs and outputs. The MK48S74/75 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWIDE™ on-board comparator - all in one chip. The MK48S74/75 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input TAG data generating a miss. The MATCH output is constructed with an open drain arrangement. This provides easy wired-OR implementation when generating a composite MATCH signal.

In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of a portion of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S74/75. and providing good hit or match ratio designs will enhance overall system performance.

Because high frequency current transients will be associated with the operation of the MK48S74/75, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

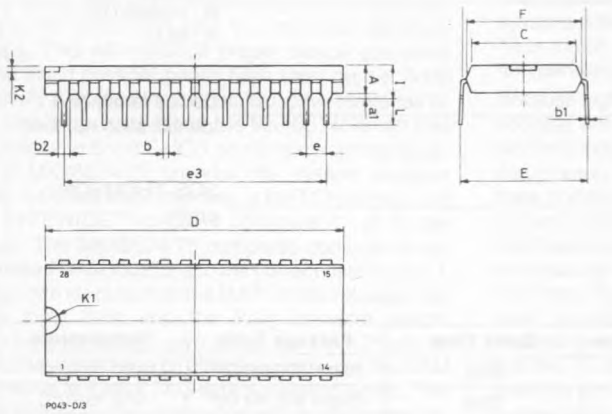


ORDER CODES

Part No.	Match Access Time	Cycle Time	Package Type	Temperature
MK48S74N20	20ns	20ns	28 pin 300 mil DIP	0°C to 70°C
MK48S74N22	22ns	25ns	28 pin 300 mil DIP	0°C to 70°C
MK48S74N25	25ns	25ns	28 pin 300 mil DIP	0°C to 70°C
MK48X74X20	20ns	20ns	28 pin 330 mil SOJ	0°C to 70°C
MK48X74X22	22ns	25ns	28 pin 330 mil SOJ	0°C to 70°C
MK48X74X25	25ns	25ns	28 pin 330 mil SOJ	0°C to 70°C
MK48S75N20	20ns	20ns	28 pin 600 mil DIP	0°C to 70°C
MK48S75N22	22ns	25ns	28 pin 600 mil DIP	0°C to 70°C
MK48S75N25	25ns	25ns	28 pin 600 mil DIP	0°C to 70°C

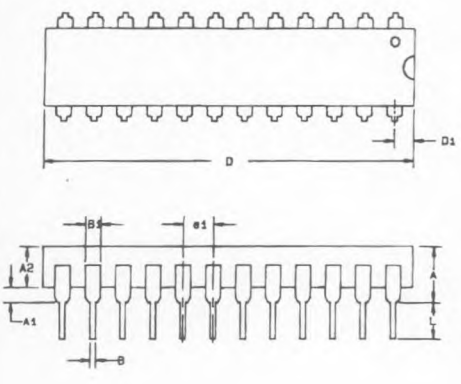
MECHANICAL DATA

Figure 7 : MK48S75 28 Pin Plastic DIP (N) 600 MIL.



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	0.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		.657
e		2.54			.100	
e3		33.02			1.300	
e4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 8 : MK48S74 28 Pin Plastic DIP (N) 300 MIL.



Dim.	Inches	
	Min.	Max.
A		.210
A1	.015	
A2	.120	.140
B	.015	.021
B1	.045	.070
C	.008	.012
D		1.270
D1	.060	.090
E	.300	.325
E1	.240	.270
e1	.090	.110
eA	.300	.365
L	.125	