SGS-THOMSON MICROELECTRONICS

MK48S80(N,X) -15/17/20

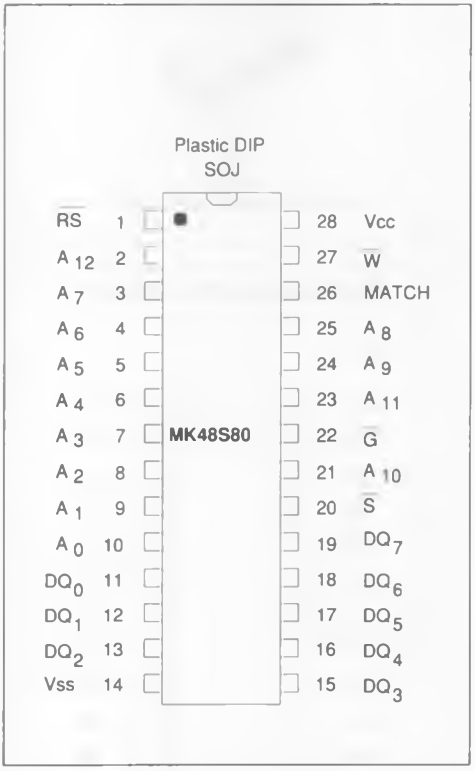
65,536 BIT FAST CMOS 8K X 8 CACHE TAGRAM™

ADVANCE DATA

FEATURES

- 8K X 8 CMOS SRAM WITH ONBOARD COMPARATOR.
- ADDRESS TO COMPARE ACCESS 15/17/20.
- FAST CHIP SELECT COMPARE ACCESS 10ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 10/12/14NS (MAX).
- STATIC OPERATION-NO CLOCKS OR TIMING STROBES REQUIRED.
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE.
- FULL CMOS FOR LOW POWER OPERATION.
- TOTEM-POLE MATCH OUTPUT.
- THREE-STATE OUTPUT.
- 28 PIN 300 MIL DIP & 28 PIN 330 MIL SOJ.
- HIGH SPEED ASYNCHRONOUS RAM CLEAR.

PIN CONNECTION



DESCRIPTION

The MK48S80 IS 65,536 fast static cache TAGRAM organized as 8K X 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMPOS4 technology. The MK48S80 features fully dtztic opeation requiring no external clocks or timing strobes, and equal access and cycles times. The device requires a single +5v ± 10% supply and is fully TTL compatible. The MK48S80 has a fast Chip Select control for high sped operation to the match compare valid, and device select/deselect operations. Additionally, the MK48S80 provides a Reset Clear, and MATCH compare pin. The RESET CLEAR, input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only 2 cycles. The MATCH output is in a totem-pole configuration to minimize switching delays associated with open-drain devices. During a MATCH compare cycle, and on-board 8-bit comparator compares the Data Input (8-bit TAG) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

MK48S80 TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	MODE	DQ	MATCH
X	X	X	L	Reset Clear	High-Z	Invalid
X	H	X	H	Deselect	High-Z	Invalid
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	Invalid
H	L	L	H	Read	Q_{OUT}	Invalid