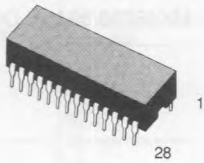
SGS-THOMSON MICROELECTRONICS

MK48Z30/30A(B) -10/12/15

32 K X 8 ZEROPOWER™ RAM

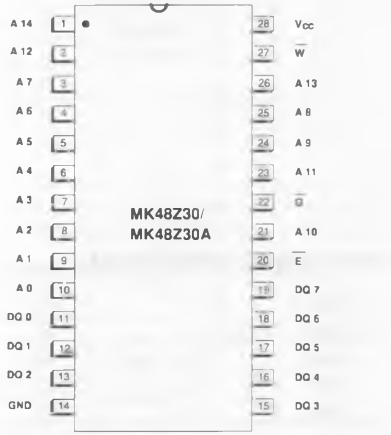
ADVANCE DATA

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED BATTERY BACK-UP OF 10 YEARS @ 25°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE: MK48Z30:4.75VOLTS. MK48Z30A: 4.50 VOLTS.



B
28-DIP
Plastic Package

PIN CONNECTIONS



DESCRIPTION

Part Number	Access Time	R/W Cycle Time	V_{CC}
MK48Z30B - 10	100 ns	100 ns	+10 / -5 %
MK48Z30 B - 12	120 ns	120 ns	+10 / -5 %
MK48Z30 B - 15	150 ns	150 ns	+10 / -5 %
MK48Z30AB-10	100 ns	100 ns	+10 / -10%
MK48Z30AB-12	120 ns	120 ns	+10 / -10%
MK48Z30AB-15	150 ns	150 ns	+10 / -10%

PIN NAMES

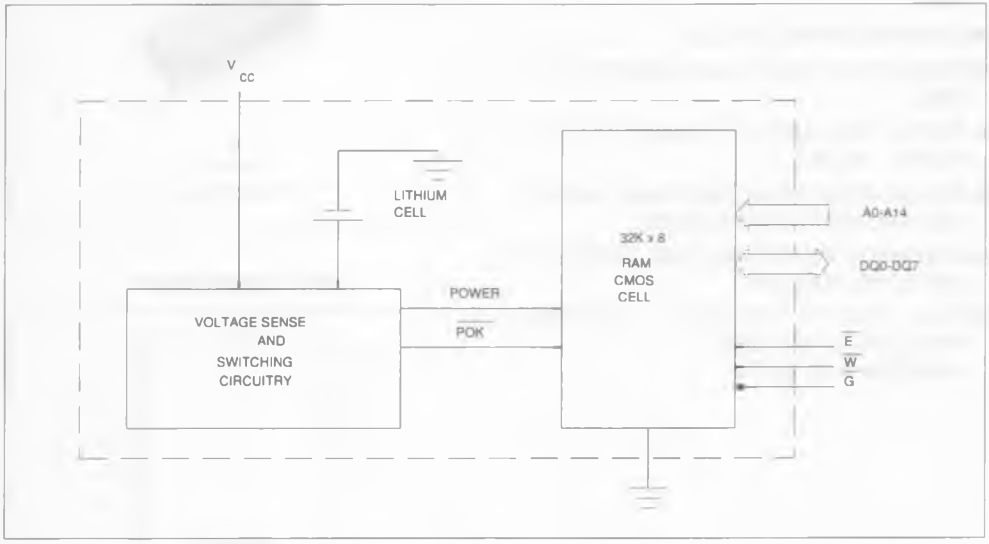
A0-A14	Address Input	Vcc	+5Volts
E	Chip Enable	W	Write Enable
		G	Output Enable
GND	Ground	DQ0-DQ7	Data IN/Data Out

DESCRIPTION

The MK48Z30/30A combines an 32K x 8 full CMOS S RAM and 2 long life carbon mono-fluoride batteries in a single plastic DIP package.The MK48Z30/30A is a nonvolatille pin and function equivalent to any JEDEC standard 32Kx 8 SRAM. it also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROM s without any requiment for special writetiming,or limitations on the number of writes that can be performed.

In addition,the MK48Z30/30A has its own Power-fail Dectect Circuit. The circuit deselect s the device whenever V_{CC} is below tolerance, providing a hight degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

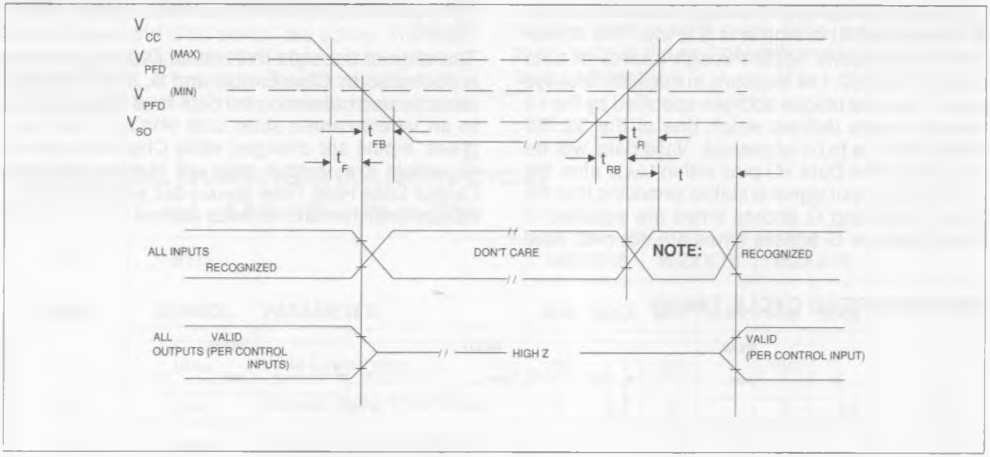
FIGURE 1 : MK48Z30/30A BLOCK DIAGRAM



TRUTH TABLE (MK48Z30/30A)

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc (Max)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
Vcc (Mln)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Mln) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER UP/DOWN TIMING



AC ELECTRICAL CHARACTERISTICS (POWER -UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} FallTime	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} FallTime	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} After Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/ DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	VALUES			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30)	4.5	4.6	4.75	V	1
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30A)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	4

NOTES:

1 . All voltages referenced to GND.

2 . V_{PFD}(Max) to V_{PFD}(Min) fall times of less t_F may result in deselection/write protection not occuring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max)to (Min) fall times of less than 10 µs may cause corruption of RAM data.

3 . V_{PFD}(Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

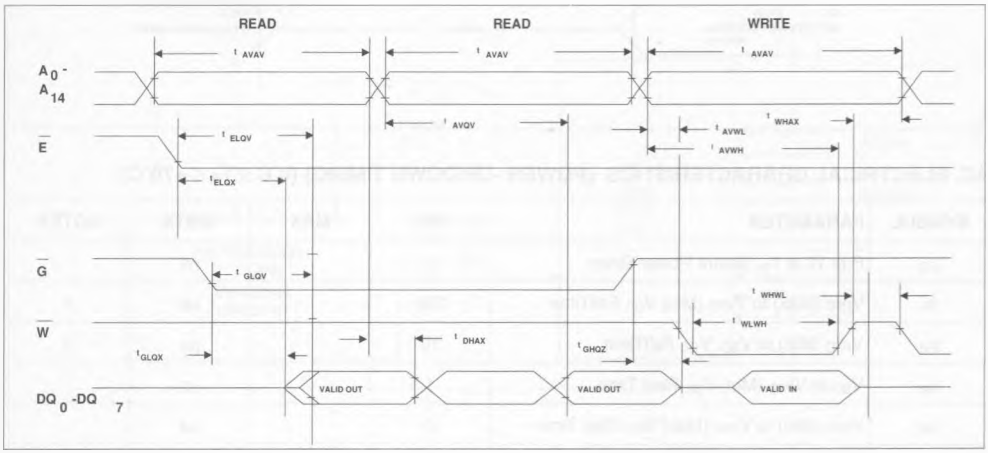
4 . 25°C ambient condition.

READ MODE

The MK48Z30/30A is in the Read Mode whenever W (Write Enable) is high and E is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 14 Address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied. If Chip Enable or G access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and G. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until tAVQV. If the Address inputs are changed while Chip Enable and G remain low, output data will remain valid for Output Data Hold Time (t_{DHAX}) but will go indeterminate until the next Address Access.

FIGURE 3 : READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

(0°C≤T_A≤ + 70°C, VCC = 5.0 V +10% / -5%or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		ns	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		
t_{CEA1}	t_{ELQV}	$\overline{E_1}$ Access Time		100		120		150		
t_{CEZ}	t_{EHQZ}	Chip Enable Off Time		50		60		75		
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		
t_{OEL}	t_{GLQX}	Output Enable To Q Low-z	5		5		5			
t_{CEL}	t_{ELQX}	Chip Enable To Q Low-z	10		10		10			
t_{OH}	t_{DHAX}	Output Hold From Address	5		5		5			

WRITE MODE

The MK48Z30/30A is in the Write Mode whenever Write Enable and Chip select are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high or for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVEH} prior to the end of write and remain valid for t_{WHDX} afterward.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

(0°C≤T_A≤+ 70°C, V_{CC} = 5.0 V +10% / -5% or -10%)

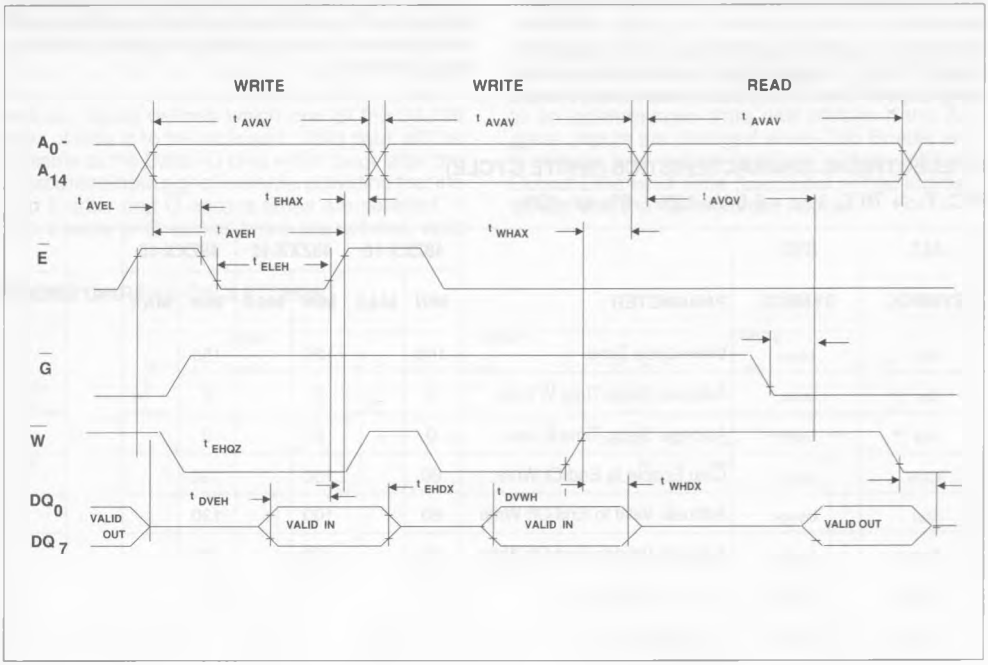
ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0			
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0			
t_{CEW}	t_{ELEH}	Chip Enable to End Of Write	80		100		130			
t_{AW}	t_{AVWH}	Address Valid to End Off Write	80		100		130			
t_{AW}	t_{AVEH}	Address Valid to End Off Write	80		100		130			
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100			
t_{TCEZ}	t_{EHQZ}	$\overline{E}$ Data of Time		50		60		75		
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data of Time		50		60		75		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10			1
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10			2
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low Next Cycle	10		10		10			
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70			1
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70			2
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5			1
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5			2

NOTES:

1 . In a $\overline{W}$ Controlled Cycle.

2 . In a $\overline{E}$ Controlled Cycle.

FIGURE 4 : WRITE CYCLE TIMING



DATA RETENTION MODE

With V_{CC} applied, the MK48Z30/30A operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F.

The power switching circuit connects external V_{CC} to the RAM and disconnects the batteries when V_{CC} rises above V_{SO}. Normal RAM opetration can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Cuation should be taken to kepp E or W hight as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

BATTERY LONGIVITY

The useful life of the MK48Z30/30A is expected to ultimately come to an end for one of two reasons: either because the effects of aging render the cell useless before it can actually be discharged; or because they have been discharged while providing current to an external load.

With V_{CC} on, the batteries are disconnected from the RAM and aging effects become th determining factor in battery-Storage Life.

With V_{CC} off, the MK48Z30/30A initates back-up mode by swithching power from V_{CC}input to the batteries.The leakage current drawn by the RAM represents the only load on the batteries and is referred as the Capacity Consomption

* Storage Life

Figure 5 illustrates how temperature affects Storazge Life of the MK48Z30 batteries. The figure graphs the battery life as a function of temperature and the percentage of time VCC remains on.

Note that regardless off V_{CC} Duty Cycle, Storage Life always decrases with an increase in temperature.

With V_{CC} continuously off, representing a 0% Duty Cycle, the Storage Life of the batteries is short due to the load of the RAM which draws current (consumes batteries capacity).

.With V_{CC} continously on, representing a 100% Duty Cycle (t1%), the Storage Life of the batteries is long due to the RAM being disconnected from the batteries and drawning no current.

Two End-of- Life curves are presented in the Figure 6. They are labeled "100% Duty Cycle - Storage " (t1%), and "Average" (t50%). These terms are related to probability that a given number of failures will have accumulated by a particular point in time. If, for example, the batteries expected life at 70°C is an issue, Figure 5 indicates that an MK48Z30/30A has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year time.

Back-Up Life Calculation

$$\text{Back-Up Life} = \frac{1}{\{[(TA_1 \div TT) \div BL_1] + [(TA_2 \div TT) \div BL_2] + \ldots + [(TAN \div TT) \div BL_N]\}}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, ect....

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_N$

BL_1, BL_2, BL_N = Back-Up System Life at Temp.1, Temp.2, ect... (See Figure 5)

Example Back-Up Life Calculation

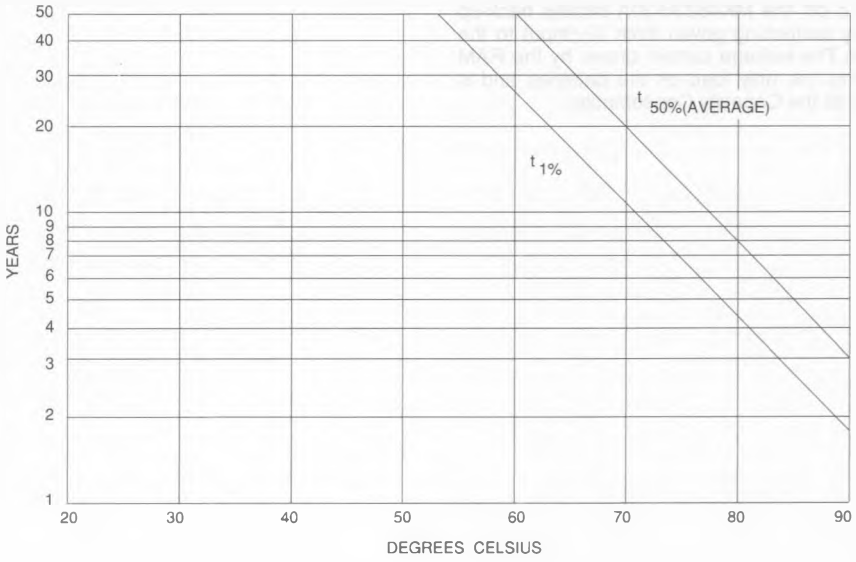
A cash register operates in an environment where the MK48Z30/30A is exposed to a 40°Ctemperatures at 50% power Duty Cycle for 5 days. The 6th day, the MK48Z30/30A is exposed to a 55°C temperature at 100% Duty Cycle. The 7th day, the regester is not used and is exposed to 25°C at 0% Duty Cycle.

Reading Predicted values from Figure 6 ; BL_1 = 4 yrs, BL_2 = 40 yrs, BL_3 = 5 yrs.
Total Time (TT) = 8760 hrs./yr. TA_1 = 6264 hrs/yr, TA_2 = 1248 hrs/yr, TA_3 = 1248 hrs/yr.

$$\text{Back-Up Life} = \frac{1}{\{[(6264/8760) \div 8] + [(1248/8760) \div 40] + [(1248/8760) \div 10]\}}$$

$$= 9.3 \text{ years}$$

FIGURE 5 : PREDICTED BATTERY STORAGE LIVE VS. TEMPERATURE AND V_{CC} DUTY CYCLE

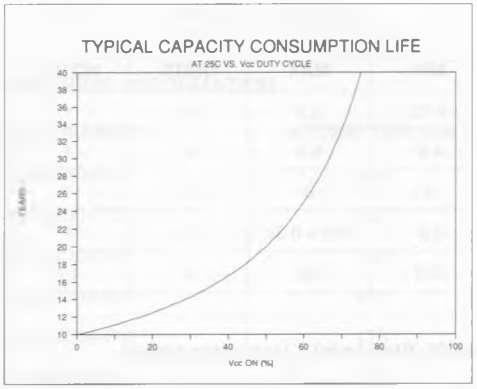


*** Capacity Consumption Life**

The MK48Z30/30A bettery cells have a minimun rated capacity of 35 mAh each. The RAM, battery-backed mode, places a nominal load of 825 nA at 25 °C. At that rate, the MK48Z30/30A will consume the capacity of the battery cells in 84,848 hours or about 10 years. But as Figure 6 Shows, Capacity Consumption can be spread over a much longer period of time whem the V_{CC} Duty Cycle is increased.

Capacity Consumption Life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption Life directly from Figure 6 and dividing by one minus the expected V_{CC} Duty Cycle.

FIGURE 6



For example, the Capacity Consumption Life of an MK48Z30/30A at 25°C and at 20% V_{CC} Duty Cycle is:

10 Years / (1-0.20) = 12.5 Years

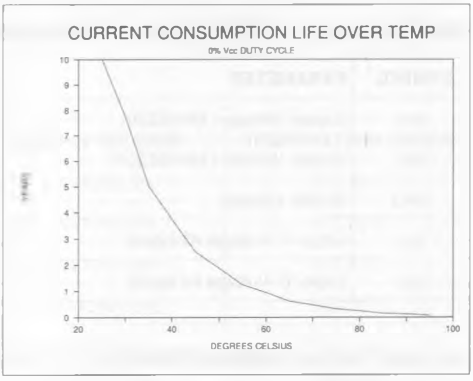
Naturally, battery-backed mode current varies with temperature. As Figure 7 indicates, the Current Consumption Life of the MK48Z30/30A in battery-Backed mode is also function of the temperature. Therefore, to calculate the Capacity Consumption Life of the MK48Z30/30A over temperature, the same equation is used except the corresponding Current Comnsumption Life for a specific temperature, derived from Figure 7 is substituted.

*** Back-Up Life**

The Back-Up Life of the MK48Z30/30A is defined as the combination of the devices'operational factors as previously mentioned. Tha is, the combination of the Storage Life and Capacity Consumption of the batteries. Both of these factors have been graphically represented in the Figure 6 and are a function of the temperature.

Calculations of Back-Up Life begins relative to the first day power is applied to the device. Each MK48Z30/30A RAM is disconnected from the battery at time of manufacture to insure battery longevity. Only after V_{CC} is initially applied is Back-Up Life affected.

FIGURE 7



Because the ambient temperature is dependent upon application controlled variables, only the user can estimate Back-Up Life in a given design. As long as ambient temperature is held reasonably constant, expected Back-Up Life can be read directly from Figure 5 If the MK48Z30/30A spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Back-Up Life.

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (V_{CC} On) Temperature (t_A)	0 to 70	°C
Ambient Storage (V_{CC} Off) Temperature	-40 to +70	°C
Total Device Power Dissipation	1.0	W
Output Current Per Pin (one Output at a Time)	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION

Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage (MK48Z30)	4.75	5.5	V	1
Vcc	Supply Voltage (MK48Z30A)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Icc1	Average Vcc Power Supply Current		90	mA	3
Icc2	TTL Standby Current ($\overline{E}_1 = V_{IH}$ or $\overline{E}2 = V_{IL}$)		5	mA	
Icc3	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		2	mA	4
I_{IL}	Input Leakage Current (Any Input)	-2	2	µA	5
I_{OL}	Onput Leakage Current	-2	2	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V1 ≥ GND and outputs deselected.

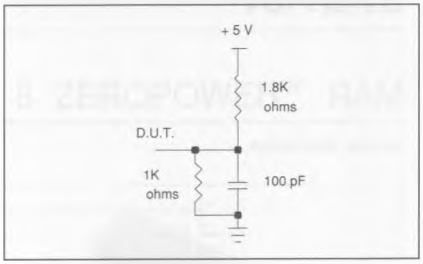
AC TEST CONDITION

Input Levels :. . . . . .0.0V to 3.0V

Transition Times :. . . . . .5 ns

Input and Output Timing
Reference Levels :. 1.5V

FIGURE 8 : OUPUT LOAD DIAGRAM



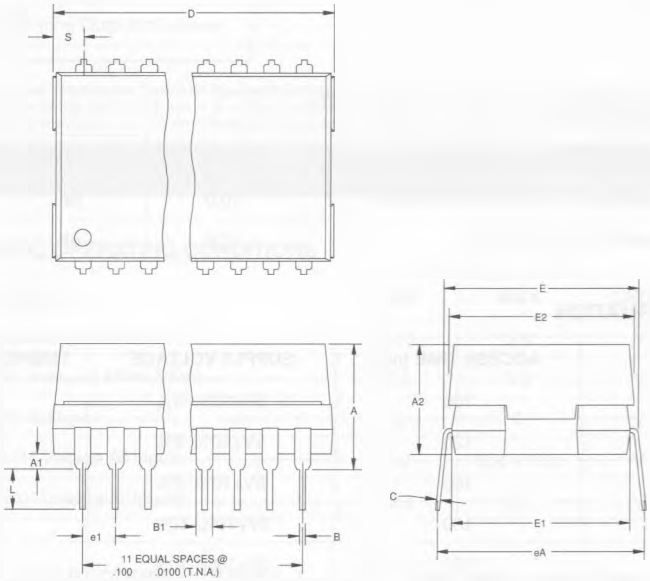
CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE	TEMPERATURE RANGE
MK48Z30-B10	100	5V+10%/-5%	0°C-70°C
MK48Z30-B12	120	5V+10%/-5%	0°C-70°C
MK48Z30-B15	150	5V+10%/-5%	0°C-70°C
MK48Z30A-B10	100	5V+10%/-10%	0°C-70°C
MK48Z30A-B12	120	5V+10%/-10%	0°C-70°C
MK48Z30A-B15	150	5V+10%/-10%	0°C-70°C

FIGURE 9 : 28 PIN BATTERY PACKAGE DESCRIPTION



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1 OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE

2 PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS

3 THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED