SGS-THOMSON MICROELECTRONICS

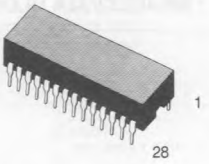
MK48Z32/32A(B) -10/12/15

32 K X 8 ZEROPOWER™ RAM

ADVANCE DATA

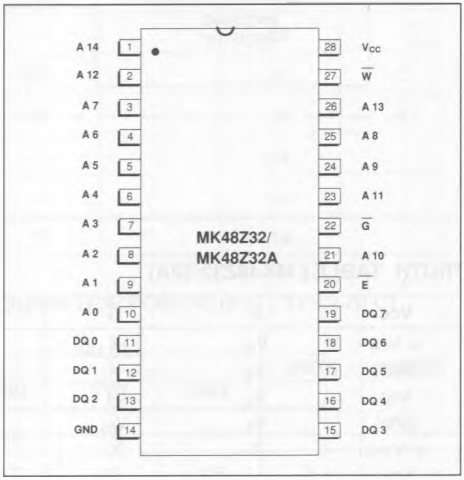
FEATURES

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED BATTERY BACK-UP OF 10 YEARS @ 25°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE:
  MK48Z30:4.75VOLTS.
  MK48Z30A: 4.50 VOLTS.



B
28-DIP
Plastic Package

PIN CONNECTIONS



DESCRIPTION

Part Number	Access Time	R/W Cycle Time	Vcc
MK48Z32 B - 10	100 ns	100 ns	+10 / -5 %
MK48Z32 B - 12	120 ns	120 ns	+10 / -5 %
MK48Z32 B - 15	150 ns	150 ns	+10 / -5 %
MK48Z32AB-10	100 ns	100 ns	+10 / -10%
MK48Z32AB-12	120 ns	120 ns	+10 / -10%
MK48Z32AB-15	150 ns	150 ns	+10 / -10%

PIN NAMES

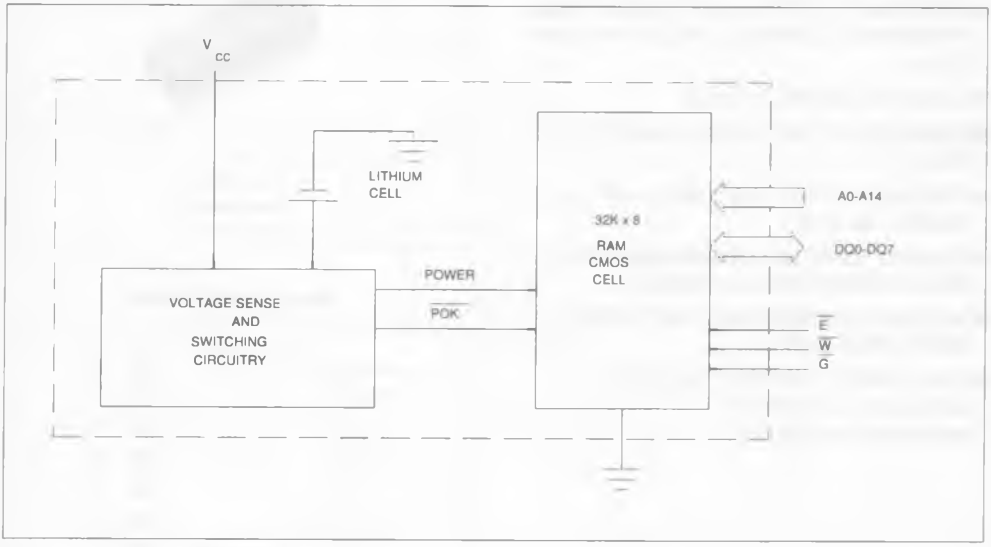
A0-A14	Address Input	Vcc	+5Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data IN/Data Out

DESCRIPTION

The MK48Z32/32A combines an 32K x 8 full CMOS S RAM and a long life carbon mono-fluoride batteries in a single plastic DIP package.The MK48Z32/32A is a nonvolatille pin and function equivalent to any JEDEC standard 32Kx 8 SRAM. it also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROM s without any requiment for special writetiming,or limitations on the number of writes that can be performed.

In addition,the MK48Z32/32A has its own Power-fail Dectect Circuit. The circuit deselect s the device whenever V_{CC} is below tolerance, providing a hight degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

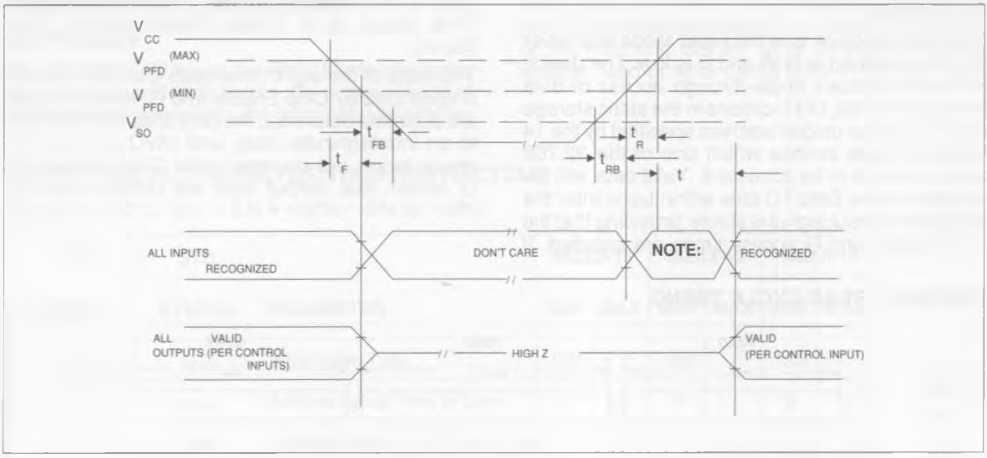
FIGURE 1 : MK48Z32/32A BLOCK DIAGRAM



TRUTH TABLE (MK48Z32/32A)

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc (Max) Vcc (Min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2 : POWER UP/DOWN TIMING



AC ELECTRICAL CHARACTERISTICS (POWER -UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} FallTime	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} FallTime	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} After Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/ DOWN TRIP POINTS) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	VALUES			UNITS	NOTES
		MIN	TYP	MAX		
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30)	4.5	4.6	4.75	V	1
V_{PFD}	Power- Fail Deselect Voltage (MK48Z30A)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	4

NOTES:

1 . All voltages referenced to GND.

2 . V_{PFD}(Max) to V_{PFD}(Min) fall times of less t_F may result in deselection/write protection not occuring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max)to (Min) fall times of less than 10 µs may cause corruption of RAM data.

3 . V_{PFD}(Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

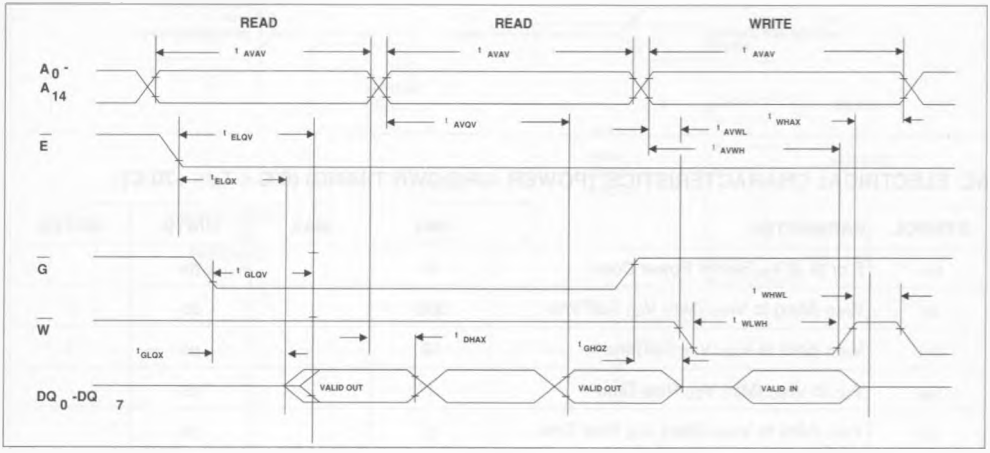
4 . 25 °C ambient condition.

READ MODE

The MK48Z32/32A is in the Read Mode whenever W (Write Enable) is high and E is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 14 Address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and G access times are satisfied. If Chip Enable or G access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and G. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until tAVQV. If the Address inputs are changed while Chip Enable and G remain low, output data will remain valid for

FIGURE 3 : READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

(0°C≤TA≤ + 70°C, VCC = 5.0 V +10% / -5%or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		ns	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		
t_{CEA1}	t_{ELQV}	$\overline{E}_1$ Access Time		100		120		150		
t_{CEZ}	t_{EHQZ}	Chip Enable Off Time		50		60		75		
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		
t_{OEL}	t_{GLQX}	Output Enable To Q Low-z	5		5		5			
t_{CEL}	t_{ELQX}	Chip Enable To Q Low-z	10		10		10			
t_{OH}	t_{DHAX}	Output Hold From Address	5		5		5			

Output Data Hold Time (t_{DHAX}) but will go indeterminate until the next Address Access.

WRITE MODE

The MK48Z32/32A is in the Write Mode whenever Write Enable and Chip select are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high or for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

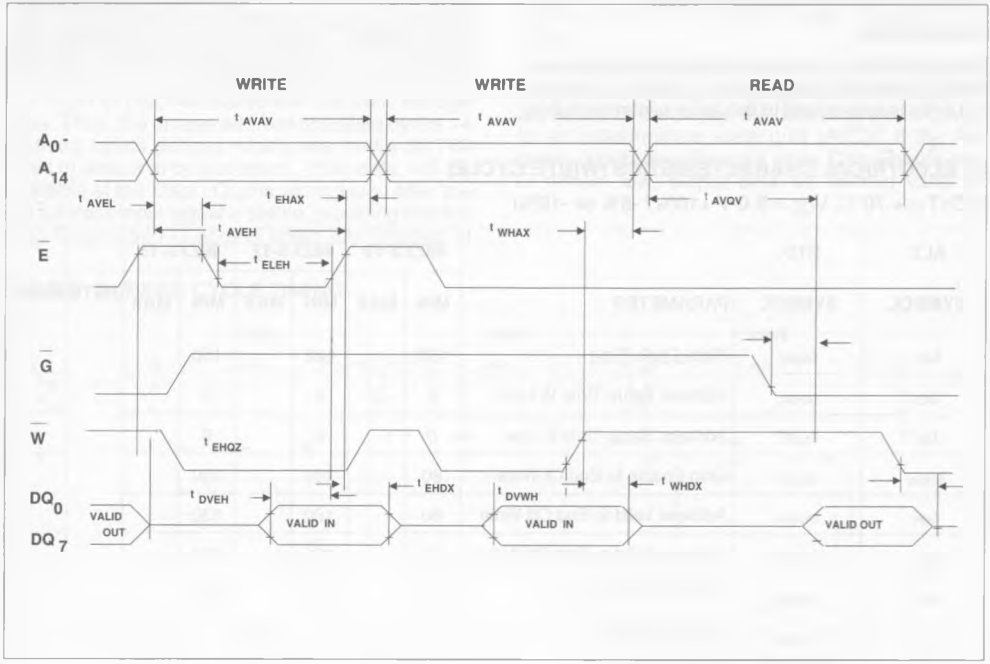
(0°C≤T_A≤+ 70°C, V_{CC} = 5.0 V +10% / -5% or -10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	48ZXX-10		48ZXX-12		48ZXX-15		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0			
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0			
t_{CEW}	t_{ELEH}	Chip Enable to End Of Write	80		100		130			
t_{AW}	t_{AVWH}	Address Valid to End Off Write	80		100		130			
t_{AW}	t_{AVEH}	Address Valid to End Off Write	80		100		130			
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100			
t_{TCEZ}	t_{EHQZ}	$\overline{E}$ Data of Time		50		60		75		
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data of Time		50		60		75		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10			1
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10			2
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low Next Cycle	10		10		10			
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70			1
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70			2
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5			1
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5			2

NOTES:

1. In a $\overline{W}$ Controlled Cycle
2. In a $\overline{E}$ Controlled Cycle

FIGURE 4 : WRITE CYCLE TIMING



ABSOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative to GND	-0.3 to + 7.0	V
Ambient Operating (V_{CC} On) Temperature (t_A)	0 to 70	°C
Ambient Storage (V_{CC} Off) Temperature	-40 to +70	°C
Total Device Power Dissipation	1.0	W
Output Current Per Pin (one Output at a Time)	50	mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION

Negative undershoots below -0.3 volts are not allowed on any pinb while in the Battery Back-up mode

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z30)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z30A)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C≤ T_A ≤+70°C) (Vcc (min) ≤ Vcc ≤ Vcc (max))

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		90	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}_1$= V_{IH} or $\overline{E}2$=V_{IL})		5	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}_1$= Vcc -0.2v)		2	mA	4
I_{IL}	Input Leakage Current (Any Input)	-2	2	µA	5
I_{OL}	Onput Leakage Current	-2	2	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 nS once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V1 ≥ GND and outputs deselected.

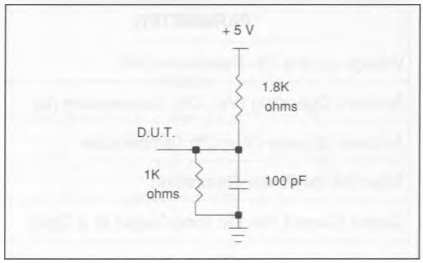
AC TEST CONDITION

Input Levels :. . . . . .0.0V to 3.0V

Transition Times :. . . . . .5 ns

Input and Output Timing
Reference Levels :. 1.5V

FIGURE 5 : OUPUT LOAD DIAGRAM



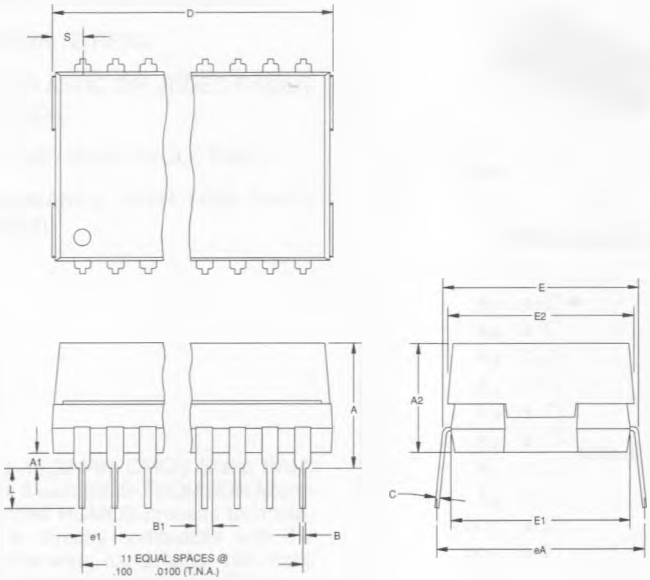
CAPACITANCE (T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2

ORDERING INFORMATION

PART NUMBER	ACCESS TIME (ns)	SUPPLY VOLTAGE	TEMPERATURE RANGE
MK48Z32(B)-10	100	5V+10%/-5%	0°C-70°C
MK48Z32(B)-12	120	5V+10%/-5%	0°C-70°C
MK48Z32(B)-15	150	5V+10%/-5%	0°C-70°C
MK48Z32A(B)-10	100	5V+10%/-10%	0°C-70°C
MK48Z32A(B)-12	120	5V+10%/-10%	0°C-70°C
MK48Z32A(B)-15	150	5V+10%/-10%	0°C-70°C

FIGURE 6 : 28 PIN BATTERY PACKAGE DESCRIPTION



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.495	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED