PRODUCT PREVIEW

MOSTEK®

MILITARY/HIGH-REL PRODUCTS

Processed to MIL-STD 883, Method 5004, Class B

Counter Timer Circuit

MKB3882 (P/J)-80/84

FEATURES

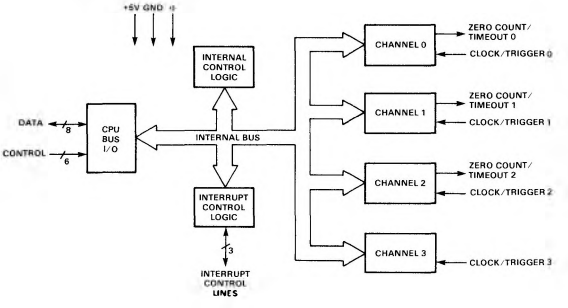
- Each channel may be selected to operate in either Counter Mode or Timer Mode
- Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- Interrupts may be programmed to occur on the zero count condition in any channel
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Typical ordering: MKB3882P-80 2.5 MHz Z80-CTC
  MKB3882P-84 4.0 MHz Z80-CTC
- Fully processed to MIL-STD-883 Method 5004 Class B. -55°C to +125°C operating range
- MKI3882 available for Industrial Hi-Rel users

DESCRIPTION

The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

A block diagram of the Z80-CTC is shown in the figure. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, Internal Control Logic, four sets of Counter/Timer Channel Logic, and Interrupt Control Logic. The four independent counter/timer channels are identified by sequential numbers from 0 to 3. The CTC has the capability of generating a unique interrupt vector for each separate channel (for automatic vectoring to an interrupt service routine). The 4 channels can be connected into four contiguous slots in the standard Z80 priority chain with channel number 0 having the highest priority. The CPU bus interface logic allows the CTC device to interface directly to the CPU with no other external logic. However, port address decoders and/or line buffers may be required for large systems.

Z80-CTC BLOCK DIAGRAM



Z80-CTC PIN CONFIGURATION