ML53612

64-Channel Full Duplex H.100/H.110 CT Bus System Interface and Tim-Slot Interface

September 1999

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OKI Semiconductor

ML53612

H.100/H.110CT Bus System Interface and Time-Slot Interchange

September 1999

1. PRODUCT DESCRIPTION

The ML53612 is a complete CT Bus system interface and time-slot interchange device that provides a cost-effective connection between a computer board's telephony interfaces or signal processing resources and the CT Bus. The ML53612 is an evolution of existing time-slot interchange ICs which offers seamless interoperability with SCbus devices.

A key element in computer telephony (CT) equipment is the auxiliary telecom bus. Most manufacturers of high-capacity CT equipment have used one or more types of telecom buses to transport and switch low-latency communications traffic between boards within the computer, bypassing the computer's main I/O and memory buses. To simplify the integration of devices that incorporate a telecom bus, the Enterprise Computer Telephony Forum (ECTF) developed a standard bus (H.100/H.110 CT Bus™) that provides compatibility modes with the most prevalent telecom buses today (SCbus™ and MVIP-90™), as well as the capacity and feature set needed to support the next generation of high capacity CT servers. The new CT Bus is embraced by Dialogic under the Signal Computing System Architecture™ (SCSA™) umbrella of open standards for building interoperable CT systems.

The ML53612 runs in both 4 MHz and 8 MHz SCbus modes and supports the switching features needed to integrate CT Bus devices with 4 MHz SCbus, 8 MHz SCbus, and 2 MHz MVIP-90 devices. Because the H.100/H.110 CT Bus uses an identical switching model and clock speeds to that used for the SCbus, developers have unparalleled flexibility in integrating these two types of devices, or in transitioning from one type to the other.

The ML53612 takes full advantage of the mandatory and optional features defined in the ECTF H.100 and H.110 interoperability specifications. It is a non-blocking 128 x 4096 time-slot switch, interfacing up to 128 ports on its parent device to any of the 4096 time-slots on the new CT Bus. The number of local time-slots available makes it easier to design low- to medium-density CT hardware, supporting up to two network interfaces or 64 voice processing ports per chip.

This powerful chip is offered in an ultra slim profile (176-pin LQFP package, with a 24 mm x 24 mm x 1.4 mm body size) that makes it possible to mount the chip on either side of the board. The chip is fully soft-ware programmable, and can be controlled by a variety of microprocessors, including Intel and Motorola in both multiplexed and nonmultiplexed modes.

2.0 FEATURES

- High functionality, low cost implementation of the ECTF H.100/H.110 interoperability specifications.
- Simple to connect PCI and cPCI™ board-level circuitry to the universally accepted CT Bus™.
- Ultra slim profiling (176-pin LQFP package).
- Up to 128 programmable connections (64 transmit and 64 receive) to any of the 4096 time-slots on the H.100/H.110 CT Bus.
- 8-channel stream-to-stream switching for data stream connections at variable rates.
- Implementation of all compatibility signals for complete interoperability with existing 4 MHz SCbus™, 8 MHz SCbus, 2 MHz MVIP-90™ devices, and H-MVIP™.
- Master PLL meets AT&T 62411 MTIE and jitter attenuation requirements to provides reliable clock synchronization for network-grade connection to digital network interfaces.
- Supports all H.100/H.110 CT Bus clock fallback features.
- Choice of constant or minimum switching delay on a per time-slot basis.
- 3.3 V I/O with 5 V tolerant input.
- Supports multiplexed and nonmultiplexed address/data bus modes for both Intel and Motorola microprocessors.
- Supports CT Bus optional message channel interface, for both H.100 (PCI) and H.110 (cPCI) applications.
- Supports a variety of framing formats via a configurable local bus.
- Efficient microprocessor interface access to Local and CT Bus data streams through direct parallel access to/from transmit and receive switch.
- Direct Parallel Access to/from Transmit and Receive switch allows efficient microprocessor interface access to local and CT Bus data streams.

2.1 Applications

- Low- to medium-density computer telephony hardware (PCI and cPCI platforms)
- Enhanced service platforms
- Private branch exchanges (PBXs)
- Wireless base stations
- Internet telephony systems
- Digital trunking equipment

3.0 PIN CONFIGURATION

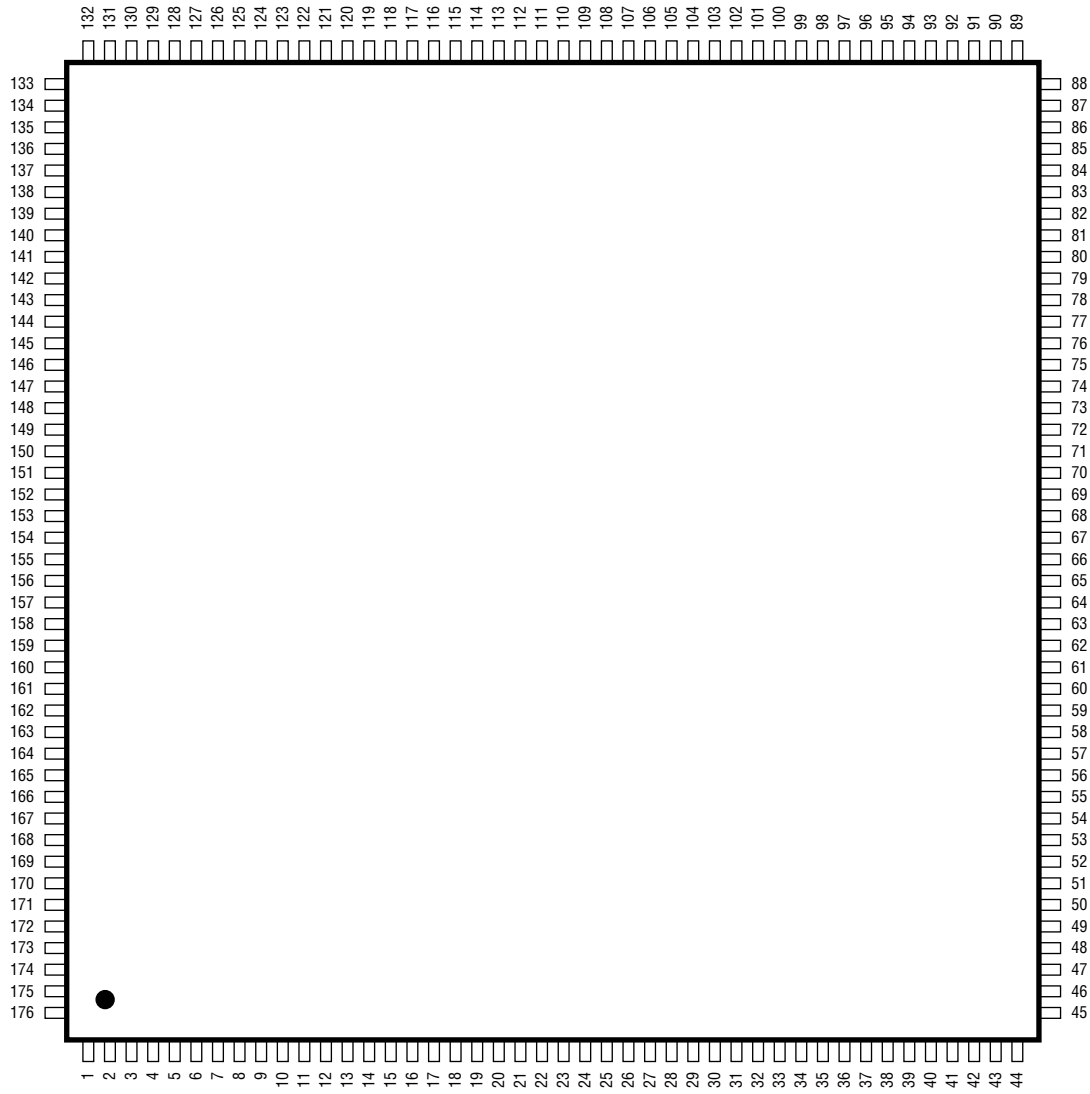


Figure 1. ML53612 176-Pin LQFP Pin Configuration

3.1 ML53612 176-Pin LQFP Pin Assignment [1]

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	VDDC	27	D_6	53	VSSO	79	VDDO	105	CT_D_9	131	CT_D_25	157	NC
2	ALE	28	A_6	54	APPL_CLKREF	80	CT_FRAME_B_N	106	CT_D_10	132	VSSC	158	NC
3	VDDO	29	D_7	55	APLL_TEST	81	VSSO	107	VDDO	133	VDDC	159	VSSO
4	CS_N	30	A_7	56	TMS	82	CT_NETREF_2	108	CT_D_11	134	CT_D_26	160	L_SO_0
5	RD_N	31	NC	57	TCK	83	CT_NETREF_1	109	VSSO	135	VDDO	161	L_SO_1
6	WR_N	32	NC	58	TRST_N	84	VDDO	110	CT_D_12	136	CT_D_27	162	NC
7	VSSO	33	NC	59	TDI	85	CT_C8_A	111	CT_D_13	137	VSSO	163	NC
8	RESET	34	VDDO	60	TDO	86	VSSO	112	VDDO	138	CT_D_28	164	VDDO
9	I_N	35	L_NETREF_0	61	VDDO	87	CT_FRAME_A_N	113	CT_D_14	139	CT_D_29	165	NC
10	INT	36	L_NETREF_1	62	MC_TXD	88	VSSC	114	VSSO	140	VDDO	166	NC
11	VDDO	37	NC	63	MC_RXD	89	VDDC	115	CT_D_15	141	CT_D_30	167	NC
12	D_0	38	NC	64	MC_CLK	90	CT_D_0	116	CT_D_16	142	CT_D_31	168	NC
13	A_0	39	VSSO	65	VSSO	91	VDDO	117	VDDO	143	VSSO	169	VSSO
14	D_1	40	NC	66	C16_NEG_N	92	CT_D_1	118	CT_D_17	144	GPIO_0	170	L_CLK_0
15	A_1	41	NC	67	C16_POS_N	93	CT_D_2	119	CT_D_18	145	GPIO_1	171	L_FS_0
16	VSSO	42	NC	68	VDDO	94	VSSO	120	VSSO	146	VDDO	172	L_CLK_1
17	D_2	43	NC	69	C4_N	95	CT_D_3	121	CT_D_19	147	GPIO_2	173	L_FS_1
18	A_2	44	VSSC	70	C2	96	CT_D_4	122	VDDO	148	GPIO_3	174	CT_D_DISABLE
19	D_3	45	VDDC	71	VSSO	97	VDDO	123	CT_D_20	149	VSSO	175	TEST
20	A_3	46	VDDO	72	SCLKX2_N	98	CT_D_5	124	VSSO	150	L_SI_0	176	VSSC
21	VDDO	47	APLL_VDDO	73	SCLK	99	VSSO	125	CT_D_21	151	L_SI_1		
22	D_4	48	APLL_VDDC	74	VDDO	100	CT_D_6	126	CT_D_22	152	NC		
23	A_4	49	APPL_PC	75	FR_COMP_N	101	VDDO	127	VDDO	153	NC		
24	D_5	50	APPL_VCO	76	CT_MC	102	CT_D_7	128	CT_D_23	154	VDDO		
25	A_5	51	APPL_VSSC	77	VSSO	103	CT_D_8	129	CT_D_24	155	NC		
26	VSSO	52	APLL_VSSO	78	CT_C8_B	104	VSSO	130	VSSO	156	NC		

1. In this document, signals ending with "_N" are "active low" (eg. CS_N). Note that in the H.100/H110 specification, active low is indicated with a preceding forward slash (eg. /CS).

4.0 SIGNAL DESCRIPTIONS

Signal Description [1]

Name	Description
D_[7:0]	Microprocessor Data Bus. (I/O, TTL Schmitt, 8 mA, 5V tolerant)
A_ [7:0]	Microprocessor Address Bus. (Input, TTL Schmitt, 5V tolerant)
ALE (AS)	Intel Bus Mode - Address Latch Enable. Motorola Bus Mode - Address Strobe. The Microprocessor Address Bus A[9:0] is latched internally on the falling edge of this signal. (Input, TTL Schmitt, 5V tolerant)
CS_N	Chip Select. This active low signal selects the ML53612 for a microprocessor read or write operation. (Input, TTL Schmitt, 5V tolerant)
RD_N (STRB_N)	Intel Bus Mode - Microprocessor Bus Read. Motorola Bus Mode - Microprocessor Bus Strobe. (Input, TTL Schmitt, 5V tolerant)
WR_N (R/W_N)	Intel Bus Mode - Microprocessor Bus Write. Motorola Bus Mode - Microprocessor Bus Read/Write signal. (Input, TTL Schmitt, 5V tolerant)
RESET	Reset. This active high input signal initializes the microprocessor interface, configuration, and routing registers. (Input, TTL Schmitt, 5V tolerant)
I_N (M)	Microprocessor Bus Mode. When this input is low, Intel Bus Mode is selected. When this input is high, Motorola Bus Mode is selected. (Input, TTL Schmitt, 5V tolerant)
CT_D_DISABLE	CT_D Global disable. (I/O, TTL Schmitt, 8 mA, 50 k Pull Up, 5V tolerant)
L_NETREF_[1:0]	Local Network Reference [1:0] Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
L_SI_[1:0]	Local bus Serial Input Data Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
MC_TXD	Message Channel Transmit Data Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
APLL_CLKREF	Analog PLL Clock Reference Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
APLL_VDDO	+3.3 Volt Analog PLL I/O Power Supply
APLL_VDDC	+3.3 Volt Analog PLL Core Power Supply
APLL_PC	Analog PLL Phase Comparator Analog Output
APLL_VCO	Analog PLL VCO Analog Input
APLL_VSSC	Analog PLL Core Ground
APLL_VSSO	Analog PLL I/O Ground
APLL_TEST	Analog PLL Test Enable Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
TEST	Test Select. This input enables the pin continuity test. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
TMS	Test Access Port Mode Select. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
TCK	Test Access Port Clock. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
TRST_N	Test Access Port Reset. (active low). (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
TDI	Test Access Port Data Input. (Input, TTL Schmitt, 50 k Pull Up, 5V tolerant)
INT	Interrupt Output. (I/O, TTL Schmitt, 50 k Pull Up, 8 mA, 5V tolerant)
CT_D_[31:0]	CT Bus Serial Data Streams. (I/O, PCI, 5V tolerant)
CT_FRAME_A_N	CT Bus "A" Frame Sync. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
CT_C8_A	CT Bus "A" 8 MHz Clock. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
CT_NETREF_1	CT Bus Network Reference 1. (I/O, PCI, 5V tolerant)
CT_NETREF_2	CT Bus Network Reference 2. (I/O, PCI, 5V tolerant)
CT_FRAME_B_N	CT Bus "B" Frame Sync. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
CT_C8_B	CT Bus "B" 8 MHz Clock. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
CT_MC	CT Bus Message Channel. (I/O, TTL Schmitt, 24 mA, 5V tolerant)

Signal Description [1]

Name	Description
FR_COMP_N	Compatibility frame sync used by SCbus, MVIP-90, and H-MVIP. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
SCLK	SCbus Clock. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
SCLKX2_N	SCbus X2 Clock. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
C2	MVIP-90 2.048 MHz Clock. (I/O, TTL Schmitt, 6 mA, 5V tolerant)
C4_N	MVIP-90 4.096 MHz Clock. (I/O, TTL Schmitt, 6 mA, 5V tolerant)
C16_POS_N	H-MVIP 16.384 MHz Positive active low Clock. High to low transition on frame boundary. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
C16_NEG_N	H-MVIP 16.384 MHz Negative active low Clock. Low to high transition on frame boundary. (I/O, TTL Schmitt, 24 mA, 5V tolerant)
L_CLK_1	Local bus Clock 1. (I/O, TTL Schmitt, 24 mA, 50 k Pull Up, 5 V tolerant)
L_FS_1	Local bus Frame Sync 1. (I/O, TTL Schmitt, 24 mA, 50 k Pull Up, 5V tolerant)
L_CLK_0	Local bus Clock 0. (I/O, TTL Schmitt, 24 mA, 50 k Pull Up, 5 V tolerant)
L_FS_0	Local bus Frame Sync 0. (I/O, TTL Schmitt, 50 k Pull Up, 24 mA, 5V tolerant)
L_SO_[1:0]	Local bus Serial Output Data Streams. (I/O, TTL Schmitt, 50 k Pull Up, 8 mA, 5V tolerant)
MC_CLK	Message Channel Clock Output. (I/O, TTL Schmitt, 50 k Pull Up, 6 mA, 5V tolerant)
MC_RXD	Message Channel Receive Data Output. (I/O, TTL Schmitt, 50 k Pull Up, 6 mA, 5V tolerant)
GPIO_[3:0]	General Purpose I/O ports. (I/O, TTL Schmitt, 24 mA, 50 k Pull Up, 5V tolerant)
TDO	Test Access Port Data Output. (Output, 6 mA, 5V tolerant)
NC	No Connect
VDDO	+3.3 Volt I/O Power Supply
VSSO	I/O Ground
VDDC	+3.3 Volt Core Power Supply
VSSC	Core Ground

1. Signals ending in "_N" are active low.

5.0 FUNCTIONAL DESCRIPTION

The ML53612 has the following interfaces:

- Microprocessor Interface
- Local Serial Data In
- Local Serial Data Out
- Local Timing
- Analog PLL Reference Clock
- CT Bus Timing
- CT Bus Serial Data

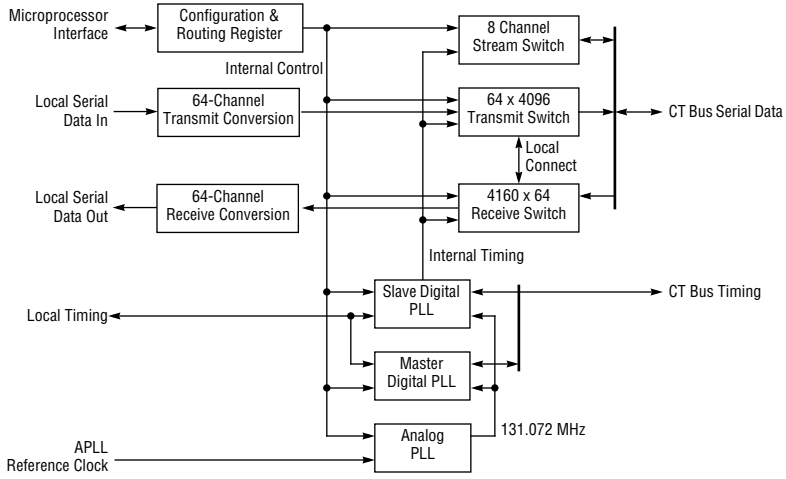


Figure 2. Block Diagram

5.1 Local Bus

The local bus consists of up to two serial input ports and two serial output ports, totalling 128 possible local bus connections to the CT Bus. The input and output ports can be configured independently as two 2 Mbps streams, one 4 Mbps stream, or one-half of an 8 Mbps stream. The chip includes two independent, configurable local clock and frame synchronization signals. The local clocks have configurable polarity and frequency that can be set to 2 MHz, 4 MHz, 8 MHz, or 16 MHz regardless of local stream data rate. The local frame syncs also have a configurable polarity and can be set to use one of three framing formats (early, straddle, or late).

To transfer data to and from the local bus, the ML53612 allows the user to select a minimum delay or constant delay buffer mode on a per channel basis. In the minimum delay mode, the input-output buffer transfer occurs on the next 2 Mbps time-slot boundary, reducing any potential channel delay for classic voice processing applications. In the constant delay mode, the buffer transfer occurs at the frame boundary for bundling and proper switching of wide-band data, for data sent on the ISDN H channel.

5.2 CT Bus

The ML53612 provides access to all 4096 CT Bus time-slots. The upper 16 data lines run at 8 Mbps, while the lower 16 data lines can be configured, in groups of four, to run at 8 Mbps, 4 Mbps, or 2 Mbps for compatibility with SCbus and MVIP-90 devices.

The chip uses an internal analog phase locked loop (PLL) as a rate multiplier to produce a 131.072 MHz internal clock locked to a variety of reference frequencies. This high frequency internal clock provides fine grained correction steps (7.6 nS) for the master and slave digital PLLs. The main CT Bus network reference signal can be configured to run at 8 kHz, 1.544 MHz, or 2048 MHz. The timing for the CT Bus can be configured to be derived from the local clock and frame sync signals to allow multiple chips to be connected to the CT Bus without overloading the reference clock line.

The ML53612 incorporates internal master digital PLL circuitry that is designed to meet the jitter attenuation, holdover and Maximum Time Interval Error (MTIE) requirements of the AT&T 62411 Stratum 3, 4 and 4E. This enables the ML53612 to be well suited for developers of digital telephone network interfaces, where reliable clock synchronization is critical. Because the circuitry is internal, board designers do not have to add expensive or custom circuitry to support these types of environments.

The ML53612 also includes an 8-channel stream-to-stream switch to connect one CT Bus data stream to another at the same or different data rates. This type of connection makes it possible for CT Bus compatible devices (such as SCbus and MVIP-90) to efficiently exchange data even though they operate at different rates. This stream switch enables switching between any of the 32 CT Bus data streams operating at 2, 4, or 8 Mbps. Depending upon the data stream rates, the stream switch provides a minimum of 256 and a maximum of 1024 unidirectional time-slot connections. Stream switches in other ML53612 devices, within a system, may be used simultaneously to increase switching capability.

5.3 Test Access Port

The ML53612 supports IEEE 1-149.1 Boundary Scan. For Normal operation, the TRST_N pin should be driven low.

5.4 Pin Continuity Test

For normal operation, the TEST pin is driven low. When the TEST pin is high, all pins except VDD, VSS, NC, APLL_PC, APLL_VCO, TMS, TCK, TRST_N, TDI, TDO, TEST are sequentially "NAND'ed" with ALE and output on TDO. This test allows each input pin to be toggled and a corresponding output to be observed on the TDO pin to verify the proper connection of the ML53612 to a printed circuit board.

5.5 Analog PLL Test

For normal operation, the APLL_TEST pin is driven low.

5.6 Microprocessor Interface

Both Intel and Motorola microprocessor bus interfaces are supported. Drive I_N (M) low for Intel mode and high for Motorola mode. Multiplexed addresses are latched on the falling edge of ALE (AS). If multiplexed address is not used, drive ALE (AS) high. Multiplexed address and data must be connected to both A_ and D_ pins.

5.7 Analog PLL

The analog PLL is used to create an internal 131.072 MHz clock locked to one of several reference frequencies. The analog PLL reference signal is input on the APLL_CLKREF pin and should be a stable clock typically ± 25 ppm. An external loop filter is required (see *Figure 3*).

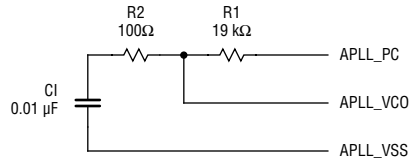


Figure 3. Analog PLL Loop Filter

5.8 Slave PLL

The slave PLL is used to generate all of the internal timing for the ML53612. Even when the ML53612 is enabled as master, the slave PLL is still in operation. The slave PLL is a fast tracking digital PLL operating at 131.072 MHz.

The slave PLL can be configured to lock to one of the following sources:

- CT_C8_A and CT_FRAME_A
- CT_C8_B and CT_FRAME_B
- SCLK and FR_COMP
- C2 and FR_COMP
- L_CLK_0 and L_FS_0
- L_CLK_1 and L_FS_1

5.9 Master PLL

The master PLL is used to generate timing for the CT Bus. The master PLL is a digital PLL operating at 131.072 MHz. When operating as primary master the PLL can lock to one of two local network references, or one of two CT Bus network references. These reference signals may be 8 kHz, 1.536 MHz, 1.544 MHz or 2.048 MHz. When operating as secondary master the PLL locks to the primary CT Bus master. The master PLL can be configured to automatically switch from secondary to primary in the event of a CT Bus timing error.

The master PLL can be configured to drive either the CT Bus "A" or "B" signals as well as all of the compatibility clocks defined in the H.100/H.110 Specifications.

When operating as the primary master, the PLL provides jitter attenuation with a cut-off frequency of 1.25 Hz and a roll-off of 20dB per decade. When operating as the secondary master, the PLL is fast tracking.

When operating as the primary master, the PLL has a lock range of ±488 ppm (minus the tolerance of APLL_CLKREF source). The maximum lock time is 3s. Holdover stability is 0.06 ppm, resulting in a frame slip rate of 42/day, assuming no drift in APLL_CLKREF source, exceeding the AT&T 62411 Stra-

tum 3 requirement of 255/day. During normal operation new holdover values are updated at 128ms intervals.

To make an MTIE compliant reference switch, enable "Condition Master PLL reference", select the "Master PLL Reference", and configure the "Master PLL Mode " to normal.The master PLL will be locked to the selected reference.

The following sequence will produce an MTIE-compliant reference switch:

1. Change the "Master PLL Mode" from Normal to Holdover. The master PLL can also be configured to make this change automatically in the event of a master PLL error.
2. Change the "Master PLL Reference Select" to the new reference, or change the reference source of CT_NETREF.
3. Change the "Master PLL Mode" back to Normal.

MTIE Specifications

	ML53612	AT&T 62411 Stratum 3 and 4E
MTIE during rearrangement	100 ns	1 µs
Phase change slope	81 ns / 1.326 ms	81 ns / 1.326 ms

5.10 Reference Master

CT_NETREF_1 and CT_NETREF_2 can be independently configured to output a reference signal to the CT Bus selected from one of two local network reference inputs. The local network references can be passed through or divided by 192, 193, or 256.

5.11 Local Clock and Frame Sync

Two sets of local clock and frame sync are provided. A variety of clock frequencies, polarities, and framing formats may be selected to allow "glue less" local port interfacing. Each set of local clock and frame sync may be configured separately. The frequency selection is independent of the local stream rate.

5.12 Local Streams

The local streams consist of up to two serial input ports and two serial output ports. The local streams can be configured to operate as two 2 Mbps streams, one 4 Mbps stream, or one-half of an 8 Mbps stream.

Local Stream Time-Slot to Channel Mapping

Local stream	8 Mbps stream rate time-slot 63:0	4 Mbps stream rate time-slot 63:0	2 Mbps stream rate time-slot 31:0
L_SI_0, L_SO_0	channel 63:0	channel 63:0	channel 31:0
L_SI_1, L_SO_1	-	-	channel 63:32

Note: When 8 Mbps stream rate is selected, time-slots 127:64 are not used.

5.13 CT Bus Streams

Connection to all 32 CT Bus streams is supported without restriction. The upper 16 streams run at 8 Mbps while the lower 16 may be configured, in groups of four, to operate at 8 Mbps, 4 Mbps, or 2 Mbps.

5.14 CT_D disable

The user may disable all CT_D output streams in the event of a bus timing error. When enabled, an error on the slave PLL reference source causes the CT_D streams to be tri-stated until an entire frame time without errors has passed. The CT_D_DISABLE signal is provided to link multiple ML53612 devices.

5.15 Diagnostic Mode

Diagnostic mode tri-states all CT Bus signals while internally looping-back CT Bus outputs to inputs. This mode allows a printed circuit board containing the ML53612 to be thoroughly tested without causing CT Bus errors.

5.16 Interrupts

The ML53612 supports the following interrupt sources:

- CT Bus A Error
- CT Bus B Error

  CT Bus A (CT Bus B) error is detected when CT_C8_A (CT_C8_B) rising edge does not occur within 35 ns of the expected time, relative to the previous period (see *Figure 4*) or when CT_FRAME_A_N (CT_FRAME_B_N) low does not occur when expected. (See ECTF H.100/H.110 Specifications for details on CT_C8_(A/B) and CT_FRAME_(A/B)_N signal timing.)

- SCbus Error

  SCbus error is detected when SCLK does not transition at close to the expected frequency (C_[25:24] determines the expected frequency) or FR_COMP_N low does not occur when expected. (See ECTF H.100/H.110 Specifications for details on SCLK, SCLKx2, and FR_COMP_N signal timing.)

- MVIP Error

  MVIP error is detected when C2 does not transition at close to 2 MHz, or FR_COMP_N low does not occur when expected. (See ECTF H.100/H.110 Specifications for details on C2 and FR_COMP_N signal timing).

- Master PLL Out of Lock Error

  Master PLL error is detected when the master PLL is not locked to the selected Reference defined by C_[43:40].

- Frame Boundary

  Frame Boundary interrupt is not an error condition, and occurs when the internal state machine crosses a frame boundary.

- GPIO

  GPIO interrupt occurs when one or more of the GPIO inputs match the programmed latch polarity, defined by C_[167:136].

The interrupts are both globally and individually maskable, and are signaled to the processor via the INT pin (pin 10). The INT pin can be configured to operate as either push-pull or open drain, and its polarity (active high or active low) is also selectable.

All of these interrupt latches have an individual enable/clear register and an individual interrupt mask register associated with them.

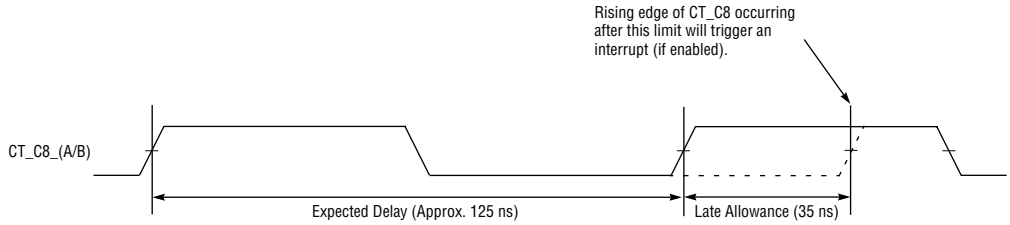


Figure 4. CT_C8_A and CT_C8_B Error Detection

5.17 GPIO Ports

Four general purpose input/output ports are provided. The ports may be individually configured to a variety of modes and can also be used as interrupt sources. Possible uses of the GPIO ports would be controlling H.100/H.110 termination switches or implementing the SCbus CLKFAIL signal.

5.18 Message Channel

The ML53612 provides a complete interface between the CT_MC CT Bus signal and a local HDLC controller. This includes generation of MC_CLK as well as buffering of MC_TXD and MC_RXD.

5.19 Law/Linear Conversion & Gain

Law/Linear conversion and/or gain are selected independently per time-slot.

The following conversions are supported:

- A to µ
- µ to A
- A to Linear
- µ to Linear
- Linear to µ
- Linear to A

A to µ and µ to A conversions are G.711 compliant (when "No gain" is selected).

Gain may be selected over a range of ± 31 dB in 1dB steps.

When conversion or gain is selected there will be an additional 1 frame (125 ms) delay through the device. To minimize delay, channels that do not require conversion or gain may by-pass the conversion and gain circuitry.

6.0 REGISTERS

6.1 Microprocessor Address Map

With Direct Parallel Access Disabled (C_[96] = 0) (Default)

A_[2:0]	Register
7h	Reserved
6h	Data Register 2 (DR_2)
5h	Data Register 1 (DR_1)
4h	Data Register 0 (DR_0)
3h	Reserved
2h	Address Register 1 (AR_1)
1h	Address Register 0 (AR_0)
0h	Command/Status Register

With Direct Parallel Access Enabled (C_[96] = 1)

A_[9:0]	Register
FFh:C0h	Direct Receive Switch Parallel Access Ch. 63:0
BFh:80h	Direct Transmit Switch Parallel Access Ch. 63:0
7Fh:08h	Reserved
07h	Reserved
06h	Data Register 2 (DR_2)
05h	Data Register 1 (DR_1)
04h	Data Register 0 (DR_0)
03h	Reserved
02h	Address Register 1 (AR_1)
01h	Address Register 0 (AR_0)
00h	Command/Status Register

6.2 Command/Status Register

D_[7:0]	Definition
0	Busy (Read Only)
1	Read Command (Write Only)
2	Write Command (Write Only)
3	Terminate Command (Write Only)
4	Reserved
5	Reserved
6	Reserved
7	Reset (Read/Write)

Busy (D_0) (Read Only)

This bit is set ("1") when a Command that requires synchronization with the ML53612's internal state machine has been initiated, and cleared ("0") when the command has been completed.
For Commands that do not require synchronization this bit is always clear ("0").
The following commands require synchronization:

- Routing Memory Write command
- In-Direct Parallel Access Read or Write command

Read (D_1) (Write Only)

Setting this bit ("1") initiates a synchronized read of the register pointed to by the Address Register. When the Busy bit is clear ("0"), the contents of the register to be read are available by reading the Data Register. It is NOT necessary to clear ("0") this bit after it has been set ("1").

Note: For "Reads" that do not require synchronization (all "Reads" except In-Direct Parallel Access Read) it is not necessary to set this bit. The Data Registers can be read immediately after writing the Address Register.

Write (D_2) (Write Only)

Setting this bit ("1") initiates a write of the register pointed to by the Address Register. It is NOT necessary to clear ("0") this bit after it has been set ("1").

Terminate (D_3) (Write Only)

Setting this bit ("1") terminates a command that requires synchronization with the ML53612's internal state machine. The command in process is completed asynchronously and the Busy bit is cleared. It is NOT necessary to clear ("0") this bit after it has been set ("1").

Reset (D_7) (Read/Write)

Setting this bit ("1") resets the ML53612 and initializes the Configuration and Routing Registers. This command is analogous to the function of the RESET pin. Clearing this bit ("0") returns the ML53612 to normal operation, ready to be configured.

6.3 Internal Address Map [1] [2]

AR	Register
0014h:0000h	Configuration
00ffh:00fch	Device ID
1007h:1000h	Stream Switch Routing Ch. 7:0
203fh:2000h	Transmit Switch Routing Ch. 63:0
303fh:3000h	Receive Switch Routing Ch. 63:0
403fh:4000h	Indirect Transmit Switch Parallel Access Ch. 63:0
503fh:5000h	Indirect Receive Switch Parallel Access Ch. 63:0
603fh:6000h	Transmit Switch Conversion Ch. 63:0
703fh:7000h	Receive Switch Parallel Conversion Ch. 63:0

1. AR is the concatenation of AR_1 and AR_0.
2. All other locations reserved (Read-back = 00, Write has no effect).

6.4 Configuration Registers

Note: All "Reserved" configuration registers should be written "0".

Configuration Register Byte 0, AR = 0000h

DR_0	C	Definition
0	0	Diagnostic Mode
1	1	Test Mode
2	2	APLL Power-down Mode
3	3	APLL Bypass Mode
[7:4]	[7:4]	APLL CLKREF Frequency [3:0]

Diagnostic Mode (C_ [0]) (Read/Write)

Set to 0 for normal operation

0 → Diagnostic Mode Disabled

1 → Diagnostic Mode Enabled (Default)

Test Mode (C_ [1]) (Read/Write)

Enables testing with the slave DPLL bypassed. Set to 0 for normal operation.

0 → Test Mode Disabled (Default)

1 → Test Mode Enabled

APLL Power-down Mode (C_ [2]) (Read/Write)

Powers down analog PLL, resets APLL charge pump. Set to 0 for normal operation.

0 → APLL Power-down Mode Disabled

1 → APLL Power-down Mode Enabled (Default)

APLL Bypass Mode (C_ [3]) (Read/Write)

APLL Bypass used during simulation and testing. Set to 0 for normal operation.

0 → APLL Bypass Mode Disabled

1 → APLL Bypass Mode Enabled (Default)

APLL CLKREF Frequency [3:0] (C_ [7:4]) (Read/Write)

Put APLL in Power-down (C_[2] = 1) when changing APLL CLKREF Frequency.

0h	→	65.536 MHz (32 X 2.048 MHz) (Default)
1h	→	49.152 MHz (24 X 2.048 MHz)
2h	→	32.768 MHz (16 X 2.048 MHz)
3h	→	16.384 MHz (8 X 2.048 MHz)
4h	→	8.192 MHz (4 X 2.048 MHz)
5h	→	4.096 MHz (2 X 2.048 MHz)
6h	→	2.048 MHz
7h	→	Reserved
8h	→	49.408 MHz (32 X 1.544 MHz)
9h	→	37.056 MHz (24 X 1.544 MHz)
Ah	→	24.704 MHz (16 X 1.544 MHz)
Bh	→	12.352 MHz (8 X 1.544 MHz)
Ch	→	6.176 MHz (4 X 1.544 MHz)
Dh	→	3.088 MHz (2 X 1.544 MHz)
Eh	→	1.544 MHz
Fh	→	1.536 MHz

Configuration Register Byte 1, AR = 0001h

DR_0	C	Definition
[1:0]	[9:8]	Slave Bus Mode [1:0]
2	10	Slave Local Timing Source Select
3	11	Advance Slave PLL Timing
4	12	Slave CT Manual/Auto Mode
5	13	Slave CT A/B Select
6	14	Slave CT A/B Read-back
7	15	Reserved

Slave Bus Mode [1:0] (C_ [9:8]) (Read/Write) [1]

00 → CT Bus - Slave to CT_C8 & CT_FRAME (see Slave CT A/B Select) (Default)
01 → SCbus - Slave to SCLK & FR_COMP
10 → MVIP - Slave to C2 & FR_COMP
11 → Local - Slave to L_CLK & L_FS (see Slave Local Timing Source Select)

1. When local slave mode is selected, L_CLK frequency, polarity and output enable, and L_FS polarity, position and output enable must be configured accordingly.

Slave Local Timing Source Select (C_ [10]) (Read/Write)

0 → L_CLK_0, L_FS_0 (Default)
1 → L_CLK_1, L_FS_1

Advance Slave PLL Timing (C_ [11]) (Read/Write)

The slave PLL timing may be advanced one 7.6 ns period to compensate for delay. Set to 0 for normal operation.

0 → Advance Slave PLL Timing Disabled (Default)
1 → Advance Slave PLL Timing Enabled

Slave CT Manual/Auto Mode (C_ [12]) (Read/Write) [1]

0 → Slave CT Manual Mode (Default)
1 → Slave CT Auto Mode

1. In auto mode, slave will only switch when an error exists on the current signal set and NOT on the other signal set.

Slave CT A/B Select (C_ [13]) (Read/Write)

Select signal set in manual mode then switch to auto.

0 → CT A Select (Default)
1 → CT B Select

Slave CT A/B Read-back (C_ [14]) (Read Only)

0 → CT A Selected
1 → CT B Selected

Configuration Register Byte 2, AR = 0002h

DR_0	C	Definition
0	16	Master CT Enable
1	17	Master CT A/B Select
2	18	Reserved
3	19	Advance Master PLL Timing
4	20	Master Manual/Auto Mode
5	21	Master Primary/Secondary Select
6	22	Master Primary/Secondary Read-back
7	23	Reserved

Master CT Enable (C_ [16]) (Read/Write)

Enables the Master PLL to drive the CT Bus.

0 → Master Disabled (Default)

1 → Master Enabled

Master CT A/B Select (C_ [17]) (Read/Write) [1]

Selects the signal set driven by the Master PLL.

0 → CT_C8_A & CT_FRAME_A (Default)

1 → CT_C8_B & CT_FRAME_B

1. When in Secondary Master mode, the signal set (A or B) NOT selected here is used as the reference.

Advance Master PLL Timing (C_ [19]) (Read/Write)

When operating as secondary master, the master PLL timing may be advanced one 7.6 ns clock period to compensate for delay.
Set to 0 for normal operation.

0 → Advance Master PLL Timing Disabled (Default)

1 → Advance Master PLL Timing Enabled

Master Manual/Auto Mode (C_ [20]) (Read/Write) [1]

0 → Master Manual Mode (Default)

1 → Master Auto Mode

1. Master Auto mode allows Secondary Master to become Primary if an error occurs on the reference signal set. To switch back to Secondary Master it is necessary to go into manual mode.

Master Primary/Secondary Select (C_ [21]) (Read/Write)

0 → Primary Master Select (Default)

1 → Secondary Master Select

Master Primary/Secondary Read-back (C_ [22]) (Read Only)

0 → Primary Master Selected

1 → Secondary Master Selected

Configuration Register Byte 3, AR = 0003h

DR_0	C	Definition
[1:0]	[25:24]	SCbus SCLK Frequency [1:0]
2	26	SCbus Master Enable - SCLK, SCLKX2 & FR_COMP
3	27	Reserved
4	28	MVIP-90 Master Enable - C2, C4 & FR_COMP
5	29	H-MVIP Master Enable - C2, C4, C16 & FR_COMP
6	30	Reserved
7	31	Reserved

SCbus SCLK Frequency [1:0] (C_ [25:24]) (Read/Write)

00 → 2.048 MHz (Default)
01 → 4.096 MHz
10 → 8.192 MHz
11 → Reserved

SCbus Master Enable (C_ [26]) (Read/Write)

When enabled as Primary Master, this register enables the SCLK, SCLKX2 & FR_COMP signals to be driven.

0 → SCbus Master Disabled (Default)
1 → SCbus Master Enabled

MVIP-90 Master Enable (C_ [28]) (Read/Write)

When enabled as Primary Master, this register enables the C2, C4 & FR_COMP signals to be driven.

0 → MVIP-90 Master Disabled (Default)
1 → MVIP-90 Master Enabled

H-MVIP Master Enable (C_ [29]) (Read/Write)

When enabled as Primary Master, this register enables the C2, C4, C16 & FR_COMP signals to be driven.

0 → H-MVIP Master Disabled (Default)
1 → H-MVIP Master Enabled

Configuration Register Byte 4, AR = 0004h

DR_0	C	Definition
[2:0]	[34:32]	Master PLL Mode [2:0]
3	35	Reserved
[5:4]	[37:36]	Master PLL Mode Read-back [1:0]
6	38	Condition Master PLL Reference
7	39	Reserved

Master PLL Mode [2:0] (C_ [34:32]) (Read/Write) [1]

000 → Normal (Default)
001 → Reserved
010 → Holdover
011 → Free Run
100 → Reserved
101 → Reserved
110 → Auto Normal to Holdover switch on Master PLL error
111 → Auto Normal to Free Run switch on Master PLL error

1. Master PLL error occurs when the Master PLL is out of lock with its reference signal. It is necessary to manually select "Normal" to go back to normal operation after an auto switch has occurred.

Master PLL Mode Read-back [1:0] (C_ [37:36]) (Read Only)

00 → Normal
01 → Reserved
10 → Holdover
11 → Free Run

Condition Master PLL Reference (C_ [38]) (Read/Write)

When enabled, conditions a change in references for MTIE compatibility.

0 → Condition Master PLL Reference Disabled (Default)
1 → Condition Master PLL Reference Enabled

Configuration Register Byte 5, AR = 0005h

DR_0	C	Definition
[3:0]	[43:40]	Master PLL Reference Select [3:0]
4	44	Reserved
[6:5]	[46:45]	Master PLL Reference Frequency [1:0]
7	47	Reserved

Master PLL Reference Select [3:0] (C_ [43:40]) (Read/Write)

0h → None (Default)
1h → Reserved
2h → Reserved
3h → Reserved
4h → Reserved
5h → Reserved
6h → CT_NETREF_1
7h → CT_NETREF_2
8h → L_NETREF_0
9h → L_NETREF_1
ah → Reserved
bh → Reserved
ch → Reserved
dh → Reserved
eh → Reserved
fh → Reserved

Master PLL Reference Frequency [1:0] (C_ [46:45]) (Read/Write)

00 → 8 kHz (Default)
01 → 1.536 MHz
10 → 1.544 MHz
11 → 2.048 MHz

Configuration Register Byte 6, AR = 0006h

DR_0	C	Definition
[3:0]	[51:48]	CT_NETREF_1 Source Select [3:0]
4	52	Reserved
[6:5]	[54:53]	CT_NETREF_1 Divider [1:0]
7	55	CT_NETREF_1 Output Enable

CT_NETREF_1 Source Select [3:0] (C_ [51:48]) (Read/Write)

0h → None (Default)
1h → Reserved
2h → Reserved
3h → Reserved
4h → Reserved
5h → Reserved
6h → Reserved
7h → Reserved
8h → L_NETREF_0
9h → L_NETREF_1
ah → Reserved
bh → Reserved
ch → Reserved
dh → Reserved
eh → Reserved
fh → Reserved

CT_NETREF_1 Divider [1:0] (C_ [54:53]) (Read/Write)

00 → Divide source by 1 (Default)
01 → Divide source by 192
10 → Divide source by 193
11 → Divide source by 256

CT_NETREF_1 Output Enable (C_ [55]) (Read/Write)

0 → CT_NETREF_1 Output Tri-stated (Default)
1 → CT_NETREF_1 Output Enabled

Configuration Register Byte 7, AR = 0007h

DR_0	C	Definition
[3:0]	[59:56]	CT_NETREF_2 Source Select [3:0]
4	60	Reserved
[6:5]	[62:61]	CT_NETREF_2 Divider [1:0]
7	63	CT_NETREF_2 Output Enable

CT_NETREF_2 Source Select [3:0] (C_ [59:56]) (Read/Write)

0h → None (Default)
1h → Reserved
2h → Reserved
3h → Reserved
4h → Reserved
5h → Reserved
6h → Reserved
7h → Reserved
8h → L_NETREF_0
9h → L_NETREF_1
ah → Reserved
bh → Reserved
ch → Reserved
dh → Reserved
eh → Reserved
fh → Reserved

CT_NETREF_2 Divider [1:0] (C_ [62:61]) (Read/Write)

00 → Divide source by 1 (Default)
01 → Divide source by 192
10 → Divide source by 193
11 → Divide source by 256

CT_NETREF_2 Output Enable (C_ [63]) (Read/Write)

0 → CT_NETREF_2 Output Tri-stated (Default)
1 → CT_NETREF_2 Output Enabled

Configuration Register Byte 8, AR = 0008h

DR_0	C	Definition
0	64	L_CLK_0, L_FS_0 Output Enable
1	65	L_CLK_1, L_FS_1 Output Enable
2	66	CT_D_ Output Enable Mode
3	67	CT_D_DISABLE Output Enable
4	68	CT_D_DISABLE
5	69	CT_D_DISABLE On Input
6	70	CT_D_DISABLE On Error
7	71	CT_D_DISABLE Read-back

L_CLK_0, L_FS_0 Output Enable (C_ [64]) (Read/Write)

0 → L_CLK_0, L_FS_0 Output Tri-stated (Default)
1 → L_CLK_0, L_FS_0 Output Enabled

L_CLK_1, L_FS_1 Output Enable (C_ [65]) (Read/Write)

0 → L_CLK_1, L_FS_1 Output Tri-stated (Default)
1 → L_CLK_1, L_FS_1 Output Enabled

CT_D_ Output Enable Mode (C_ [66]) (Read/Write)

0 → CT_D_[31:0] Output Tri-stated before bit cell boundary - Based on H.100/H.110 (Default)
1 → CT_D_[31:0] Output Tri-stated at bit cell boundary

CT_D_DISABLE Output Enable (C_ [67]) (Read/Write)

0 → CT_D_DISABLE pin Output Tri-stated (Default)
1 → CT_D_DISABLE pin Output Enabled

CT_D_DISABLE (C_ [68]) (Read/Write)

0 → CT_D_ Outputs Enabled (Default)
1 → CT_D_ Outputs Disabled

CT_D_DISABLE On Input (C_ [69]) (Read/Write)

0 → CT_D_DISABLE On Input Disabled (Default)
1 → CT_D_DISABLE On Input Enabled

CT_D_DISABLE On Error (C_ [70]) (Read/Write)

0 → CT_D_DISABLE On Error Disabled (Default)
1 → CT_D_DISABLE On Error Enabled

CT_D_DISABLE Read-back (C_ [71]) (Read Only)

0 → CT_D_ Outputs Enabled
1 → CT_D_ Outputs Disabled

Configuration Register Byte 9, AR = 0009h

DR_0	C	Definition
[1:0]	[73:72]	L_SI_[1:0], L_SO_[1:0] Stream Rate [1:0]
[3:2]	[75:74]	L_CLK_0 Frequency [1:0]
4	76	L_CLK_0 Polarity
5	77	L_FS_0 Polarity
[7:6]	[79:78]	L_FS_0 Position [1:0]

L_SI_[1:0], L_SO_[1:0] Stream Rate [1:0] (C_ [73:72]) (Read/Write)

00 → 2.048 Mbps (L_SI_[1:0], L_SO_[1:0]) (Default)
01 → 4.096 Mbps (L_SI_[0], L_SO_[0])
10 → 8.192 Mbps (L_SI_[0], L_SO_[0])
11 → Reserved

L_CLK_0 Frequency [1:0] (C_ [75:74]) (Read/Write)

00 → 2.048 MHz (Default)
01 → 4.096 MHz
10 → 8.192 MHz
11 → 16.384 MHz

L_CLK_0 Polarity (C_ [76]) (Read/Write)

0 → L_CLK_0 Non-Inverted (Default)
1 → L_CLK_0 Inverted

L_FS_0 Polarity (C_ [77]) (Read/Write)

0 → L_FS_0 Non-Inverted (Default)
1 → L_FS_0 Inverted

L_FS_0 Position [1:0] (C_ [79:78]) (Read/Write)

00 → Early - L_FS_0 occurs during the last L_CLK_0 period of the frame (Default)
01 → Straddle - L_FS_0 straddles the frame boundary
10 → Late - L_FS_0 occurs during the first L_CLK_0 period of the frame
11 → Reserved

Configuration Register Byte 10, AR = 000ah

DR_0	C	Definition
[1:0]	[81:80]	Reserved
[3:2]	[83:82]	L_CLK_1 Frequency [1:0]
4	84	L_CLK_1 Polarity
5	85	L_FS_1 Polarity
[7:6]	[87:86]	L_FS_1 Position [1:0]

L_CLK_1 Frequency [1:0] (C_ [83:82]) (Read/Write)

00 → 2.048 MHz (Default)
01 → 4.096 MHz
10 → 8.192 MHz
11 → 16.384 MHz

L_CLK_1 Polarity (C_ [84]) (Read/Write)

0 → L_CLK_1 Non-Inverted (Default)
1 → L_CLK_1 Inverted

L_FS_1 Polarity (C_ [85]) (Read/Write)

0 → L_FS_1 Non-Inverted (Default)
1 → L_FS_1 Inverted

L_FS_1 Position [1:0] (C_ [87:86]) (Read/Write)

00 → Early - L_FS_1 occurs during the last L_CLK_1 period of the frame (Default)
01 → Straddle - L_FS_1 straddles the frame boundary
10 → Late - L_FS_1 occurs during the first L_CLK_1 period of the frame
11 → Reserved

Configuration Register Byte 11, AR = 000bh

DR_0	C	Definition
[1:0]	[89:88]	CT_D_[3:0] Data Stream Rate [1:0]
[3:2]	[91:90]	CT_D_[7:4] Data Stream Rate [1:0]
[5:4]	[93:92]	CT_D_[11:8] Data Stream Rate [1:0]
[7:6]	[95:94]	CT_D_[15:12] Data Stream Rate [1:0]

CT_D_[3:0] Data Stream Rate [1:0] (C_ [89:88]) (Read/Write)

00 → 2.048 Mbps
01 → 4.096 Mbps
10 → 8.192 Mbps (Default)
11 → Reserved

CT_D_[7:4] Data Stream Rate [1:0] (C_ [91:90]) (Read/Write)

00 → 2.048 Mbps
01 → 4.096 Mbps
10 → 8.192 Mbps (Default)
11 → Reserved

CT_D_[11:8] Data Stream Rate [1:0] (C_ [93:92]) (Read/Write)

00 → 2.048 Mbps
01 → 4.096 Mbps
10 → 8.192 Mbps (Default)
11 → Reserved

CT_D_[15:12] Data Stream Rate [1:0] (C_ [95:94]) (Read/Write)

00 → 2.048 Mbps
01 → 4.096 Mbps
10 → 8.192 Mbps (Default)
11 → Reserved

Configuration Register Byte 12, AR = 000ch

DR_0	C	Definition
0	96	Direct Parallel Access Enable
1	97	Microprocessor Watchdog Enable
2	98	APLL Clock Watchdog Enable
3	99	Reserved
4	100	Message Channel Registered TXD Enable
5	101	Message Channel Output Disable
6	102	Reserved
7	103	Reserved

Direct Parallel Access Enable (C_ [96]) (Read/Write)

0 → Direct Parallel Access disabled (Default)

1 → Direct Parallel Access enabled

Microprocessor Watchdog Enable (C_ [97]) (Read/Write)

When enabled, the ML53612 enters into reset after the Analog PLL clocks for 256mS (± 50%).
Each time C_[97] is cleared (0) and then set (1), the microprocessor watchdog count is reset.

0 → Microprocessor Watchdog disabled (Default)

1 → Microprocessor Watchdog enabled

APLL Clock Watchdog Enable (C_ [98]) (Read/Write)

When enabled, C_[98] will read back as being set (1) until the Analog PLL clocks for 125 µS (± 50%), then will read back as being cleared (0). Each time C_[98] is cleared (0) and then set (1), the clock watchdog count is reset.

0 → APLL Clock Watchdog disabled (Default)

1 → APLL Clock Watchdog enabled

Message Channel Registered TXD Enable (C_ [100]) (Read/Write)

0 → MC_TXD passed though to CT_MC (Default)

1 → MC_TXD registered to CT_MC on rising edge of MC_CLK

Message Channel Output Disable with Loop-back (C_ [101]) (Read/Write)

When CT_MC output is disabled, the local message channel circuitry can be tested without disturbing the CT Bus.

0 → CT_MC Output enabled (Default)

1 → CT_MC Output Tri-stated, MC_TXD looped back to MC_RXD

Configuration Register Byte 13, AR = 000dh

DR_0	C	Definition
0	104	INT Polarity
1	105	INT Mask
2	106	INT Output Driver Configuration
3	107	INT
4	108	Reserved
5	109	Reserved
6	110	Reserved
7	111	Reserved

INT Polarity (C_ [104]) (Read/Write)

0 → INT Active Low (Default)
1 → INT Active High

INT Mask (C_ [105]) (Read/Write)

0 → INT Unmasked
1 → INT Masked (Default)

INT Output Driver Configuration (C_ [106]) (Read/Write)

0 → Open Drain (Default)
1 → Push-Pull

INT (C_ [107]) (Read Only)

This register is the logical or of all unmasked interrupt sources.

0 → All unmasked interrupts false
1 → Any unmasked interrupt true

Configuration Register Byte 14, AR = 000eh [1]

DR_0	C	Definition
0	112	CT Bus A Error Interrupt Mask
1	113	CT Bus B Error Interrupt Mask
2	114	SCbus Error Interrupt Mask
3	115	MVIP Error Interrupt Mask
4	116	Master PLL Error Interrupt Mask
5	117	Frame Boundary Interrupt Mask
6	118	Reserved
7	119	Reserved

1. Masking an interrupt disables that interrupt from being OR'ed together with other interrupts to the INT pin. The state of the latches are accessible while masked (polling mode).

CT Bus A Error Interrupt Mask (C_ [112]) (Read/Write)

0 → CT Bus A Error Interrupt Unmasked

1 → CT Bus A Error Interrupt Masked (Default)

CT Bus B Error Interrupt Mask (C_ [113]) (Read/Write)

0 → CT Bus B Error Interrupt Unmasked

1 → CT Bus B Error Interrupt Masked (Default)

SCbus Error Interrupt Mask (C_ [114]) (Read/Write)

0 → SCbus Error Interrupt Unmasked

1 → SCbus Error Interrupt Masked (Default)

MVIP Error Interrupt Mask (C_ [115]) (Read/Write)

0 → MVIP Error Interrupt Unmasked

1 → MVIP Error Interrupt Masked (Default)

Master PLL Error Interrupt Mask (C_ [116]) (Read/Write)

0 → Master PLL Error Interrupt Unmasked

1 → Master PLL Error Interrupt Masked (Default)

Frame Boundary Interrupt Mask (C_ [117]) (Read/Write)

0 → Frame Boundary Interrupt Unmasked

1 → Frame Boundary Interrupt Masked (Default)

Configuration Register Byte 15, AR = 000fh

DR_0	C	Definition
0	120	CT Bus A Error Latch Clear
1	121	CT Bus B Error Latch Clear
2	122	SCbus Error Latch Clear
3	123	MVIP Error Latch Clear
4	124	Master PLL Error Latch Clear
5	125	Frame Boundary Latch Clear
6	126	Reserved
7	127	Reserved

CT Bus A Error Latch Clear (C_ [120]) (Read/Write)

0 → CT Bus A Error Latch Enabled
1 → CT Bus A Error Latch held clear (Default)

CT Bus B Error Latch Clear (C_ [121]) (Read/Write)

0 → CT Bus B Error Latch Enabled
1 → CT Bus B Error Latch held clear (Default)

SCbus Error Latch Clear (C_ [122]) (Read/Write)

0 → SCbus Error Latch Enabled
1 → SCbus Error Latch held clear (Default)

MVIP Error Latch Clear (C_ [123]) (Read/Write)

0 → MVIP Error Latch Enabled
1 → MVIP Error Latch held clear (Default)

Master PLL Error Latch Clear (C_ [124]) (Read/Write)

0 → Master PLL Error Latch Enabled
1 → Master PLL Error Latch held clear (Default)

Frame Boundary Latch Clear (C_ [125]) (Read/Write)

0 → Frame Boundary Latch Enabled
1 → Frame Boundary Latch held clear (Default)

Configuration Register Byte 16, AR = 0010h

DR_0	C	Definition
0	128	CT Bus A Error Latch
1	129	CT Bus B Error Latch
2	130	SCbus Error Latch
3	131	MVIP Error Latch
4	132	Master PLL Error Latch
5	133	Frame Boundary Latch
6	134	Reserved
7	135	Reserved

CT Bus A Error Latch (C_ [128]) (Read Only)

0 → CT Bus A Error Latch False
1 → CT Bus A Error Latch True

CT Bus B Error Latch (C_ [129]) (Read Only)

0 → CT Bus B Error Latch False
1 → CT Bus B Error Latch True

SCbus Error Latch (C_ [130]) (Read Only)

0 → SCbus Error Latch False
1 → SCbus Error Latch True

MVIP Error Latch (C_ [131]) (Read Only)

0 → MVIP Error Latch False
1 → MVIP Error Latch True

Master PLL Error Latch (C_ [132]) (Read Only)

0 → Master PLL Error Latch False
1 → Master PLL Error Latch True

Frame Boundary Latch (C_ [133]) (Read Only)

0 → Frame Boundary Latch False
1 → Frame Boundary Latch True

Configuration Register Byte 17, AR = 0011h

DR_0	C	Definition
0	136	GPIO_0 Input
1	137	GPIO_0 Output
2	138	GPIO_0 Output Enable
3	139	GPIO_0 Output Driver Configuration
4	140	GPIO _0 Latch Polarity
5	141	GPIO _0 Interrupt Mask
6	142	GPIO _0 Latch Clear
7	143	GPIO _0 Latch

GPIO_0 Input (C_ [136]) (Read Only)

0 → GPIO_0 Input = 0
1 → GPIO_0 Input = 1

GPIO_0 Output (C_ [137]) (Read/Write)

0 → GPIO_0 Output = 0 (Default)
1 → GPIO_0 Output = 1

GPIO_0 Output Enable (C_ [138]) (Read/Write)

0 → GPIO_0 Output Tri-stated (Default)
1 → GPIO_0 Output Enabled

GPIO_0 Output Driver Configuration (C_ [139]) (Read/Write)

0 → Open Drain (Default)
1 → Push-Pull

GPIO _0 Latch Polarity (C_ [140]) (Read/Write)

0 → GPIO _0 Latch set when GPIO_0 input = 0 (Default)
1 → GPIO _0 Latch set when GPIO_0 input = 1

GPIO _0 Interrupt Mask (C_ [141]) (Read/Write)

0 → GPIO _0 Interrupt Unmasked
1 → GPIO _0 Interrupt Masked (Default)

GPIO _0 Latch Clear (C_ [142]) (Read/Write)

0 → GPIO _0 Latch Enabled
1 → GPIO _0 Latch held clear (Default)

GPIO _0 Latch (C_ [143]) (Read Only)

0 → GPIO _0 Latch False
1 → GPIO _0 Latch True

Configuration Register Byte 18, AR = 0012h

DR_0	C	Definition
0	144	GPIO_1 Input
1	145	GPIO_1 Output
2	146	GPIO_1 Output Enable
3	147	GPIO_1 Output Driver Configuration
4	148	GPIO _1 Latch Polarity
5	149	GPIO _1 Interrupt Mask
6	150	GPIO _1 Latch Clear
7	151	GPIO _1 Latch

GPIO_1 Input (C_ [144]) (Read Only)

0 → GPIO_1 Input = 0
1 → GPIO_1 Input = 1

GPIO_1 Output (C_ [145]) (Read/Write)

0 → GPIO_1 Output = 0 (Default)
1 → GPIO_1 Output = 1

GPIO_1 Output Enable (C_ [146]) (Read/Write)

0 → GPIO_1 Output Tri-stated (Default)
1 → GPIO_1 Output Enabled

GPIO_1 Output Driver Configuration (C_ [147]) (Read/Write)

0 → Open Drain (Default)
1 → Push-Pull

GPIO _1 Latch Polarity (C_ [148]) (Read/Write)

0 → GPIO _1 Latch set when GPIO_1 input = 0 (Default)
1 → GPIO _1 Latch set when GPIO_1 input = 1

GPIO _1 Interrupt Mask (C_ [149]) (Read/Write)

0 → GPIO _1 Interrupt Unmasked
1 → GPIO _1 Interrupt Masked (Default)

GPIO _1 Latch Clear (C_ [150]) (Read/Write)

0 → GPIO _1 Latch Enabled
1 → GPIO _1 Latch held clear (Default)

GPIO _1 Latch (C_ [151]) (Read Only)

0 → GPIO _1 Latch False
1 → GPIO _1 Latch True

Configuration Register Byte 19, AR = 0013h

DR_0	C	Definition
0	152	GPIO_2 Input
1	153	GPIO_2 Output
2	154	GPIO_2 Output Enable
3	155	GPIO_2 Output Driver Configuration
4	156	GPIO _2 Latch Polarity
5	157	GPIO _2 Interrupt Mask
6	158	GPIO _2 Latch Clear
7	159	GPIO _2 Latch

GPIO_2 Input (C_ [152]) (Read Only)

0 → GPIO_2 Input = 0
1 → GPIO_2 Input = 1

GPIO_2 Output (C_ [153]) (Read/Write)

0 → GPIO_2 Output = 0 (Default)
1 → GPIO_2 Output = 1

GPIO_2 Output Enable (C_ [154]) (Read/Write)

0 → GPIO_2 Output Tri-stated (Default)
1 → GPIO_2 Output Enabled

GPIO_2 Output Driver Configuration (C_ [155]) (Read/Write)

0 → Open Drain (Default)
1 → Push-Pull

GPIO _2 Latch Polarity (C_ [156]) (Read/Write)

0 → GPIO _2 Latch set when GPIO_2 input = 0 (Default)
1 → GPIO _2 Latch set when GPIO_2 input = 1

GPIO _2 Interrupt Mask (C_ [157]) (Read/Write)

0 → GPIO _2 Interrupt Unmasked
1 → GPIO _2 Interrupt Masked (Default)

GPIO _2 Latch Clear (C_ [158]) (Read/Write)

0 → GPIO _2 Latch Enabled
1 → GPIO _2 Latch held clear (Default)

GPIO _2 Latch (C_ [159]) (Read Only)

0 → GPIO _2 Latch False
1 → GPIO _2 Latch True

Configuration Register Byte 20, AR = 0014h

DR_0	C	Definition
0	160	GPIO_3 Input
1	161	GPIO_3 Output
2	162	GPIO_3 Output Enable
3	163	GPIO_3 Output Driver Configuration
4	164	GPIO _3 Latch Polarity
5	165	GPIO _3 Interrupt Mask
6	166	GPIO _3 Latch Clear
7	167	GPIO _3 Latch

GPIO_3 Input (C_ [160]) (Read Only)

0 → GPIO_3 Input = 0
1 → GPIO_3 Input = 1

GPIO_3 Output (C_ [161]) (Read/Write)

0 → GPIO_3 Output = 0 (Default)
1 → GPIO_3 Output = 1

GPIO_3 Output Enable (C_ [162]) (Read/Write)

0 → GPIO_3 Output Tri-stated (Default)
1 → GPIO_3 Output Enabled

GPIO_3 Output Driver Configuration (C_ [163]) (Read/Write)

0 → Open Drain (Default)
1 → Push-Pull

GPIO _3 Latch Polarity (C_ [164]) (Read/Write)

0 → GPIO _3 Latch set when GPIO_3 input = 0 (Default)
1 → GPIO _3 Latch set when GPIO_3 input = 1

GPIO _3 Interrupt Mask (C_ [165]) (Read/Write)

0 → GPIO _3 Interrupt Unmasked
1 → GPIO _3 Interrupt Masked (Default)

GPIO _3 Latch Clear (C_ [166]) (Read/Write)

0 → GPIO _3 Latch Enabled
1 → GPIO _3 Latch held clear (Default)

GPIO _3 Latch (C_ [167]) (Read Only)

0 → GPIO _3 Latch False
1 → GPIO _3 Latch True

6.5 Device ID Registers (Read Only)

Device ID byte 3, AR = 00ffh

DR_0	Definition
[7:4]	Version [3:0]
[3:0]	Part Number [15:12]

Device ID byte 2, AR = 00feh

DR_0	Definition
[7:0]	Part Number [11:4]

Device ID byte 1, AR = 00fdh

DR_0	Definition
[7:4]	Part Number [3:0]
[3:0]	Manufacturer ID [10:7]

Device ID byte 0, AR = 00fch

DR_0	Definition
[7:1]	Manufacturer ID [6:0]
[0]	0 = Device does not support Boundary Scan
	1 = Device supports Boundary Scan

Note: Device ID byte [3:0] for the MG73Q011-181TC (engineering sample) = 00 6c 00 5dh

6.6 Stream Switch Routing Registers, AR = 1007h:1000h (Ch. 7:0)

Note: To ensure compatibility with possible future versions of this device, write "0" to all "Reserved" bits in the routing registers. All "Reserved" routing registers read-back "0".

DR_0	Definition
[4:0]	Input Data Stream [4:0]
[7:5]	Reserved (write zero)

Input Data Stream [4:0] (Read/Write)

00h → CT_D_[0] (Default)
01h → CT_D_[1]
02h → CT_D_[2]
• •
• •
1eh → CT_D_[30]
1fh → CT_D_[31]

DR_1	Definition
[4:0]	Output Data Stream [4:0]
[6:5]	Reserved (write zero)
7	Output Enable

Output Data Stream [4:0] (Read/Write)

00h → CT_D_[0] (Default)
01h → CT_D_[1]
02h → CT_D_[2]
• •
• •
1eh → CT_D_[30]
1fh → CT_D_[31]

Output Enable (Read/Write)

0 → Output Disabled (Default)
1 → Output Enabled

DR_2	Definition
[1:0]	Partition [1:0]
[7:2]	Reserved (write zero)

Partition [1:0] (Read/Write)

Selects which time-slots are used when rate conversion is taking place. See the following table for a description of the partition function.

6.7 Stream Switch Connection Mapping

Input Data Stream Rate	Output Data Stream Rate	Partition	Time-Slot Connection
2 Mbps	2 Mbps	0	0 to 1, 1 to 2, 2 to 3, … , 31 to 0
	4 Mbps	0	0 to 2, 1 to 4, 2 to 6, … , 31 to 0
		1	0 to 3, 1 to 5, 2 to 7, … , 31 to 1
	8 Mbps	0	0 to 4, 1 to 8, 2 to 12, … , 31 to 0
		1	0 to 5, 1 to 9, 2 to 13, … , 31 to 1
		2	0 to 6, 1 to 10, 2 to 14, … , 31 to 2
		3	0 to 7, 1 to 11, 2 to 15, … , 31 to 3
4 Mbps	2 Mbps	0	0 to 1, 2 to 2, 4 to 3, … , 62 to 0
		1	1 to 1, 3 to 2, 5 to 3, … , 63 to 0
	4 Mbps	0	0 to 1, 1 to 2, 2 to 3, … , 63 to 0
	8 Mbps	0	0 to 2, 1 to 4, 2 to 6, … , 63 to 0
		1	0 to 3, 1 to 5, 2 to 7, … , 63 to 1
8 Mbps	2 Mbps	0	0 to 1, 4 to 2, 8 to 3, … , 124 to 0
		1	1 to 1, 5 to 2, 9 to 3, … , 125 to 0
		2	2 to 1, 6 to 2, 10 to 3, … , 126 to 0
		3	3 to 1, 7 to 2, 11 to 3, … , 127 to 0
	4 Mbps	0	0 to 1, 2 to 2, 4 to 3, … , 126 to 0
		1	1 to 1, 3 to 2, 5 to 3, … , 127 to 0
	8 Mbps	0	0 to 1, 1 to 2, 2 to 3, … , 127 to 0

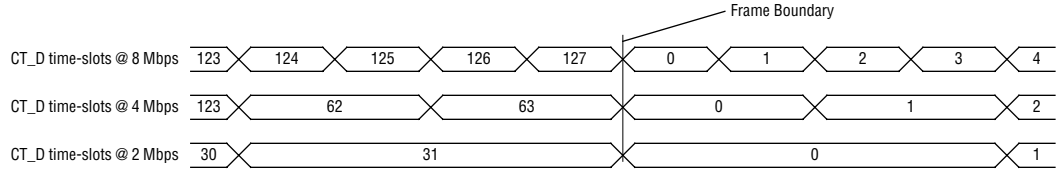


Figure 5. CT Bus Data Stream Switching

The Stream Switch provides a data stream-to-data stream connection capability. Switching between any of the 32 CT Bus data streams operating at 2, 4, or 8 Mbps is supported. Eight stream switch channels are provided. Individual time-slots are not tri-state controlled. Buffering is done on single time-slots rather than entire frames. This trade-off complicates the connection matrix, but without this compromise it would not be practical to implement the Stream Switch.

Depending upon the data stream rates, the stream switch provides a minimum of 256 and a maximum of 1024 uni-directional time-slot connections. Stream switches in other ML53612 devices in a system may be used simultaneously to increase switching capability. The output of the stream switch is multiplexed with the output of the transmit switch, with the transmit switch having priority.

The main application of the Stream Switch is to provide an inter-rate exchange highway allowing legacy Bus devices operating at different rates to exchange data.

A typical configuration of the Stream Switch using 2 switch channels and 3 streams to provide 32 full duplex connections between SCbus (operating at 4 MHz) and MVIP is outlined below.

Example:

Stream switch channel 0 is configured with CT_D_0 as the input data stream and the even time-slots (partition = 0) of CT_D_8 as the output data stream.

Stream switch channel 1 is configured with the odd time-slots (partition = 1) of CT_D_8 as the input data stream and CT_D_1 as the output data stream.

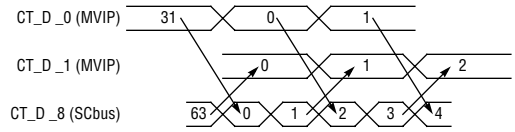


Figure 6. Data Stream Switching Example

6.8 Transmit Switch Routing Registers, AR = 203fh:2000h (Ch. 63:0)

Note: To ensure compatibility with subsequent versions of this device, write "0" to all "Reserved" bits in the routing registers. All "Reserved" routing registers read-back "0".

DR_0	Definition
[6:0]	Output Time-slot
7	Reserved (write zero)

Output Time-slot [6:0] (Read/Write)

Selects the CT_D time-slot for transmit channel routing.

00h → Time-slot 0 (Default)
01h → Time-slot 1
02h → Time-slot 2
• •
• •
7eh → Time-slot 126
7fh → Time-slot 127

Note: Internally all time-slots run at 8 Mbps. To transmit on CT_D data streams running at a slower rate, use the following conversion:

If CT_D data stream is operating at 4 Mbps, transmit switch output time-slot = CT_D time-slot X 2.

If CT_D data stream is operating at 2 Mbps, transmit switch output time-slot = CT_D time-slot X 4.

DR_1	Definition
[4:0]	Output Data Stream
[6:5]	Reserved (write zero)
7	Output Enable

Output Data Stream [4:0] (Read/Write)

Selects the CT_D Data stream for transmit channel routing.

00h → CT_D_[0] (Default)
01h → CT_D_[1]
02h → CT_D_[2]
• •
• •
1eh → CT_D_[30]
1fh → CT_D_[31]

Output Enable (Read/Write)

Controls the Output Enable for the selected CT Bus data stream and time-slot.

0 → Output Disabled (Default)
1 → Output Enabled

DR_2	Definition
0	Delay
1	CT Bus Connect
2	Source
[7:3]	Reserved (write zero)

Delay (Read/Write)

Selects the switching delay mode. When set to Constant, data is switched on frame boundaries resulting in a constant 1 frame delay and allowing "bundling". When set to Minimum, data is switched on 2 Mbps time-slot boundaries reducing the delay through the switch for certain combinations of input to output time-slots.

0 → Constant (Default)

1 → Minimum

Note: Do not use Minimum delay mode on channels using parallel data source.

CT Bus Connect Enable (Read/Write)

Enables the switch to be used for CT Bus to CT Bus connection without externally connecting L_SO to L_SI. When enabled, the L_SI input is replaced by the corresponding L_SO output. CT Bus connect allows inter-operability switching to be provided by any unused transmit and receive switch pair.

0 → CT Bus Connect Disabled (Default)

1 → CT Bus Connect Enabled

Note:
1. When CT Bus Connect is enabled, the L_SO to L_SI connection does not pass through the conversion circuitry. See Figure 2.
2. The Receive Switch Output Enable register does not have to be set to make this connection.

Source (Read/Write)

Selects the transmit channel data source. When set to 0, Serial TDM data from L_SI or L_SO (see CT Bus Connect Enable) is selected. When set to 1, the corresponding parallel access register is selected as the source of the transmit channel data.

0 → Serial TDM data (Default)

1 → Parallel microprocessor data

Note: The Serial TDM data and the parallel access register share common registers within the transmit switch. Therefore it is necessary to write to the parallel access register after the source is changed to parallel microprocessor data.

6.9 Receive Switch Routing Registers, AR = 303fh:3000h (Ch. 63:0)

Note: To ensure compatibility with subsequent versions of this device, write "0" to all "Reserved" bits in the routing registers. All "Reserved" routing registers read-back "0".

DR_0	Definition
[6:0]	Input Time-slot
7	Reserved (write zero)

Input Time-slot [6:0] (Read/Write)

Selects the CT_D time-slot for receive channel routing.

00h → Time-slot 0 (Default)
01h → Time-slot 1
02h → Time-slot 2
• •
• •
7eh → Time-slot 126
7fh → Time-slot 127

Note: Internally all time-slots run at 8 Mbps. To receive from CT_D streams running at a slower rate, use the following conversion:

If CT_D stream is operating at 4 Mbps, receive switch input time-slot register = CT_D time-slot X 2 + 1.

If CT_D stream is operating at 2 Mbps, receive switch input time-slot register = CT_D time-slot X 4 + 3.

DR_1	Definition
[4:0]	Input Data Stream
[6:5]	Reserved (write zero)
7	Output Enable

Input Data Stream [4:0] (Read/Write)

Selects the CT_D data stream for receive channel routing.

00h → CT_D_[0] (Default)
01h → CT_D_[1]
02h → CT_D_[2]
• •
• •
1eh → CT_D_[30]
1fh → CT_D_[31]

Output Enable (Read/Write)

Controls the Output Enable for the channel's local stream.

0 → Output Disabled (Default)
1 → Output Enabled

DR_2	Definition
0	Delay
1	Local Connect
2	Source
[7:3]	Reserved (write zero)

Delay (Read/Write)

Selects the switching delay mode. When set to Constant, data is switched on frame boundaries resulting in a constant 1 frame delay and allowing "bundling". When set to Minimum, data is switched on 2 Mbps time-slot boundaries reducing the delay through the switch for certain combinations of input to output time-slots.

0 → Constant (Default)

1 → Minimum

Note: Do not use Minimum delay mode on channels using parallel data source.

Local Connect Enable (Read/Write)

Enables the receive switch to be used for local connection. When enabled, a transmit channel is connected to a receive channel without using the CT Bus.

0 → Local Connect Disabled (Default)

1 → Local Connect Enabled

Note: When Local Connect is Enabled, the Receive Switch routing registers DR_0 is redefined as the 6 bits of the transmit channel number instead of the CT_D time-slot, as shown below:

DR_0_[5:0] → Transmit channel bits [5:0]

Source (Read/Write)

Selects the receive channel data source. When set to 0, Serial TDM data from the CT Bus data stream or transmit channel (see Local Connect Enable) is selected. When set to 1, the channels parallel access register is selected as the source of the receive channel data.

0 → Serial TDM data (Default)

1 → Parallel microprocessor data

Note: The Serial TDM data and the parallel access register share common registers within the receive switch. Therefore it is necessary to write to the parallel access register after the source is changed to parallel microprocessor data.

6.10 Indirect Transmit Switch Parallel Access Registers, AR = 403fh:4000h (Ch. 63:0)

DR_0	Definition
[7:0]	TDM Data [1:8]

TDM Data [1:8] (Read/Write)

Writing to this register provides the transmit data when the transmit switch channel is configured to use parallel microprocessor data as its source (to CT_D). This register and the serial input buffer share common hardware, therefore this register must be written after the transmit switch channel source is changed from serial TDM data to parallel microprocessor data.

The transmit switch channel output buffer data obtained by reading the TDM data register. When the transmit switch channel is configured to use serial TDM data as its source, the data from the local SI channel can be monitored. When the transmit switch channel is configured to use parallel microprocessor data as its source, the data written into this register can be monitored.

Note: When converted from parallel to serial, TDM Data Bit 1 is transmitted first.

6.11 Indirect Receive Switch Parallel Access Registers, AR = 503fh:5000h (Ch. 63:0)

DR_0	Definition
[7:0]	TDM Data [1:8]

TDM Data [1:8] (Read/Write)

Writing to this register provides the receive data when the receive switch channel is configured to use parallel microprocessor data as its source (to L_SO). This register and the serial input buffer share common hardware, so this register must be written after the receive switch channel source is changed from serial TDM data to parallel microprocessor data.

The receive switch channel output buffer data is obtained by reading the TDM Data register. When the receive switch channel is configured to use serial TDM data as its source, the data from the CT_D stream and time-slot selected in the receive switch routing registers can be monitored. When the receive switch channel is configured to use parallel microprocessor data as its source, the data written into this register can be monitored.

Note: When converted from parallel to serial, TDM Data Bit 1 is transmitted first.

6.12 Transmit Switch Conversion Registers, AR = 603Fh:6000h (Ch. 63:0) Receive Switch Conversion Registers, AR = 703Fh:7000h (Ch. 63:0)

To ensure compatibility with possible future versions of this device all "Reserved" Conversion registers should be written "0". All "Reserved" Conversion registers read-back "0".

DR_0	Definition
[5:0]	Gain
[7:6]	Reserved

Gain [5:0] (Read/Write)

Selects the gain of a channel.

1Fh → +31 dB
1Eh → +30 dB
1Dh → +29 dB
.
.
03h → +3 dB
02h → +2 dB
01h → +1 dB
00h → No gain (Default)
20h → Idle (μ = 7f, A = d5, Linear = 8000)
21h → -1 dB
22h → -2 dB
23h → -3 dB
.
.
3Dh → -29 dB
3Eh → -30 dB
3Fh → -31 dB

Note: Gain settings do not apply when Mode is By-pass.

Even # Channels	
DR_1	Definition
[3:0]	Mode
[7:4]	Reserved

Odd # Channels	
DR_1	Definition
[2:0]	Mode
[7:3]	Reserved

Mode [3:0] (Read/Write)		
00xx	→	By-pass (Default)
0100	→	A to A
0101	→	μ to μ
0110	→	A to μ
0111	→	μ to A
1000	→	A to Linear
1001	→	μ to Linear
1010	→	Linear to μ
1011	→	Linear to A
11xx	→	Linear to Linear

Mode [2:0] (Read/Write)		
0xx	→	By-pass (Default)
100	→	A to A
101	→	μ to μ
110	→	A to μ
111	→	μ to A

Note: Linear Conversions require two consecutive channels.
When an Even numbered Channel is configured for Linear Conversion, the configuration registers of the next higher Odd numbered Channel are "don't care".
When A/μ to Linear conversion is selected, the A/μ data is taken from the even numbered channel.
When Linear to A/μ conversion is selected, the A/μ data is presented on the even numbered channel.
Linear data (16 bit - sign/magnitude) is formatted MSB in the even channel, LSB in the odd channel.

7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Parameter	Symbol	Test Conditions	Min	Max	Unit
Storage Temperature	T_S		-65	150	°C
Power Supply Voltage	V_{PS}		-0.3	4.6	V
Input Voltage	V_I		-0.3	6	V

7.2 Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Max	Unit
Ambient Temperature	T_A		-40	85	°C
Supply Voltage	V_{DD}		3.0	3.6	V

7.3 DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Core Supply Current	I_{DDC}	V_{DDC} = 3.6V		125	mA
I/O Supply Current	I_{DDO}	V_{DDO} = 3.6V		140	mA
Analog PLL Supply Current	I_{DDA}	V_{DDA} = 3.6V		10	mA
Input High Voltage	V_{IH}		2.0	5.5	V
Input Low Voltage	V_{IL}		-0.5	0.8	V
Schmitt Input High Voltage	V_{t+}		2.05	5.5	V
Schmitt Input Low Voltage	V_{t-}		-0.5	0.7	V
Schmitt Input Hysteresis Voltage	V_{HYS}		±0.4		V
Output High Voltage - PCI	V_{OH-PCI}	I_{OH} = -2 mA	2.4		V
Output Low Voltage - PCI	V_{OL-PCI}	I_{OL} = 6 mA		0.55	V
Output High Voltage – 24mA	$V_{OH-24mA}$	I_{OH} = -24 mA	2.4		V
Output Low Voltage – 24mA	$V_{OL-24mA}$	I_{OL} = 24 mA		0.4	V
Output High Voltage – 8mA	V_{OH-8mA}	I_{OH} = -8 mA	2.4		V
Output Low Voltage – 8mA	V_{OL-8mA}	I_{OL} = 8 mA		0.4	V
Output High Voltage – 6mA	V_{OH-6mA}	I_{OH} = -6 mA	2.4		V
Output Low Voltage – 6mA	V_{OL-6mA}	I_{OL} = 6 mA		0.4	V
50 k Pull-up Current	I_P	V_{PAD} = 0 V	-15	-170	µA
I/O Leakage Current	$I_{LI/O}$	$V_{I/O}$ = V_{DD} or V_{SS}		±10	µA

NOTES:

1. PCI Drivers meet the AC Specifications for the PCI 5V signaling environment.
2. Pin Capacitance: Input pins = 6 pF, Output pins = 9 pF, Bi-directional pins = 10 pF.

7.4 AC Electrical Characteristics

Note: Signals ending in "_N" are active low.

Microprocessor Interface Timing - Intel Bus Mode, Non-multiplexed Address [1] [2] [3]

Parameter	Symbol	Min	Typ	Max	Unit
CS_N setup to WR_N ↑	t1	40			ns
WR_N pulse width	t2	40			ns
A_[9:0] setup to WR_N ↓ (C_96=1)	t3	5			ns
A_[2:0] setup to WR_N ↑(C_96=0)	t4	40			ns
A_[9:0] hold from WR_N ↑	t5	5			ns
D_[7:0] setup to WR_N ↑	t6	40			ns
D_[7:0] hold from WR_N ↑	t7	5			ns
D_[7:0] float to valid delay from CS_N RD_N, and A_[9:0]	t8	0		50	ns
D_[7:0] valid to float delay from CS_N or RD_N	t9	0		10	ns

1. Timing measured with 100 pF load on D_[7:0].
2. Write cycle may be controlled by CS_N or WR_N.
3. ALE=1.

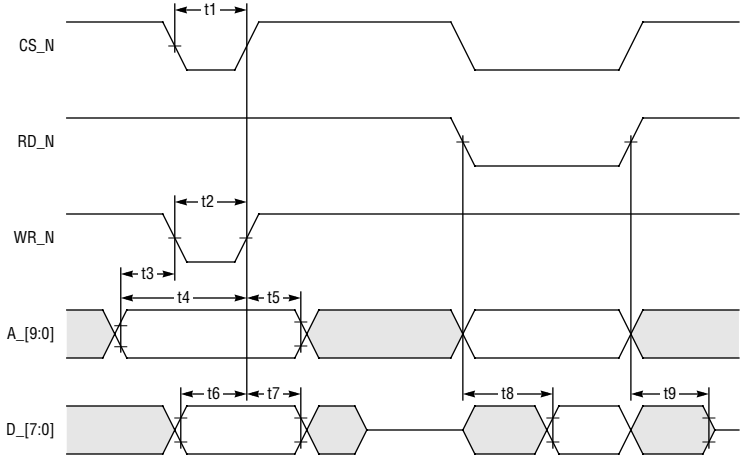


Figure 7. Microprocessor Interface Timing - Intel Bus Mode, Non-multiplexed Address

Microprocessor Interface Timing - Motorola Bus Mode, Non-multiplexed Address [1] [2] [3]

Parameter	Symbol	Min	Typ	Max	Unit
CS_N setup to STRB_N ↑	t1	40			ns
STRB_N pulse width	t2	40			ns
R/W_N setup to STRB_N ↓	t3	5			ns
R/W_N hold from STRB_N ↑	t4	5			ns
A_[9:0] setup to STRB_N ↓ (C_96=1)	t5	5			ns
A_[2:0] setup to STRB_N ↑ (C_96=0)	t6	40			ns
A_[9:0] hold from STRB_N ↑	t7	5			ns
D_[7:0] setup to STRB_N ↑	t8	40			ns
D_[7:0] hold from STRB_N ↑	t9	5			ns
D_[7:0] float to valid delay from CS_N, STRB_N, and A_[9:0]	t10	0		50	ns
D_[7:0] valid to float delay from CS_N or STRB_N	t11	0		10	ns

1. Timing measured with 100 pF load on D_[7:0].
2. Write cycle may be controlled by CS_N or STRB_N.
3. AS=1.

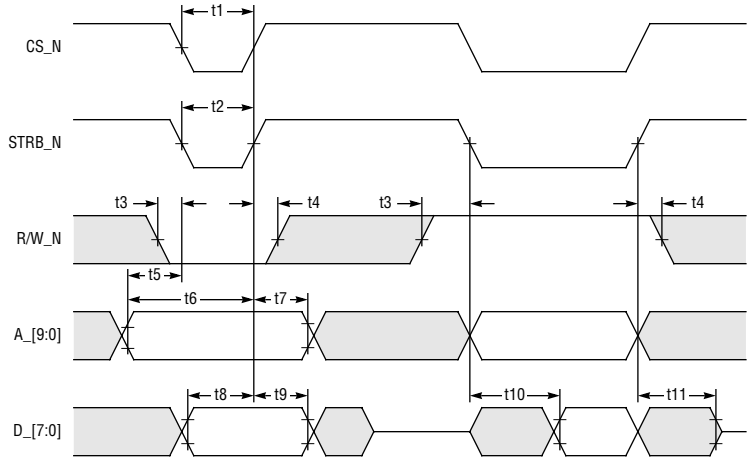


Figure 8. Microprocessor Interface Timing - Motorola Bus Mode, Non-multiplexed Address

Microprocessor Interface Timing - Multiplexed Address

Parameter	Symbol	Min	Typ	Max	Unit
ALE (AS) pulse width	t1	20			ns
A_[9:0] setup to ALE (AS) ↓	t2	5			ns
A_[9:0] hold from ALE (AS) ↓	t3	5			ns

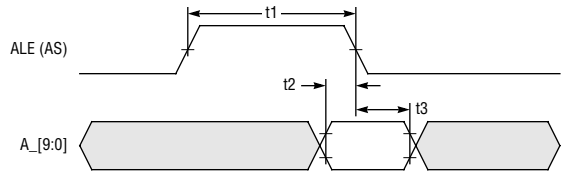


Figure 9. Microprocessor Interface Timing - Multiplexed Address

Reset Timing

Parameter	Symbol	Min	Typ	Max	Unit
RESET pulse width	t1	50			ns

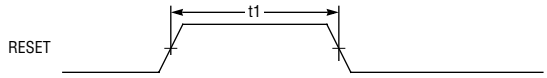


Figure 10. Reset Timing

Local Clock and Frame Synchronization Timing

Parameter	Symbol	Min	Typ	Max	Unit
Local Clock and Frame Synchronization Timing [1] [2]					
L_CLK Period (2.048 MHz)	t1a		488		ns
L_CLK Period (4.096 MHz)	t1b		244		ns
L_CLK Period (8.192 MHz)	t1c		122		ns
L_CLK Period (16.384 MHz)	t1d		61		ns
L_FS delay from L_CLK ↑ (Early Position)	t2	-10		+10	ns
L_FS delay from L_CLK ↑ (Straddle Position)	t3	-10		+10	ns
L_FS delay from L_CLK ↑ (Late Position)	t4	-10		+10	ns
Local Clock to CT Bus clock skew [3]					
With C_11 (Advance Slave DPLL Timing) set to 0 (default)	t5			+22.5 / -0	ns
With C_11 (Advance Slave DPLL Timing) set to 1	t5			+15 / -7.5	ns

1. Timing measured with 100 pF load on all Local bus outputs.
2. L_CLK and L_FS shown with positive polarity, timing is equivalent when signals are inverted.
3. When L_CLK is more stable, there is no reduction in the amplitude of the skew, but a reduction in the number of occurrences. The farther away from the center frequency, the more frequently the skew occurs. The skew amplitude will jump in steps, but the range will remain the same. Test conditions were 65.536 MHz (C_[7:4]=0) and 2.048 MHz (C_[7:4]=6).

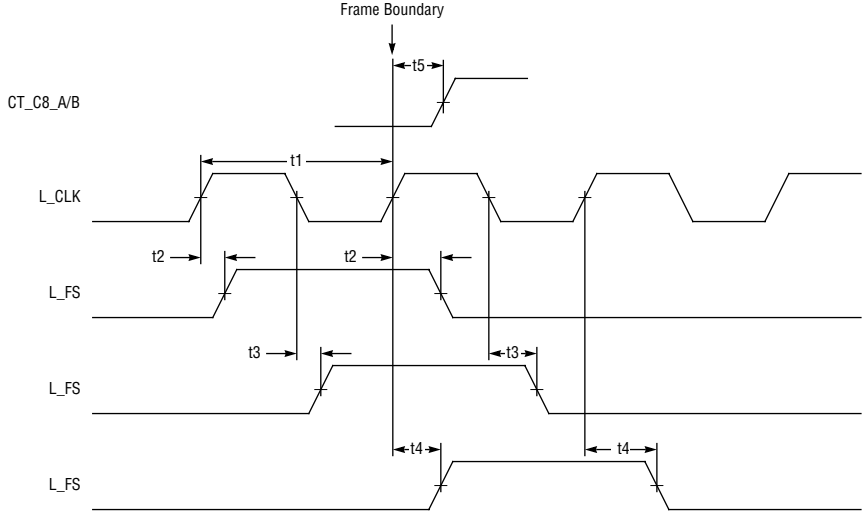


Figure 11. Local Clock and Frame Synchronization Timing

Local Serial Stream Timing [1] [2]

Parameter	Symbol	Min	Typ	Max	Unit
L_SO float to valid delay from Bit Cell Boundary	t1	-10		10	ns
L_SO valid to valid delay from Bit Cell Boundary	t2	-10		10	ns
L_SO valid to float delay from Bit Cell Boundary	t3	-10		10	ns
2.048 Mbps Sample Point from Bit Cell Boundary	t4a		335.5		ns
4.096 Mbps Sample Point from Bit Cell Boundary	t4b		213.5		ns
8.192 Mbps Sample Point from Bit Cell Boundary	t4c		91.5		ns
L_SI setup to Sample Point	t5	10			ns
L_SI hold from Sample Point	t6	10			ns

1. The Bit Cell Boundary is defined by relative edge of L_CLK.
2. Timing measured with 100 pF load on all local bus outputs.

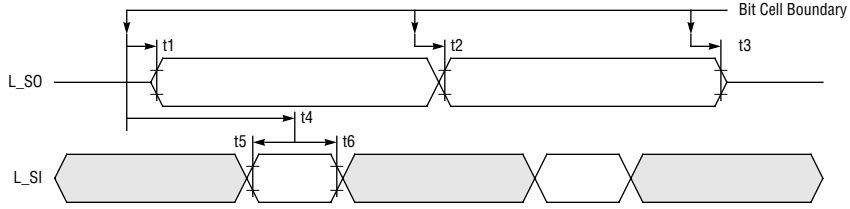
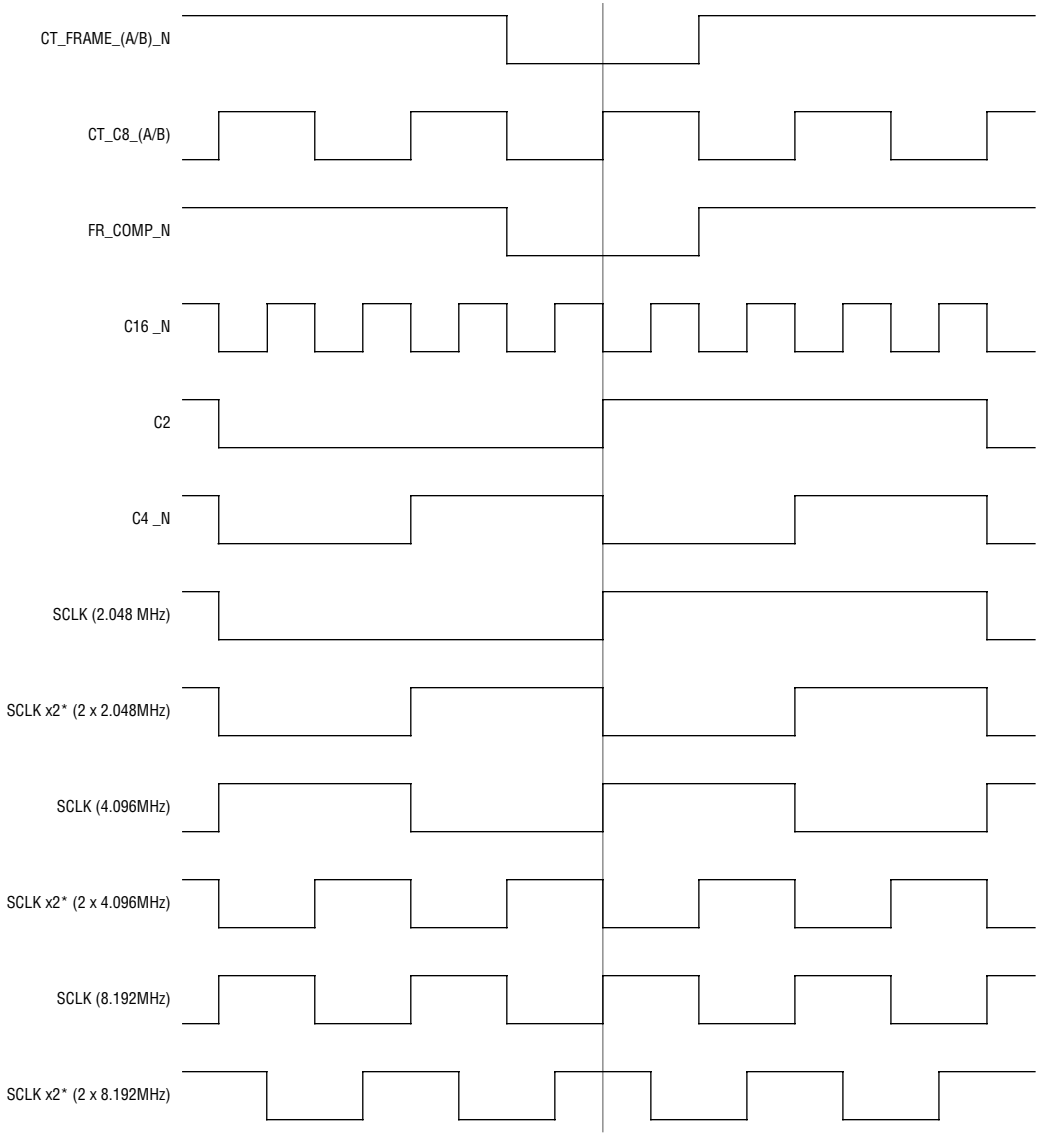


Figure 12. Local Serial Stream Timing

H.100/H.110 Clock Alignment

(Extract from H.100/H.110 Specifications, Rev. 1.0)



Note: C16_N, C2, and C4_N not defined in H.110.

Figure 13. H.100/H.110 Clock Alignment

H.100/H.110 Frame Structure

(Extract from H.100/H.110 Specifications, Rev. 1.0)

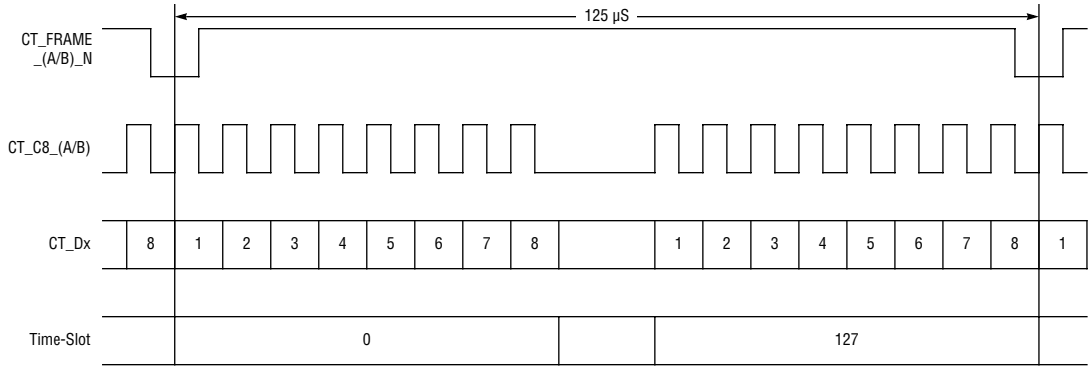


Figure 14. H.100/H.110 Frame Structure

H.100/H.110 Detailed Data Bus Timing

(Extract from H.100/H.110 Specifications, Rev. 1.0)

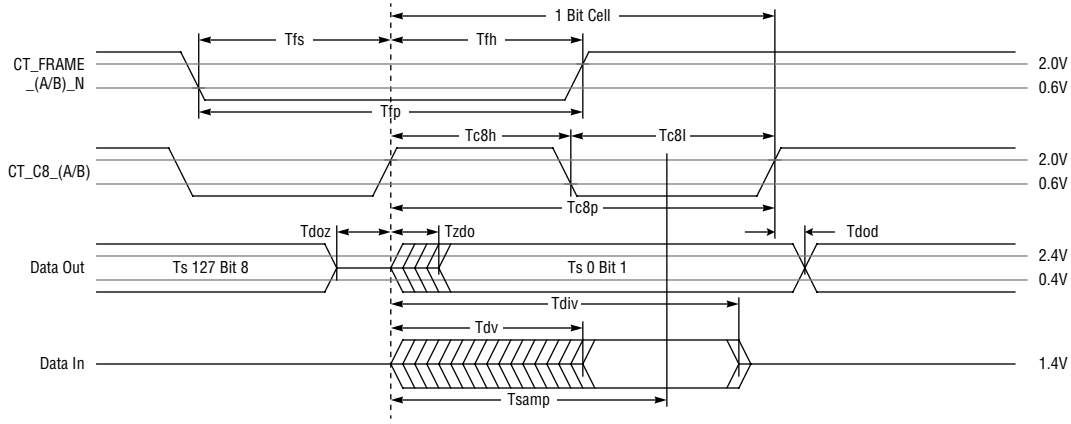


Figure 15. H.100/H.110 Detailed Data Bus Timing

7.5 H.100/H.110 Bus Timing Specification

(Extract from H.100/H.110 Specifications, Rev. 1.0)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Clock edge rate (All Clocks)	H.100		0.25		2	V/ns	[1]
CT_C8_(A/B) and CT_FRAME_(A/B)_N edge rate	H.110		0.25		2	V/ns	[1]
CT_NETREF edge rate	H.110				0.3	V/ns	[2]
Clock CT_C8_(A/B) Period		Tc8p	122.066-Φ		122.074+Φ	ns	[3]
Clock CT_C8_(A/B) High Time	H.100	Tc8h	49-Φ		73+Φ	ns	[4]
	H.110		63-Φ		69+Φ	ns	[4] [5]
Clock CT_C8_(A/B) Low Time	H.100	Tc8l	49-Φ		73+Φ	ns	[4]
	H.110		63-Φ		69+Φ	ns	[4] [5]
Data Sample Point		Tsamp		90		ns	[6]
Data Output to HiZ Time	H.100	Tdoz	-20		0	ns	[7] [8] [9]
	H.110		-10		0	ns	[8] [9] [10]
Data HiZ to Output Time	H.100	Tzdo	0		22	ns	[7] [8] [9]
	H.110		0		11	ns	[8] [9] [10]
Data Output Delay Time	H.100	Tdod	0		22	ns	[7] [8]
	H.110		0		11	ns	[8] [10]
Data Valid Time	H.100	Tdv	0		69	ns	[7] [11] [12]
	H.110		0		83	ns	[11] [13] [14]
Data Invalid Time	H.100	Tdiv	102		112	ns	
	H.110		102		112	ns	[15] [16]
CT_FRAME_(A/B)_N Width		Tfp	90	122	180	ns	
CT_FRAME_(A/B)_N Setup Time		Tfs	45		90	ns	
CT_FRAME_(A/B)_N Hold Time		Tfh	45		90	ns	
Phase Correction		Φ	0		10	ns	[17]

1. The rise and fall times are determined by the edge rate in V/nS. A maximum edge rate is the fastest rate at which a clock transitions.
2. 10% - 90%. Test Load = 150 pF.
3. Tc8p Min and Max are under free-run conditions assuming ±32 ppm clock accuracy.
4. Non-cumulative, Tc8p requirements still need to be met.
5. Duty Cycle measured at transmitter under no load conditions.
6. For reference only
7. Test Load - 200 pF
8. Measured at the transmitter.
9. Tdoz and Tzdo apply at every time-slot boundary.
10. Test Load - 12 pF
11. Measured at the receiver.
12. Reference only: Tdv = Max. clock cable delay + Max. data cable delay + Max. data HiZ to output time = 12nS + 35nS + 22 nS = 69nS. Max. clock cable delay and max. data cable delay are worst case numbers based on electrical simulation.
13. Reference only: Tdv = Max. clock backplane delay + Max. data backplane delay + Max. data HiZ to output time = 26nS + 46nS + 11nS = 83nS. Max. clock delay and max. data delay are worst case numbers based on electrical simulation.
14. Based on worst case electrical simulation.
15. This range accounts for Φ (Phase Correction).
16. Tcell = Max. clock backplane delay + Max. data backplane delay + Max. Tzdo + (Min. Tdiv - Max. Tdv) + Max Tdoz + F = 26nS + 46nS + 11nS + (102nS - 83nS) + 10nS + 10nS = 122nS. Max. clock delay and max. data delay are worst case numbers based on electrical simulation.

17. Φ (Phase Correction) results from PLL timing corrections.

H.100. Measuring conditions:	Data lines	Vth (threshold voltage) = 1.4V
		Vhi (test high voltage) = 2.4V
		Vlo (test low voltage) = 0.4V
		Input signal edge rate = 1 V/nS
	Clock and Frame lines	Vt+ (test high voltage) = 2.0V
		Vt- (test low) = 0.6V
		Input signal edge rate = 1 V/nS
H.110. Measuring conditions:	Data lines	Vhi (test high voltage) = 2.0V
		Vlo (test low voltage) = 0.8V
		Input signal edge rate = 1 V/nS
	Clock and Frame lines	Vt+ (test high voltage) = 2.0V
		Vt- (test low voltage) = 0.6V
		Input signal edge rate = 1 V/nS

7.6 Clock Skew Requirements

(Extract from H.100/H.110 Specifications, Rev. 1.0)

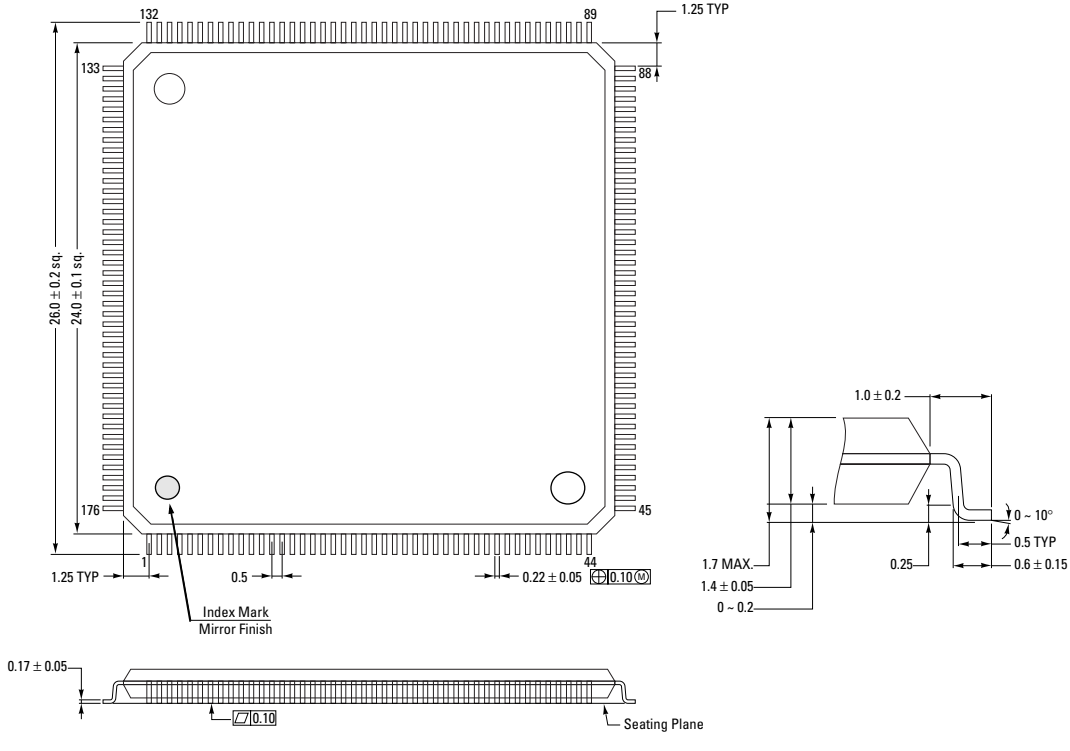
Parameter	Symbol	Min	Typ	Max	Unit	Notes
(H.100) Max Skew between CT_C8 "A" and "B"	Tskc8			±10 ±Φ	ns	[1] [2] [3] [4]
(H.110) Max Skew between CT_C8 "A" and "B"	Tskc8			±10 ±Φ	ns	[2] [3] [4] [5]
(H.100) Max Skew between CT_C8_A and any compatibility clock	Tskcomp			±5	ns	[1]
(H.110) Max Skew between CT_C8_A and any compatibility clock	Tskcomp			±5	ns	[5]

1. Test Load – 200 pF.
2. Assumes "A" and "B" masters in adjacent slots.
3. When static skew is 10nS and, in the same clock cycle, each clock performs a 10nS phase correction in opposite directions, a maximum skew of 30nS will occur during that clock cycle.
4. Meeting the skew requirements in Table 2 and the requirements of Section 2.3 (in the H.100/H.110 Specifications, Rev. 1.0) could require the PLL's generating CT_C8 to have different time constants when acting as primary and secondary clock masters.
5. Test Load - "A" load = "B" load.

Figure 16. Clock Skew Requirements

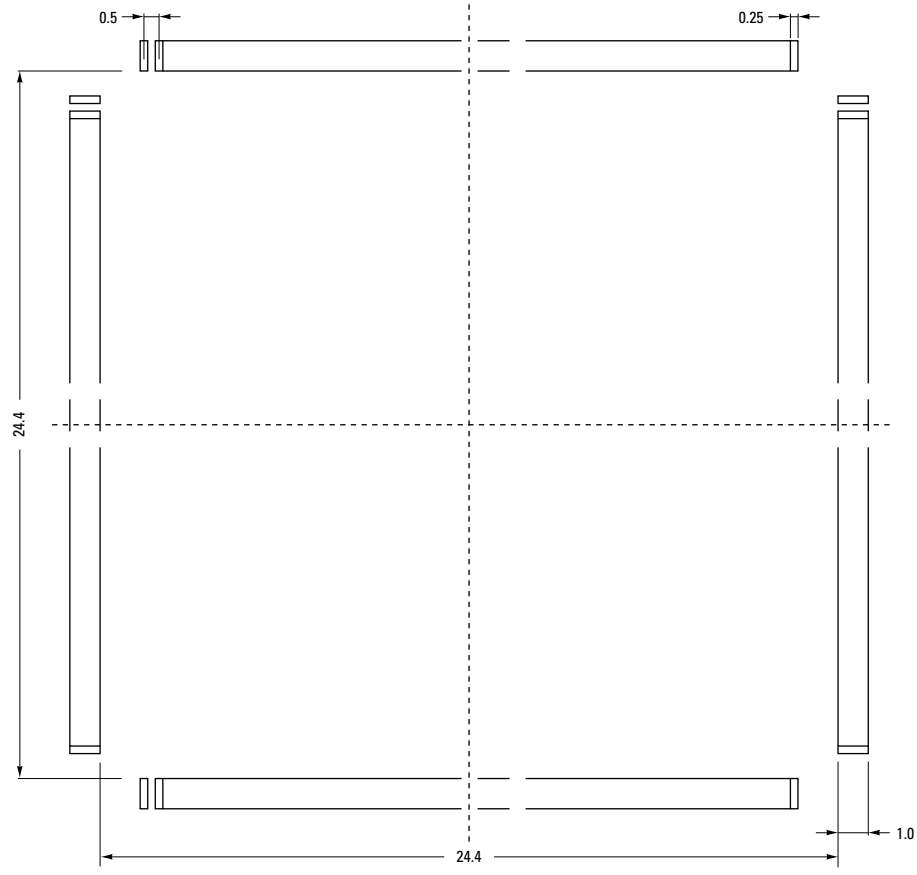
8.0 ML53612 PACKAGE SPECIFICATIONS

8.1 LQFP176 Package Outlines and Dimensions



All measurements are in millimeters or degrees

8.2 LQFP176 Mounting Pad Reference Measurements



LQFP176-P-2424-0.50-BK

All measurements are in millimeters

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