ML670100

OKI's High-Performance CMOS 32-Bit Single Chip Microcontroller

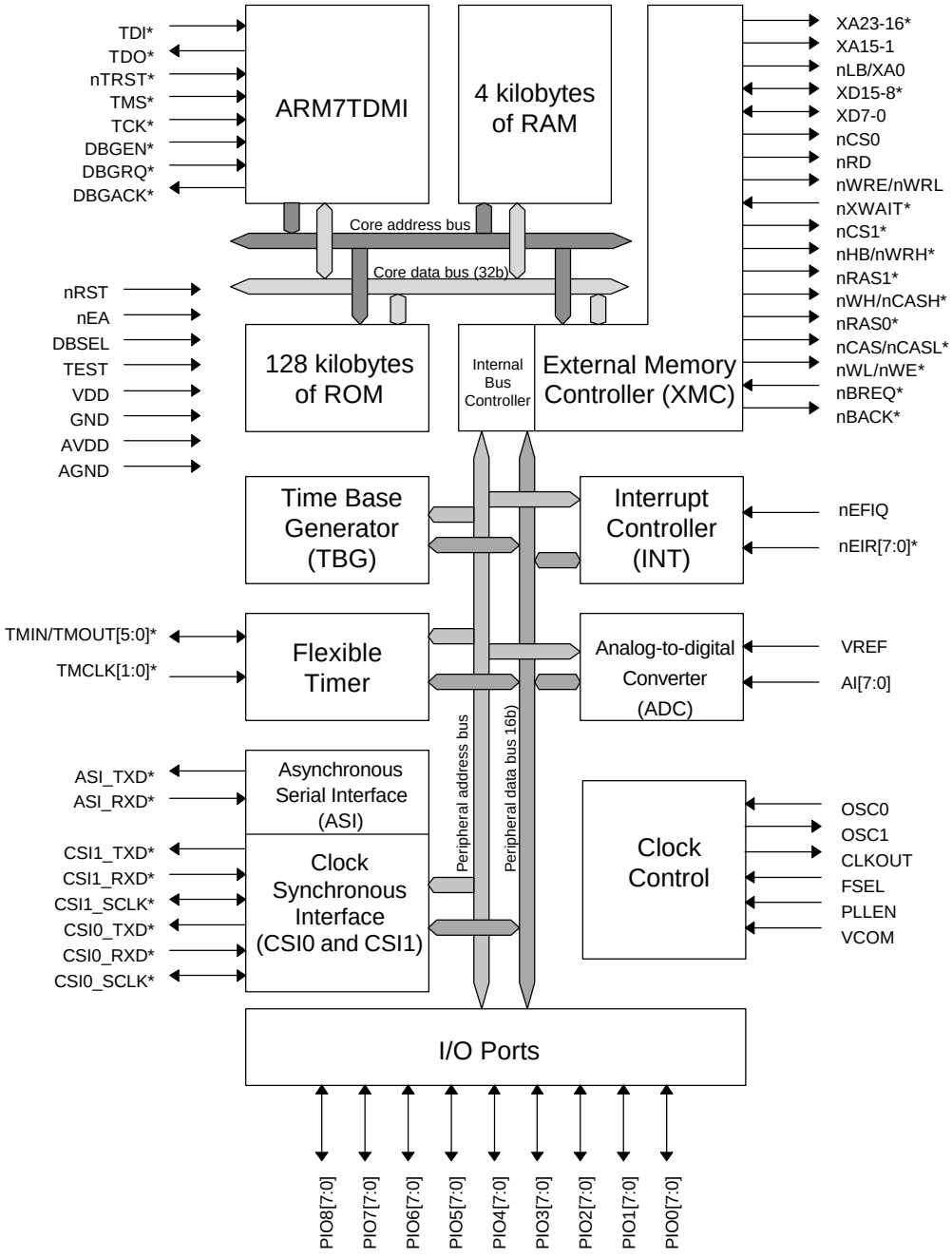
GENERAL DESCRIPTION

The ML670100 is a high-performance 32-bit microcontroller combining a RISC based, 32-bit CPU core - the ARM7TDMI™ - with memory and such peripheral circuits as timers, serial ports, and analog-to-digital converter. This combination of 32-bit data processing, built-in memory, and on-chip peripherals make it ideal for controlling equipment requiring both high speed and high functionality. An external memory controller supports direct connection to memory and peripheral devices for adding even more functionality.

FEATURES

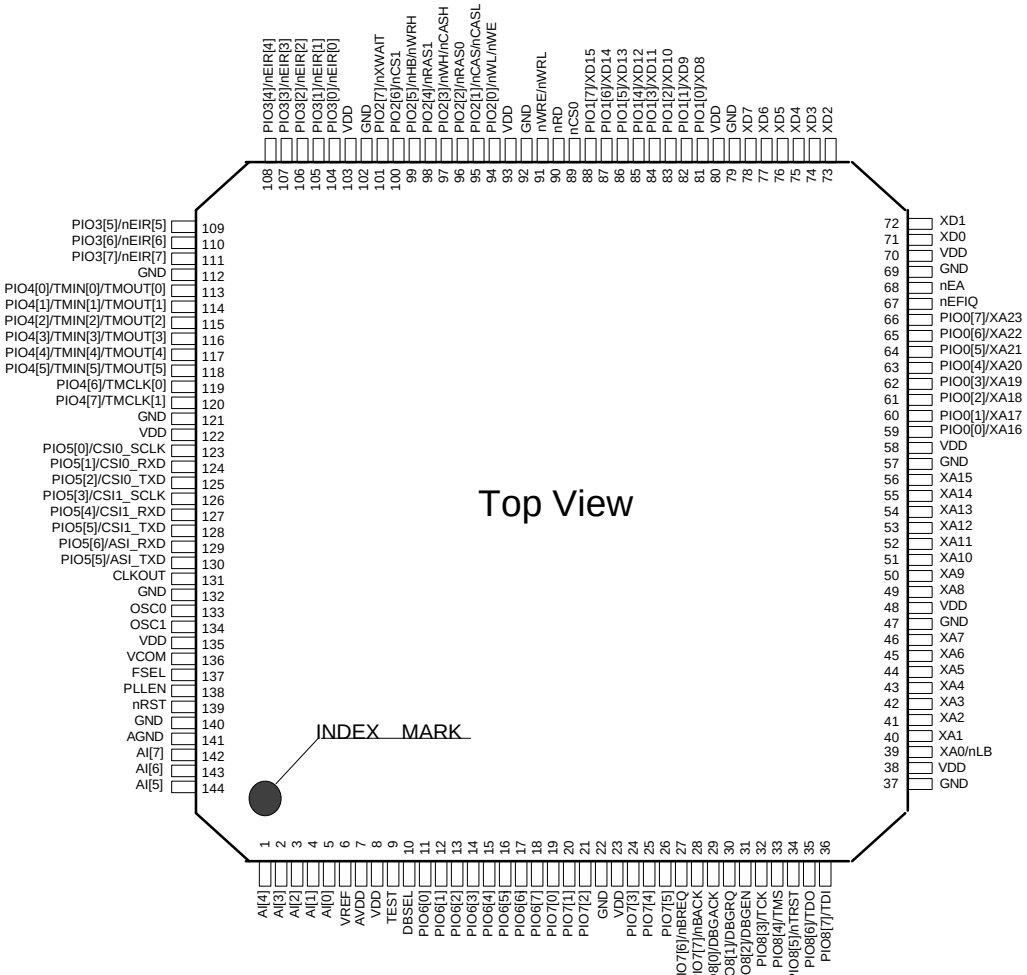
Operating Voltage	2.7 to 3.6V
Operating Frequency	25MHz maximum(3.0 to 3.6V)
On-chip memory	-ROM: 128 kilobytes -RAM: 4 kilobytes
I/O Function	I/O ports: 8 bits x 9, I/O directions are specified at the bit level
Timer	-Flexible timer (16-bit multi-function timer with six channels) Choice of operating modes: auto-reload timer, compare output, PWM and capture -Time base counter with WDT function
Serial Port	-One asynchronous serial port (UART) with baud rate generator -Two clock synchronous serial port
A-to-D Converter	-8-bit resolution A-to-D converter with eight analog input ports
Interrupt Controller	-Support for 28 interrupt sources: 9 external and 19 internal -Choice of eight priority levels for each source
External Memory Controller	-Direct connection to ROM, SRAM, DRAM and peripheral devices -Support for four banks: two for ROM, SRAM and I/O devices plus two for DRAM -User-configurable bus width (8/16 bits) and wait control and other parameters for accessing memory and external devices
Clock Generator	-Built-in crystal oscillation circuit and PLL -Choice of divider ratio (1/1, 1/2, 1/4) for adjusting operating clock frequency to match the load of processing
Package	144-pin LQFP (LQFP144-P-2020-0.50-K)

BLOCK DIAGRAM



Asterisks indicate signals that aresecondary functions of I/O ports.
Brackets indicate bit ranges.

PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

Type	Signal Name	I/O Direction	Description
Address bus	XA23 - XA16	Output	These are bits 23-16 of the external address bus. They represent secondary functions for I/O port PIO0[7:0].
	XA15 - XA0	Output	These are bits 15 - 0 of the external address bus.
Data bus	XD15 - XD8	Bidirectional	These are bits 15-8 of the external data bus. They represent secondary functions for I/O port PIO1[7:0].
	XD7- -XD0	Bidirectional	These are bits 7-0 of the external data bus.
Bus control signals	nCS0	Output	This output is the chip select signal for bank 0.
	nCS1	Output	This output is the chip select signal for bank 1. It represents a secondary function for I/O port PIO2[6].
	nRD	Output	This output is the read signal for SRAM banks (0 and 1).
	nWRL	Output	This output is the Write Enable Low signal for SRAM banks (0 and 1).
	nWRH	Output	This output is the Write Enable High signal for SRAM banks (0 and 1). It represents a secondary function for I/O port PIO2[5].
	nWRE	Output	This output is the Write Enable signal for SRAM banks (0 and 1).
	nLB	Output	This output is the Low Byte Select signal for SRAM banks (0 and 1).
	nHB	Output	This output is the High Byte Select signal for SRAM banks (0 and 1). It represents a secondary function for I/O port PIO2[5].
	nRAS0	Output	This output is the Row Address Strobe signal for bank 2. It represents a secondary function for I/O port PIO2[2].
	nRAS1	Output	This output is the Row Address Strobe signal for banks 3. It represents a secondary function for I/O port PIO2[4].
	nCASL	Output	This output is the Column Address Strobe Low signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[1].
	nCASH	Output	This output is the Column Address Strobe High signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[3].
	nWE	Output	This output is the Write Enable signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[0].
	nCAS	Output	This output is the Column Address Strobe signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[1].
	nWH	Output	This output is the Write Enable High signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[3].
	nWL	Output	This output is the Write Enable Low signal for DRAM banks (2 and 3). It represents a secondary function for I/O port PIO2[0].
	nXWAIT	Input	This input pin controls insertion of wait cycles. It represents a secondary function for I/O port PIO2[7].

PIN DESCRIPTIONS (Cont.)

Type	Signal Name	I/O Direction	Description
Bus control signals	nBREQ	Input	This input is a bus request signal from an external device. It represents a secondary function for I/O port PIO7[6].
	nBACK	Output	This output is an acknowledgment signal to a bus request signal from an external device. It represents a secondary function for I/O port PIO7[7].
Interru-pts	nEFIQ	Input	This input is an external fast interrupt request (FIQ). When accepted, the request is processed as an FIQ exception.
	nEIR[7:0]	Input	This inputs are external interrupt requests. They represent secondary functions for I/O port PIO3[7:0].
Timers	TMIN[5:0]	Input	These pins function as capture trigger input pins for Flexible Timer channels 5-0 in capture mode. They represent secondary functions for I/O port PIO4[5:0].
	TMOUT[5:0]	Output	These pins function as output pins for Flexible Timer channels 5-0 in compare output or PWM mode. They represent secondary functions for I/O port PIO4[5:0].
	TMCLK[1:0]	Input	These pins function as Flexible Timer channels 1 and 0 clock input pins. They represent secondary functions for I/O port PIO4[7:6].
Serial ports	ASI_TXD	Output	This output is the transmit data for the Asynchronous Serial Interface. It represents a secondary function for I/O port PIO5[7].
	ASI_RXD	Input	This input is the receive data for the Asynchronous Serial Interface. It represents a secondary function for I/O port PIO5[6].
	CSI0_TXD	Output	This output is the transmit data for the Clock Synchronous Serial Interface 0. It represents a secondary function for I/O port PIO5[2].
	CSI0_RXD	Input	This input is the receive data for the Clock Synchronous Serial Interface 0. It represents a secondary function for I/O port PIO5[1].
	CSI0_SCLK	Bidirectional	This pin accepts/provides clock signal for the Clock Synchronous Serial Interface 0. It represents a secondary function for I/O port PIO5[0].
	CSI1_TXD	Output	This output is the transmit data for the Clock Synchronous Serial Interface 1. It represents a secondary function for I/O port PIO5[5].
	CSI1_RXD	Input	This input is the receive data for the Clock Synchronous Serial Interface 1. It represents a secondary function for I/O port PIO5[4].
	CSI1_SCLK	Bidirectional	This pin accepts/provides clock signal for the Clock Synchronous Serial Interface 1. It represents a secondary function for I/O port PIO5[3].

PIN DESCRIPTIONS (Cont.)

Type	Signal Name	I/O Direction	Description
Analog-to-digital converter	VREF	Input	This input is the reference voltage for the analog-to-digital converter channels 7-0. Connect it to VDD.
	AI[7:0]	Input	These are analog signal input pins for analog-to-digital converter channels 7-0.
Debugging interface	TDI	Input	This input is the serial data input for the debugging scan circuit. It represents a secondary function for I/O port PIO8[7].
	TDO	Output	This output is the serial data output for the debugging scan circuit. It represents a secondary function for I/O port PIO8[6].
	nTRST	Input	"L" level input to this pin resets the debugging scan circuit. It represents a secondary function for I/O port PIO8[5].
	TMS	Input	This input selects the mode for the debugging scan circuit. It represents a secondary function for I/O port PIO8[4].
	TCK	Input	This input is the serial clock input for the debugging scan circuit. It represents a secondary function for I/O port PIO8[3].
	DBGEN	Input	"H" level input to this pin enables the CPU's debugging function. It represents a secondary function for I/O port PIO8[2].
	DBGRQ	Input	This input is a debugging request signal from an external device. It represents a secondary function for I/O port PIO8[1].
	DBGACK	Output	This output is an acknowledgment signal to a debugging request signal from an external device. It represents a secondary function for I/O port PIO8[0].
I/O ports	PIO8[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO7[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO6[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO5[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO4[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO3[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO2[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO1[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.
	PIO0[7:0]	Bidirectional	These form an 8-bit I/O port. I/O directions are specified at the bit level.

PIN DESCRIPTIONS (Cont.)

Type	Signal Name	I/O Direction	Description
Clock control	OSC0	Input	This pin is for connecting a crystal oscillator. If an external clock is used, supply it to this pin.
	OSC1	Output	This pin is for connecting a crystal oscillator. If an external clock is used, leave this pin open.
	CLKOUT	Output	This output is the internal system clock signal.
	FSEL	Input	Connect this pin to VDD or ground to indicate the frequency range for the basic clock.
	PLLEN	Input	Connect this pin to VDD to enable the built-in phase-looked loop. If the PLL is not used because an external clock with a guaranteed duty is available, connect this pin to ground.
	VCOM	Input	This input controls the oscillation frequency of the PLL's voltage-controlled oscillator. Connect it to ground.
System control	nRST	Input	"L" level input to this pin produces an external system reset for this LSI. "H" level input then causes execution to resume from address 0x000000.
	DBSEL	Input	During a system reset of this LSI, this input specifies the width of the external data bus for bank 0. Connect this pin to VDD for a data bus width of 16bits and to ground for 8bits.
	nEA	Input	During a system reset of this LSI, this input controls the use of the internal ROM. Connect this pin to VDD to enable the ROM and to ground to disable it.
	TEST	Input	During a system reset of this LSI, this input controls the initial pin functions for the I/O port 8 pins(PIO8[7:0]). Connect this pin to VDD to initialize the port for its secondary function, the debugging interface, and to ground for I/O.
Power Supply	VDD	Input	These pins are this LSI's power supply pins. Connect them all to VDD.
	GND	Input	These pins are this LSI's ground pins. Connect them all to ground.
	AVDD	Input	This pin is the analog-to-digital converter's power supply. Connect it to VDD.
	AGND	Input	This pin is the analog-to-digital converter's ground pin. Connect it to ground.

OUTLINE of PERIPHERAL FUNCTIONS

○ I/O Ports

The I/O ports consist of nine 8-bit ports: PIOn(n=0 - 8). I/O directions are specified at the bit level. When configured for input, the pins use high-impedance input.

○ Flexible Timer

The flexible timer consists of six 16-bit timer channels. Each channel offers independent choice of four operating modes and of eight count clocks.

-Timer operating modes
- Auto-reload timer
- Compare output
- Pulse width modulation (PWM)
- Capture input

-Timer synchronization
- Timer channels can be started and stopped in union.

-External clocks
- Timer channels 0 and 1 accept external clock signals.

○ Time Base Generator

The time base generator consists of the time base counter, a frequency divider which derives the time base signals for the on-chip peripherals from the system clock signals, and watchdog timer, which counts time base clock cycles and produces a system reset signal when its internal counter overflows.

○ Asynchronous Serial Interface

The asynchronous serial interface is a serial port that frames each character of information with start and stop elements. Parameters control transfer speed (using a dedicated baud rate generator), character length, number of stop bits and use of parity.

-Built-in baud rate generator
-Character length: 7 or 8 bits
-Stop bits: 1 or 2
-Parity: none, odd, or even
-Error detection for receiving: parity, framing and overrun errors
-Full duplex operation

○ Clock Synchronous Serial Interface

The clock synchronous serial interface are two channels of serial ports that transmit 8-bit data synchronized with internal or external clock signals.

○ **Analog-to-Digital Converter**

The analog-to-digital converter is an 8-bit successive approximation analog-to-digital converter with eight input channels and four result registers. It offers two operating mode: scan mode, which sequentially converts the inputs from the selected set of four input channels, and select mode, which converts the input from a single input channel.

-Resolution: 8 bits
-Eight analog input channels
-Four result registers for holding conversion results
-Operating modes
- Scan modes: Sequential conversion of the analog inputs from the upper or lower set of four input channels
- Select mode: Conversion of the analog inputs from a single input channel

○ **Interrupt Controller**

The interrupt controller manages interrupt requests from 9 external sources and 19 internal ones and passes them on to the CPU as interrupt request (IRQ) or fast interrupt request (FIQ) exception requests. It supports eight interrupt levels for each source for use in priority control.

-The interrupt controller supports 9 external interrupt sources connected to nEFIQ and nEIR[7:0] pins and 19 internal interrupt sources, including the serial ports and the flexible timer channels.
-The interrupt controller simplifies interrupt priority control with a choice of eight interrupt levels for each source.
-The interrupt controller assigns a unique interrupt number to each source to permit rapid branching to the appropriate routine.

○ **External Memory Controller**

The external memory controller generates control signals for accessing external memory (ROM, SRAM, DRAM, etc.), and other devices with address in the external memory space.

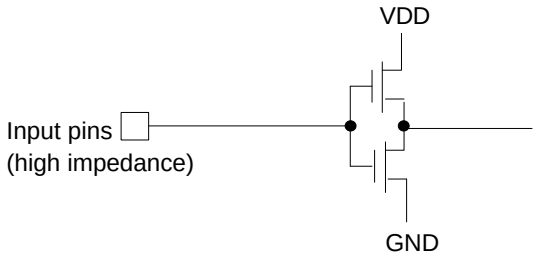
-Support for direct connection of ROM, SRAM and I/O devices
- Strobe signal outputs for a variety of memory and I/O devices
-Support for direct connection of DRAM
- Multiplexed row and column addresses
- Random access and high-speed paged modes
- Programmable wait cycle insertion
-Memory space divided into four banks
- Two banks for ROM, SRAM and I/O devices
- Two banks for DRAM
- Address space of 16 megabytes for each bank
- Separate data bus width (8 or 16 bits), wait cycle, and off time setting for each bank
-Single-stage store buffer permitting internal access during a wait cycle to external memory or device
-Arbitration of external bus requests from external devices

○ **Clock Controller**

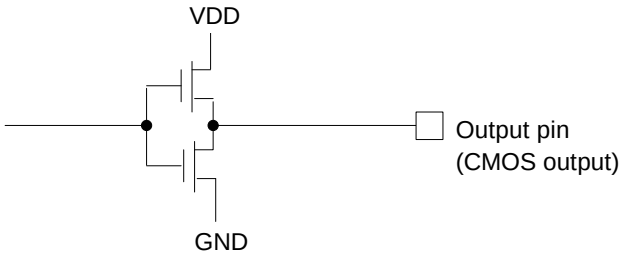
The clock controller controls the oscillator circuit based on a crystal oscillator and a built-in phase-locked loop which together generate and control the system clock signal. It offers a choice of divider ratio (1/1, 1/2 and 1/4) for adjusting operating clock frequency to match the load of processing. It also controls the transitions to and from a stand-by mode, HALT mode.

CONFIGURATIONS of PINS and I/O PORTS

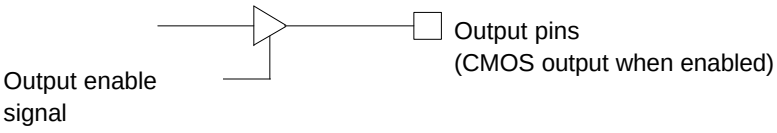
○ **Input Pins (nRST, nEA, DBSEL, TEST, nEFIQ, FSEL, PLLEN, VCOM)**



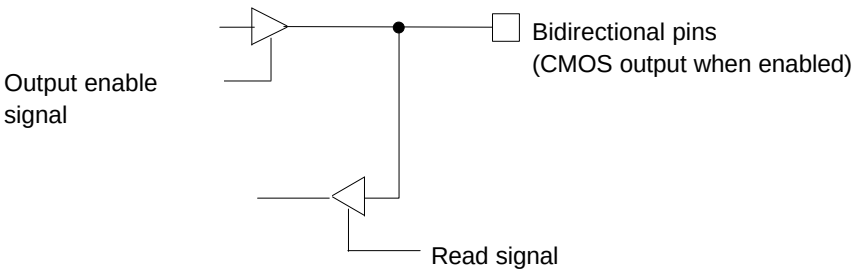
○ **Output Pin (CLKOUT)**



○ **Tri-state output pins (XA23 - XA1, nLB/XA0, nCS0, nRD, nWRE/nWRL)**

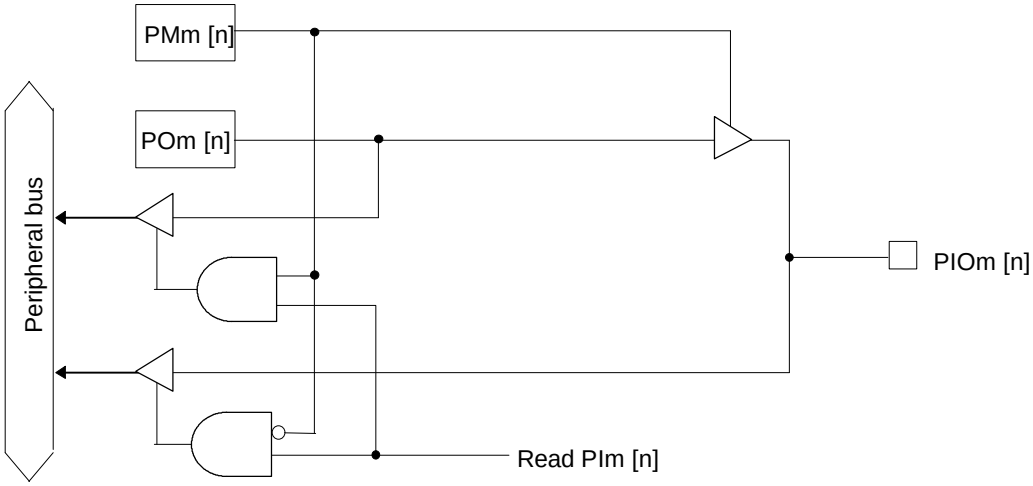


○ **Bidirectional pins (XD7 - XD0)**



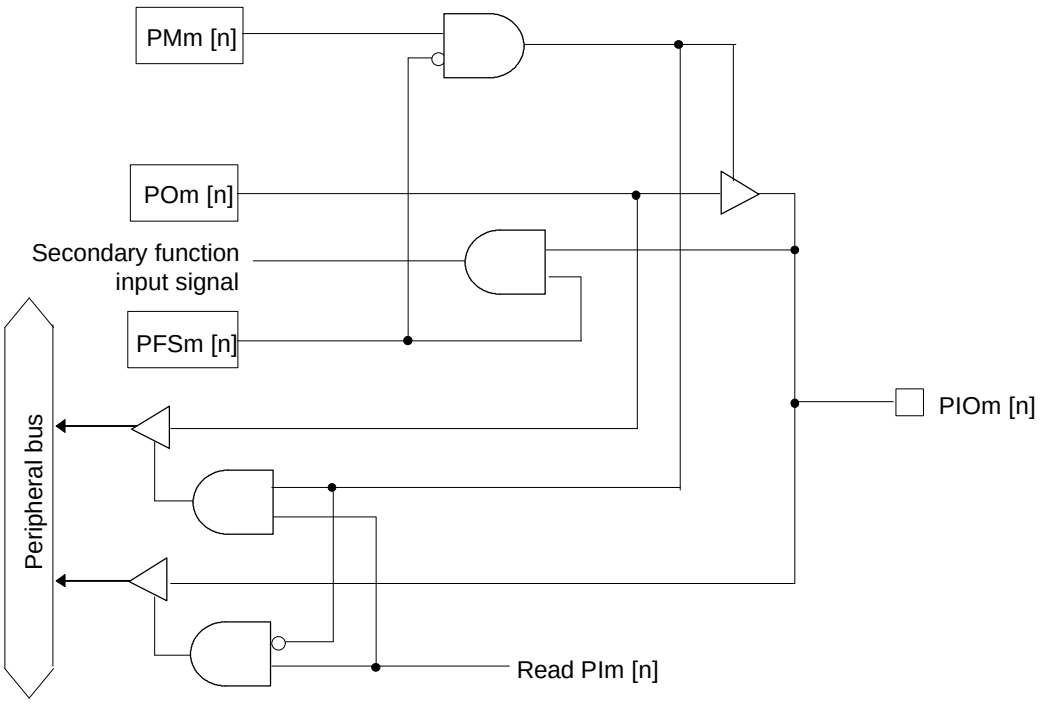
○ **I/O port A (I/O ports without second functions)**

PIO6[7:0], PIO7[5:0]



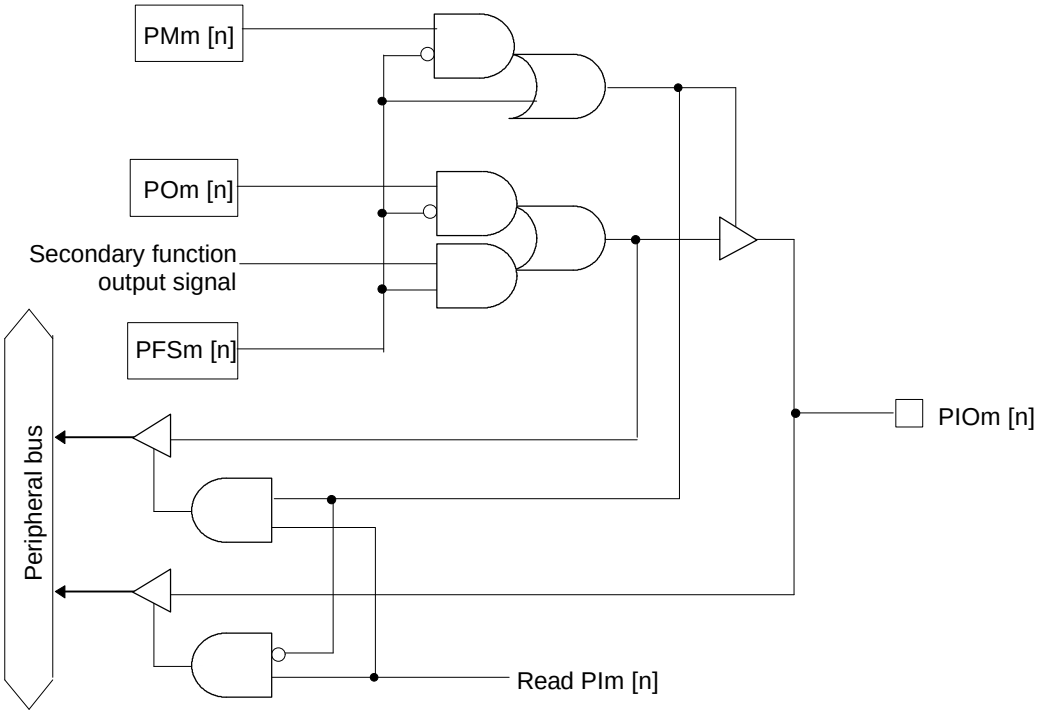
○ **I/O port B (I/O ports with second functions of input)**

PIO2[7], PIO3[7:0] , PIO4[7:6] , PIO5[6] , PIO5[4], PIO5[1] , PIO7[6] , PIO8[7] , PIO8[5:1]



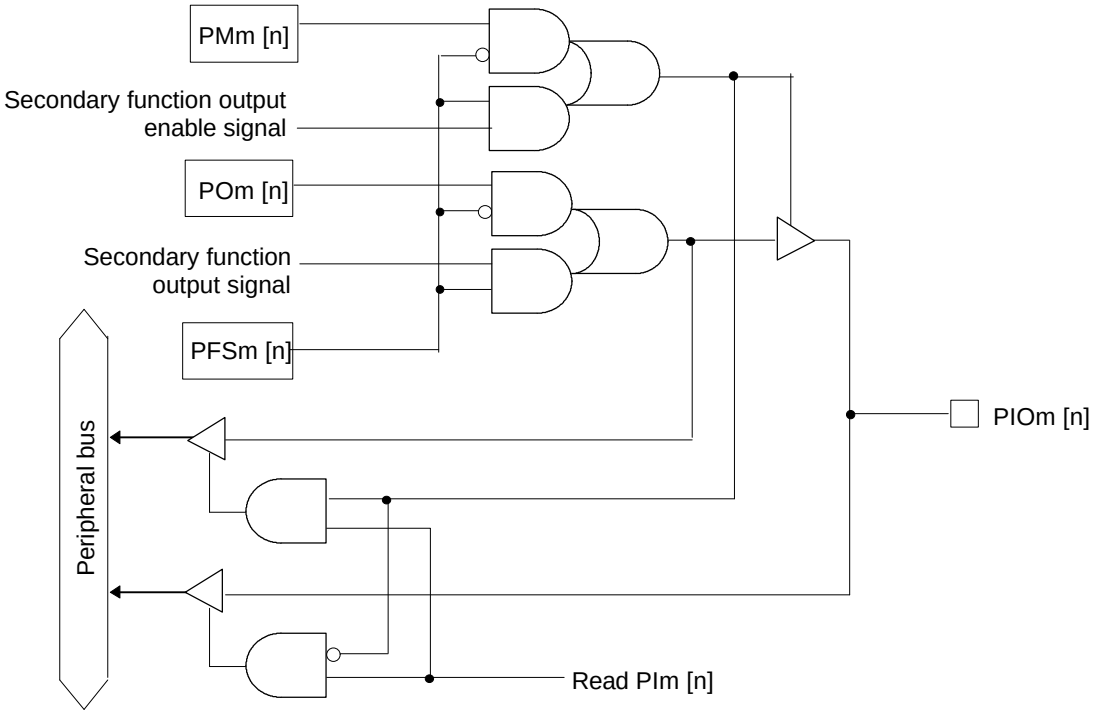
○ **I/O port C (I/O ports with second functions of output)**

PIO5[7], PIO5[5], PIO5[2], PIO7[7], PIO8[6], PIO8[0]



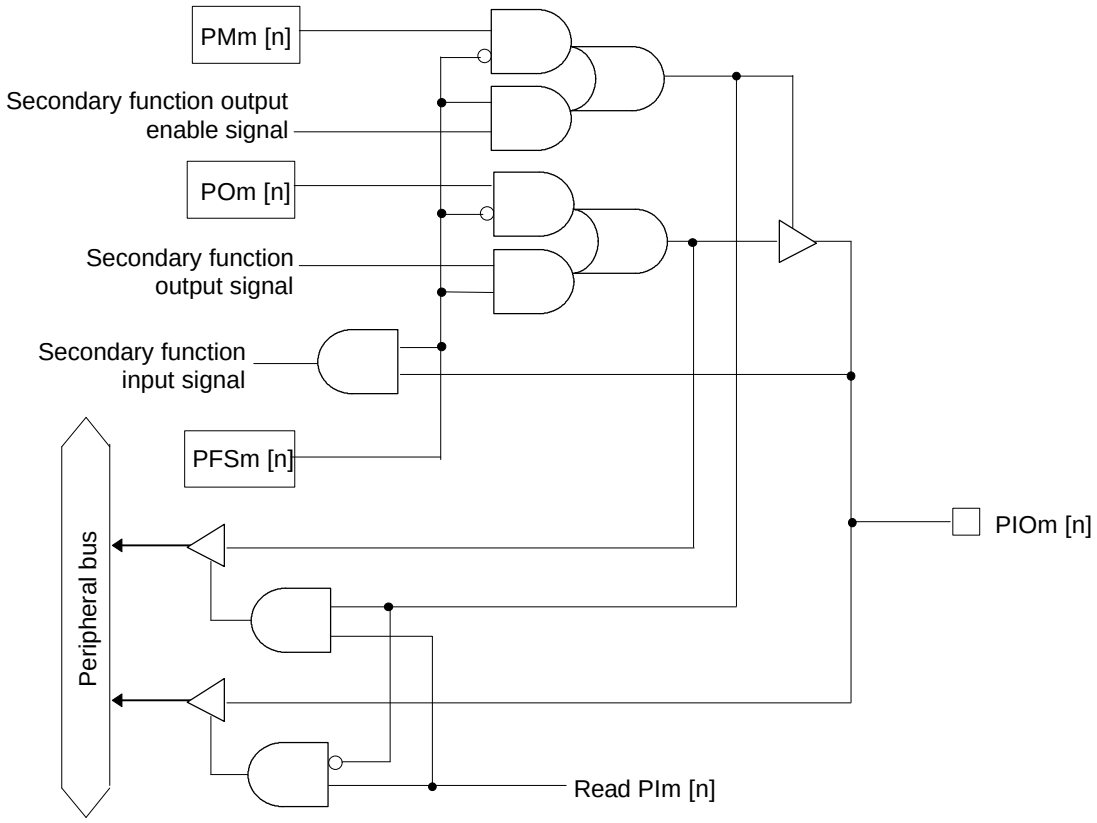
○ **I/O port D (I/O ports with second functions of tri-state output)**

PIO0[7:0], PIO2[6:0]



I/O port E (I/O ports with second functions of input and output)

PIO1[7:0], PIO4[5:0], PIO5[3], PIO5[0]



ELECTRICAL CHARACTERISTICS

○ **Absolute Maximum ratings**

Item	Symbol	Condition	Rated Value	Unit
Power supply	V_{DD}	V_{DD}=AV_{DD}=V_{REF} GND=AGND=0V	-0.3 to 4.6	V
Input voltage	V_{IN}		-0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AI}		-0.3 to AV_{DD} +0.3	
Output current	I_O	Ta=25V	12	mA
Power dissipation	P_D		850	mW
Storage temperature	T_{STG}	-	-55 to +150	°C

○ **Recommended Operating Conditions**

(Condition: GND=AGND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply	V_{DD}	-	2.7	3.3	3.6	V
Analog power supply	AV_{DD}	V_{DD}=AV_{DD}	2.7	3.3	3.6	
Analog reference voltage	V_{REF}	-	AV_{DD}-0.3	-	AV_{DD}	
Analog input voltage	V_{AI}	-	AGND	-	V_{REF}	
Operating Frequency 1	f_{C1}	V_{DD} =3.0 to 3.6V, 1	4	-	25	MHz
Operating Frequency 2	f_{C2}	V_{DD} =2.7 to 3.6V, 2	4	-	20	
Ambient temperature	T_a	-	-40	25	+85	°C

1

Basic clock frequency from the oscillator circuit or an external clock signal	PLLEN Input	FSEL Input	Operating Frequency 1 f_{C1}
4 - 6.25MHz	"H" level (Connect to V_{DD})	"H" level (Connect to V_{DD})	4 - 25MHz
8 - 12.5MHz		"L" level (Connect to GND)	4 - 25MHz
4 - 25MHz (External clock only)	"L" level (Connect to GND)	"H" level (Connect to V_{DD}) or "L" level (Connect to GND)	4 - 25MHz

2

Basic clock frequency from the oscillator circuit or an external clock signal	PLLEN Input	FSEL Input	Operating Frequency 2 f_{C2}
4 - 5MHz	"H" level (Connect to V_{DD})	"H" level (Connect to V_{DD})	4 - 20MHz
8 - 10MHz		"L" level (Connect to GND)	4 - 20MHz
4 - 20MHz (External clock only)	"L" level (Connect to GND)	"H" level (Connect to V_{DD}) or "L" level (Connect to GND)	4 - 20MHz

○ **DC Characteristics**

(Condition: V_{DD}=AV_{DD}=V_{REF}=2.7V to 3.6V, GND=AGND=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	V_{IH1}	1	0.65x V_{DD}	-	V_{DD}+0.3	V
High level input voltage 2	V_{IH2}	2	2	-	V_{DD}+0.3	
Low level input voltage 1	V_{IL1}	1	-0.3	-	0.3x V_{DD}	
Low level input voltage 2	V_{IL2}	2	-0.3	-	0.8	
High level output voltage	V_{OH}	I_{OH}=-4mA I_{OH}=-100uA	2.2(*2) V_{DD}-0.2	- -	- -	
Low level output voltage	V_{OL}	I_{OL}= 4mA	-	-	0.4	
Input leak current 1	$\|I_{LI}\|$	V_I=0/V_{DD} ,3	-	-	2.0(*3)	µA
Input leak current 2	$\|I_{L2}\|$	V_I=0/V_{DD} ,4	-	-	10.0(*3)	
Output leak current	$\|I_{LO}\|$	V_O=0/V_{DD}	-	-	2.0(*3)	
Input capacity	C_I	-	-	6	-	µF
Output capacity	C_O	-	-	9	-	
Input/output capacity	C_{IO}	-	-	10	-	
Power consumption (in HALT mode)	I_{DDH}	f_C= 25MHz No load	-	30	50	mA
Power consumption	I_{DD}		-	60	100	

1 Applied to PIO8 - PIO0, XD7 - XD0, nEFIQ
2 Applied to nRST, nEA, DBSEL, TEST, FSEL, PLLEN, VCOM
3 Applied to Input pins other than OSC0
4 Applied to OSC0

(*1): Typ. means that V_{DD}=3.3V, Ta=25 °C
(*2): 2.4V in case of that V_{DD}=AV_{DD}=V_{REF}=3.0 to 3.6V
(*3): 20µA in case of that T_a is equal or greater than 50 °C

AC Characteristics

(Condition: V_{DD}=AV_{DD}=V_{REF}=2.7V to 3.6V, GND=AGND=0V,Ta=-40 to +85°C)

● Clock timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_C	V_{DD} =3.0 to 3.6V	4	-	25	MHz
Clock cycle time	t_C		40	-	250	ns
Clock high level pulse width	t_{CH}		16	-	-	
Clock low level pulse width	t_{CL}		16	-	-	
External clock frequency	f_{EXC}		4	-	25	MHz
External clock cycle time	t_{EXC}		40	-	250	ns
External clock high level pulse width	t_{EXCH}		16	-	-	
External clock low level pulse width	t_{EXCL}		16	-	-	
Clock frequency	f_C	V_{DD} =2.7 to 3.6V	4	-	20	MHz
Clock cycle time	t_C		50	-	250	ns
Clock high level pulse width	t_{CH}		20	-	-	
Clock low level pulse width	t_{CL}		20	-	-	
External clock frequency	f_{EXC}		4	-	20	MHz
External clock cycle time	t_{EXC}		50	-	250	ns
External clock high level pulse width	t_{EXCH}		20	-	-	
External clock low level pulse width	t_{EXCL}		20	-	-	
Clock rise time	t_R	-	-	-	5	ns
Clock fall time	t_F	-	-	-	5	
External clock rise time	t_{EXR}	-	-	-	5	
External clock fall time	t_{EXF}	-	-	-	5	

- Control Signals Timing

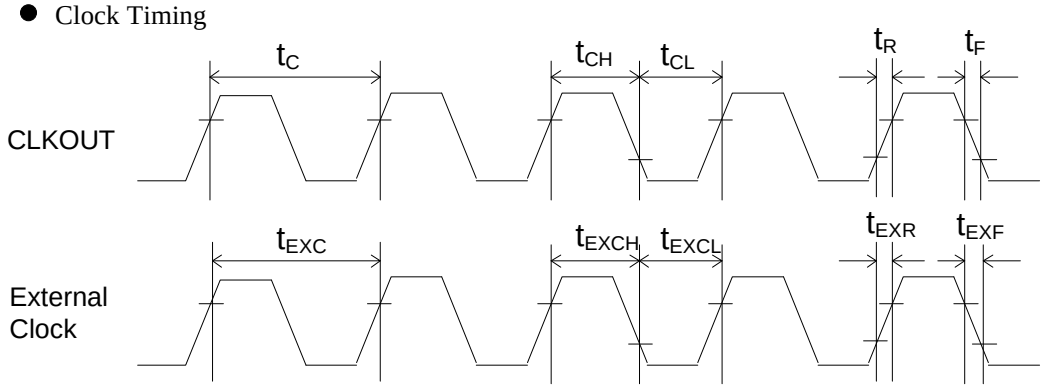
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
nRST pulse width(*1)	t_{RSTW1}	-	$2t_C$	-	-	ns
nRST pulse width(*2)	t_{RSTW2}		Oscillation stable time	-	-	-
nEFIQ pulse width	t_{EFIQW}	-	$2t_C$	-	-	ns
nEIR pulse width	t_{EIRW}	-	$2t_C$	-	-	
TMIN pulse width	t_{TMINW}	-	$2t_C$	-	-	
TMCLK pulse width	t_{TMCLKW}	-	$2t_C$	-	-	
SCLKfrequency	f_{SC}	-	-	-	$1/8f_C$	MHz
SCLK high level pulse width	t_{SCLKH}	-	$4t_C$	-	-	ns
SCLK low level pulse width	t_{SCLKL}	-	$4t_C$	-	-	
TXD delay time	t_{TXD}	C_L=50pF	-	-	$1t_C$+22	
RXD set-up time	t_{RXS}	-	$0.5t_C$	-	-	
RXD hold time	t_{RXH}	-	$1.5t_C$	-	-	
DBGRQ set-up time	t_{RQS}	-	1.0	-	-	
DBGRQ hold time	t_{RQH}	-	2.6	-	-	
DBGACK delay time	t_{DBGD}	C_L=50pF	2.4	-	15.2	

(*1): Not applied to power-on.
(*2): Applied to power-on.

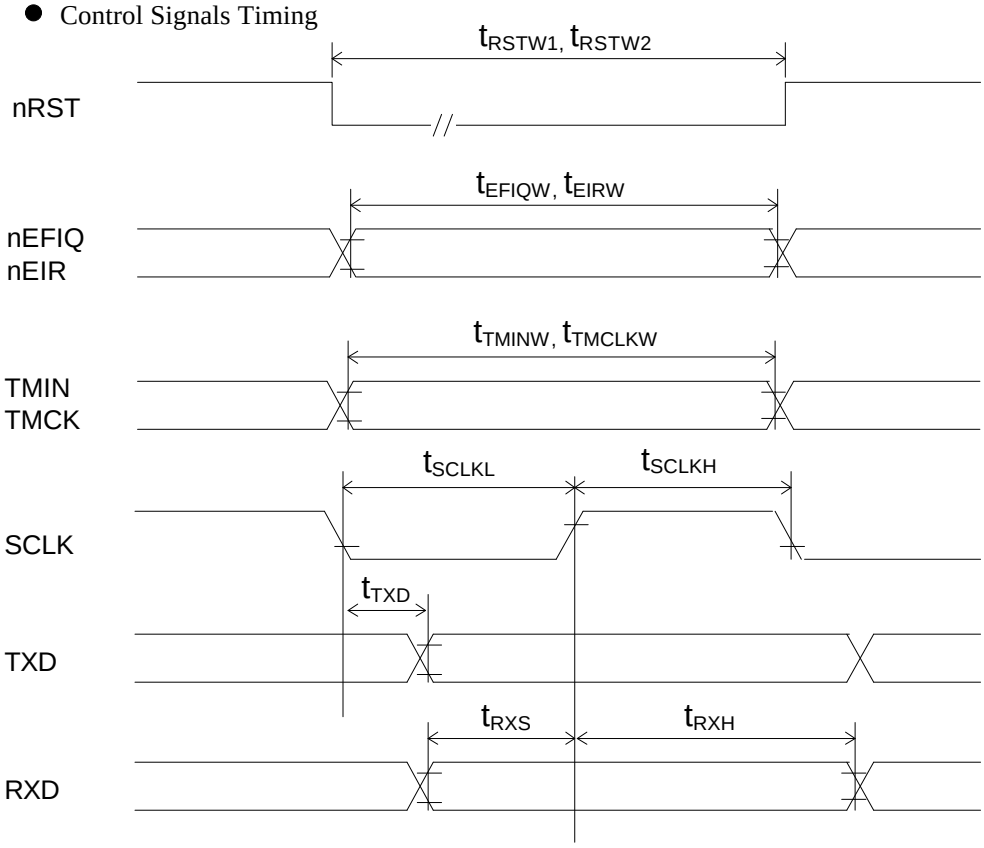
- External Bus Timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
XA[23:1],nLB/XA0 delay time	t_{XAD}	C_L=50pF	3	-	14	ns
XD[15:0] output delay time	t_{XDOD}		5	-	20	
XD[15:0] input set-up time	t_{XDIS}		11	-	-	
XD[15:0] input hold time	t_{XDIH}		0	-	-	
nXWAIT set-up time	t_{XWAITS}		3	-	-	
nXWAIT hold time	t_{XWAITH}		0	-	-	
nHB delay time	t_{HBD}		2	-	12	
nCS[1:0] delay time	t_{CSD}		2	-	11	
nWRE,nWRH,nWRL delay time	t_{WRD}		3	-	12	
nRD delay time	t_{RDD}		4	-	11	
nRAS[1:0] delay time	t_{RASD}		3	-	12	
nCAS delay time	t_{CASD}		3	-	13	
nWE,nWH,nWL delay time	t_{WED}		2	-	12	
nBREQ set-up time	t_{BREQS}		5	-	-	
nBREQ hold time	t_{BREQH}		3	-	-	
nBACK delay time	t_{BACKD}		4	-	13	
High-impedance delay time	t_{XHD}		4	-	13	

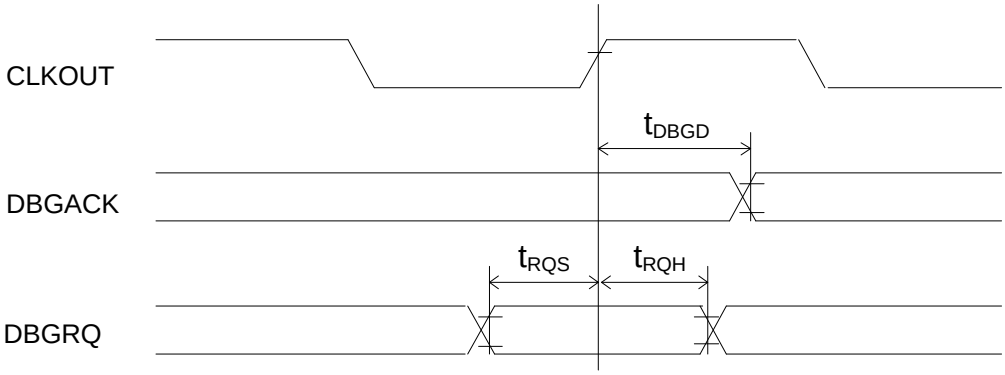
- Clock Timing



- Control Signals Timing

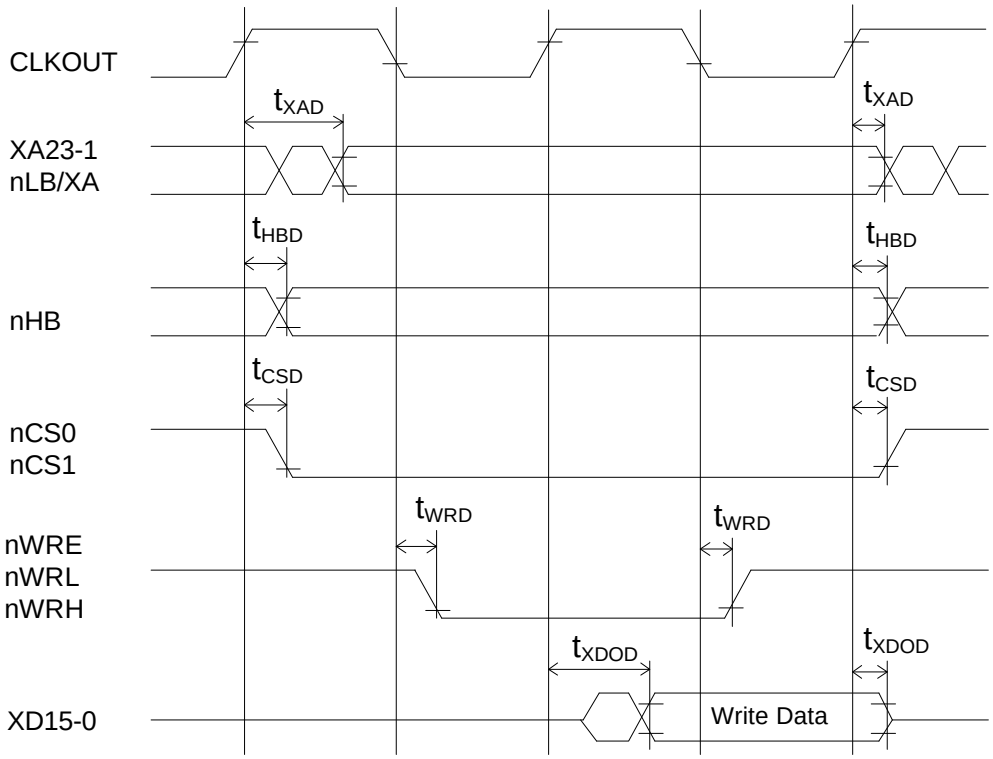


- Control Signals Timing (Cont.)

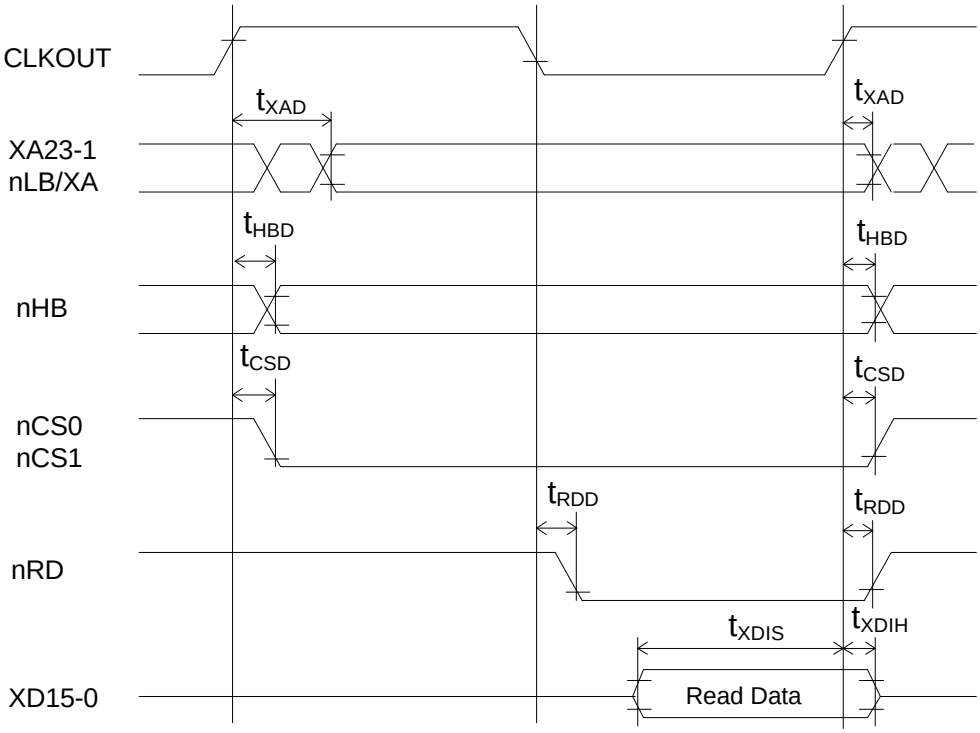


- External Bus Timing

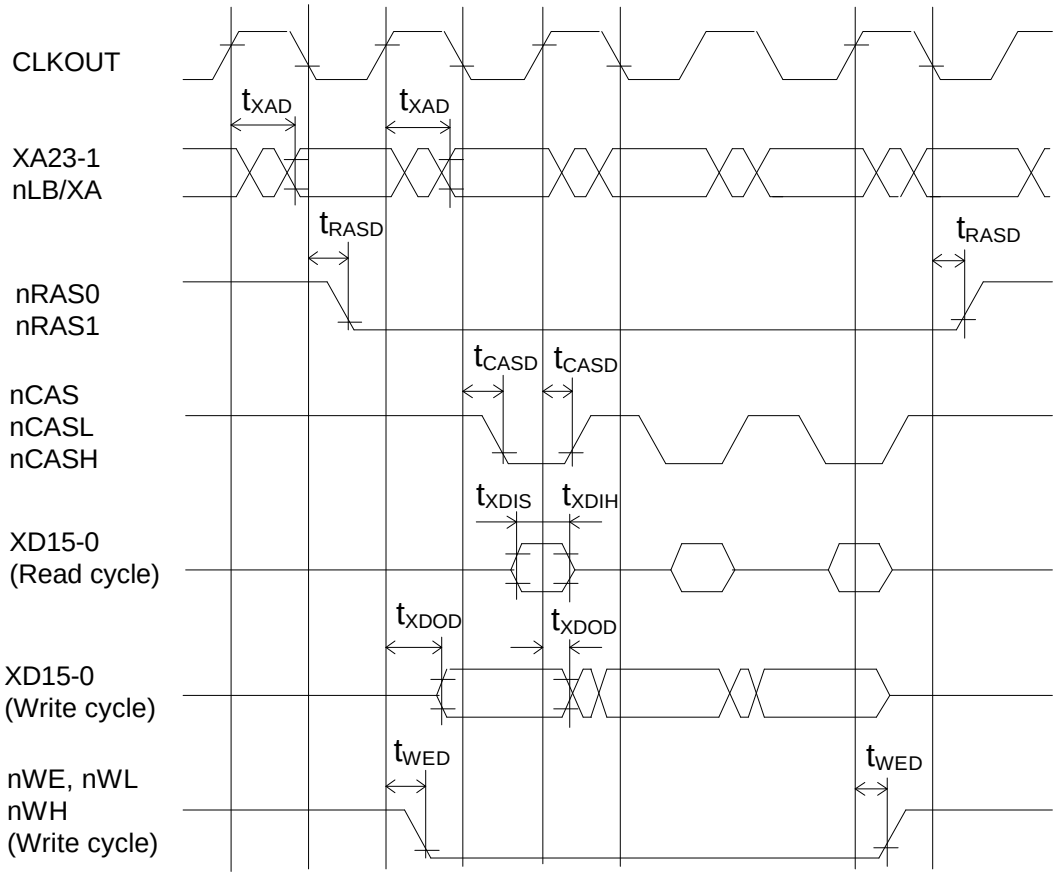
  Bank 0 and Bank 1 Write Cycle Timing



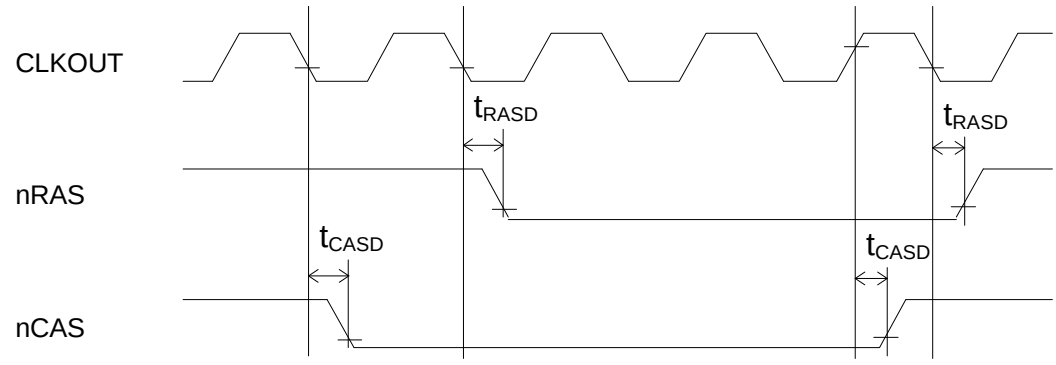
Bank 0 and Bank 1 Read Cycle Timing



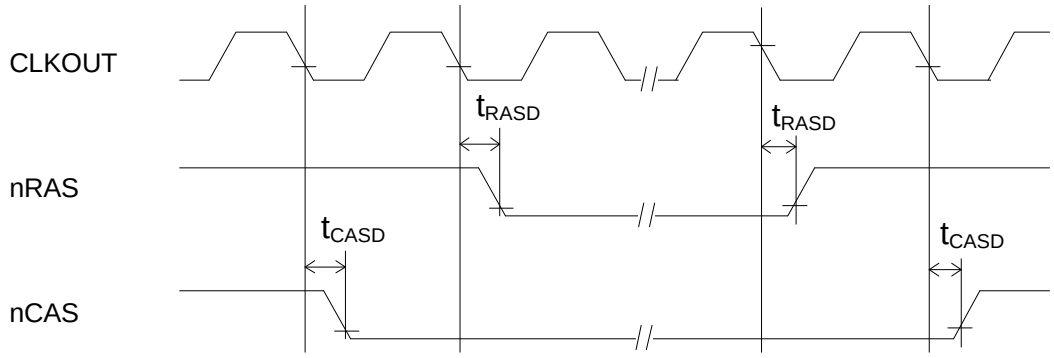
Bank 2 and Bank 3 Read/Write Cycle Timing



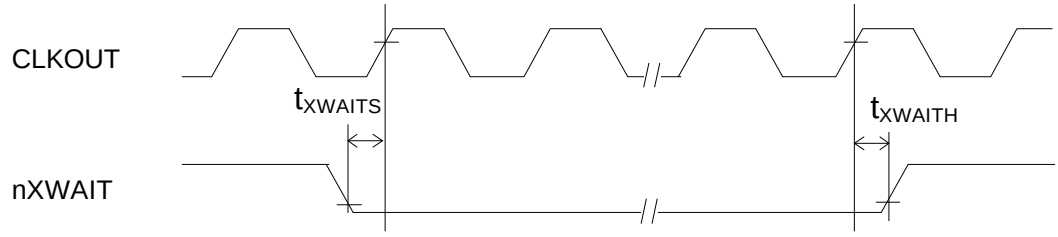
CAS before RAS (CBR) Refresh



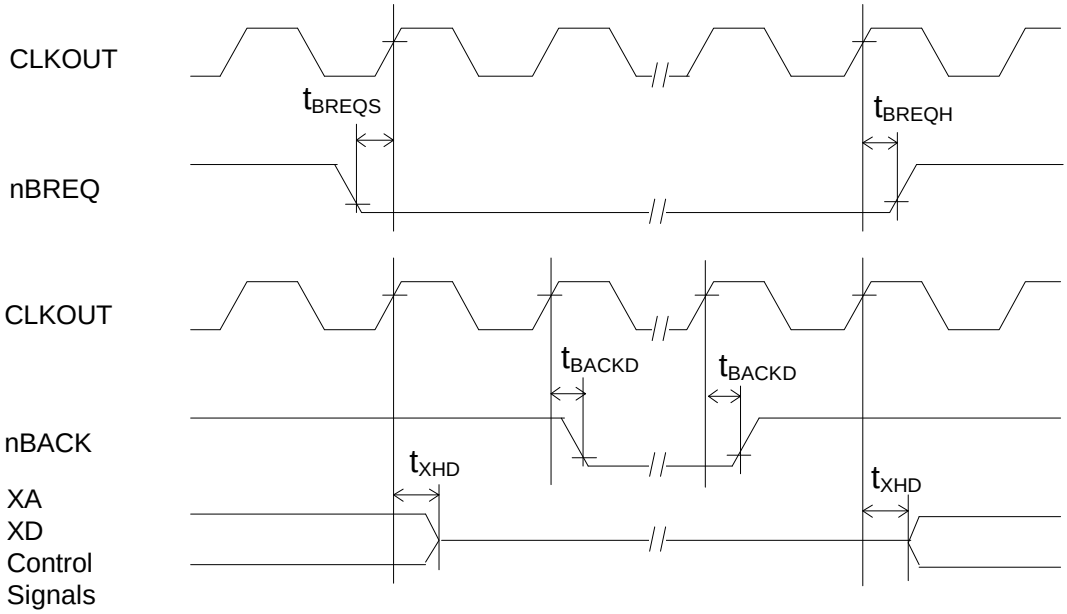
Self Refresh



nXWAIT Input Timing



External Bus Release Timing



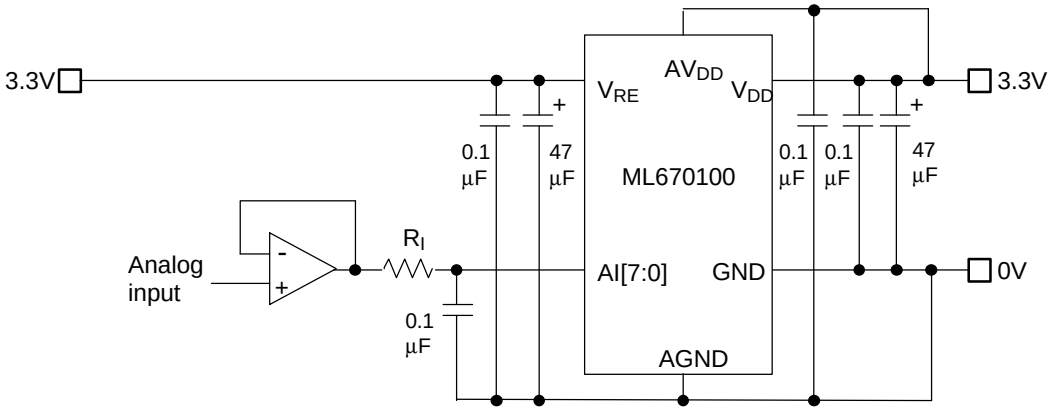
○ **A-to-D Converter Characteristics**

(Condition: V_{DD}=AV_{DD}=V_{REF}=2.7V to 3.6V, GND=AGND=0V,Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the following recommended circuit. Analog input source impedance R_I is equal or less than 5K Ω	-	-	8	bit
Linearity error	E_L		-3.0	-	+3.0	LSB
Differential linearity error	E_D		-1.0	-	+1.0	LSB
Zero scale error	E_{ZS}		-	-	+2.0	LSB
Full scale error	E_{FS}		-	-	-2.0	LSB
Conversion time	t_{CONV}	f_C=25MHz	-	10.68	-	μS/CH

Definitions of terms

Resolution	The minimum distinguishable analog value. For 8 bits, 2^8=256, i.e.(VREF-AGND)/256.
Linearity error	Variance between the ideal conversion characteristics as an 8-bit A-to-D converter and actual conversion characteristics (does not include quantatized error).
Differential linearity error	Indicates the smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1LSB=(VREF-AGND)/256 ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.
Zero scale error	Variance between the ideal conversion characteristics at the switching point of digital output ”0x00” - ”0x01” and actual conversion characteristics.
Full scale error	Variance between the ideal conversion characteristics at the switching point of digital output ”0xFE” - ”0xFF” and actual conversion characteristics.



R_I (Analog input source impedance) is equal or less than 5KΩ