OKI

Oki, Network Solutions for a Global Society

OKI Semiconductor

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ML674000

32-bit General-purpose Single-chip Microcontroller

GENERAL DESCRIPTION

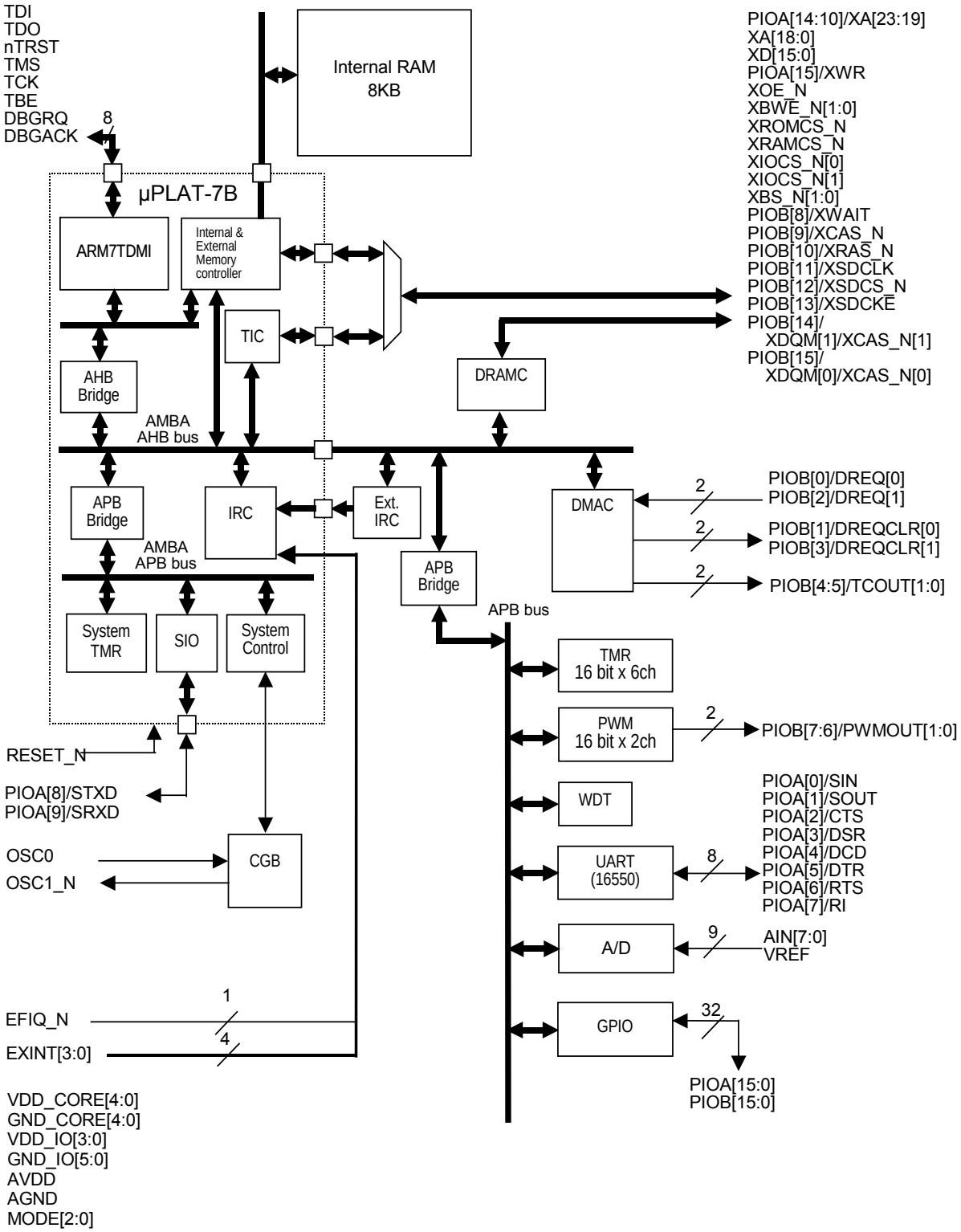
This LSI incorporates µPLAT®-7B, employing the CPU core ARM7TDMI™, as the CPU platform and operates at maximum 33 MHz. It contains built-in RAM and peripheral IOs such as Timer, WDT, GPIO, PWM, UART (16550 compatible), AD converter, DMA controller and DRAM controller, etc. and can be used as a microcontroller for configuring various systems.

FEATURES

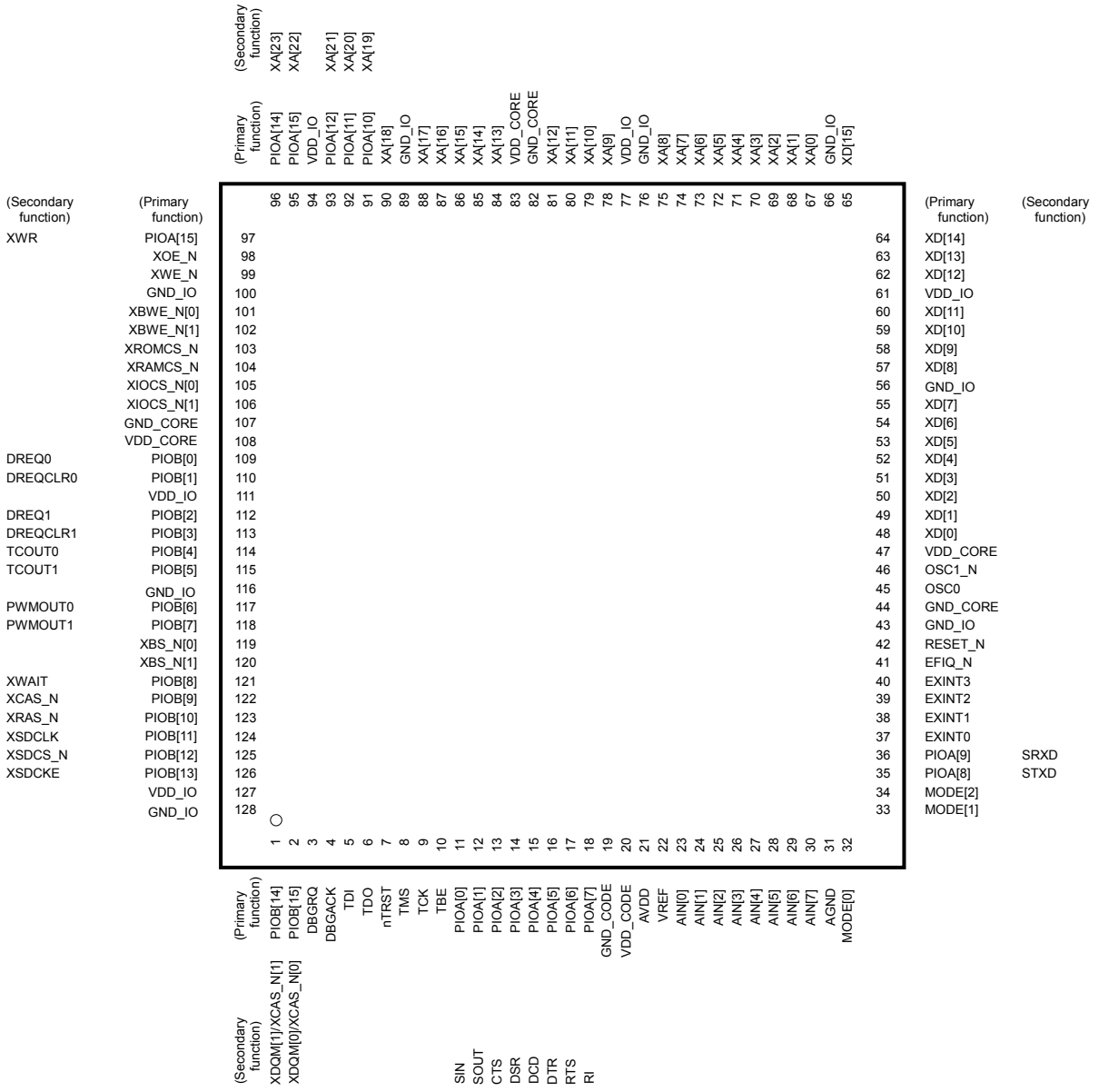
CPU	32-bit RISC CPU (ARM7TDMI) 32-bit instructions (ARM Instructions) and 16-bit instructions (Thumb Instructions) mixed General purpose registers : 31 x 32 bits Barrel shifter and multiplier (32 bit x 8 bit, Modified Booth's Algorithm) Little endian Built-in debug function
Internal memory	RAM 8 KB (32-bit access)
External memory controller	ROM (FLASH): 16 Mbytes SRAM: 16 Mbytes DRAM: 16 Mbytes (SDRAM and EDO-DRAM support) External IO devices: 16 Mbytes x 2 banks (with wait control by external signal) Programmable wait setting by each bank
Interrupt controller	24 sources: 19 internals and 5 externals (IRQ: 4, FIQ: 1)
DMA controller	2 channels: Dual address mode, cycle steal and burst tranfer mode maximum transfer count: 65536
Timer	1 channel: 16-bit auto reload for operating system 6 channels: 16-bit auto reload for application 1 channel: 16 bit watchdog timer
Serial interface	1 channel: asynchronous, Xon/Xoff interface 1 channel: asynchronous with 16-byte FIFO
Parallel I/O port	2 channels x 16 bits (bitwise input/output settings)
PWM	2 channels x 16 bits
AD converter	8 channels x 10 bits
Power down mechanism	Standby and Halt (clock stop by each function block) Clock gear (selectable 1/1, 1/2, 1/4, 1/8, 1/16 input clock frequency)
JTAG interface	Connectable to JTAG ICE (ex. ARM MutiICE)
Power supply voltage	Core section: 2.25 V to 2.75 V, IO section: 3.0 V to 3.6 V
Operating frequency	33 MHz (Max.)
Operating temperature (ambient temperature)	–40°C to +85°C
Package	128-pin plastic TQFP (TQFP128-P-1414-0.40-K)

ARM

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic TQFP

LIST OF PINS

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
1	PIOB[14]	I/O	General port (with interrupt function)	XDQM[1]/XCAS_N[1]	O	INPUT/OUTPUT mask/CAS (MSB)
2	PIOB[15]	I/O	General port (with interrupt function)	XDQM[0]/XCAS_N[0]	O	INPUT/OUTPUT mask/CAS (LSB)
3	DBGRQ	I	Input signal for debug	—		
4	DBGACK	O	Output signal for debug	—		
5	TDI	I	JTAG data input	—		
6	TDO	O	JTAG data output	—		
7	nTRST	I	JTAG reset	—		
8	TMS	I	JTAG mode selection	—		
9	TCK	I	JTAG clock	—		
10	TBE	I	Input signal for testing	—		
11	PIOA[0]	I/O	General-purpose port (with interrupt function)	SIN	I	UART Serial Data In
12	PIOA[1]	I/O	General-purpose port (with interrupt function)	SOUT	O	UART Serial Data Out
13	PIOA[2]	I/O	General-purpose port (with interrupt function)	CTS	I	UART Clear To Send
14	PIOA[3]	I/O	General-purpose port (with interrupt function)	DSR	I	UART Data Set Ready
15	PIOA[4]	I/O	General-purpose port (with interrupt function)	DCD	I	UART Data Carrier Detect
16	PIOA[5]	I/O	General-purpose port (with interrupt function)	DTR	O	UART Data Terminal Ready
17	PIOA[6]	I/O	General-purpose port (with interrupt function)	RTS	O	UART Request To Send
18	PIOA[7]	I/O	General-purpose port (with interrupt function)	RI	I	UART Ring Indicator
19	GND_CORE	GND	GND for CORE	—		
20	VDD_CORE	VDD	Power supply for CORE	—		
21	AVDD	VDD	Power supply for A/D converter	—		
22	VREF	I	Reference voltage for A/D converter	—		
23	AIN[0]	I	A/D converter analog input port	—		
24	AIN[1]	I	A/D converter analog input port	—		
25	AIN[2]	I	A/D converter analog input port	—		
26	AIN[3]	I	A/D converter analog input port	—		
27	AIN[4]	I	A/D converter analog input port	—		
28	AIN[5]	I	A/D converter analog input port	—		
29	AIN[6]	I	A/D converter analog input port	—		
30	AIN[7]	I	A/D converter analog input port	—		
31	AGND	GND	GND for A/D converter	—		
32	MODE[0]	I	Mode setting	—		
33	MODE[1]	I	Mode setting	—		
34	MODE[2]	I	Mode setting	—		
35	PIOA[8]	I/O	General-purpose port (with interrupt function)	STXD	O	SIO send data output
36	PIOA[9]	I/O	General-purpose port (with interrupt function)	SRXD	I	SIO receive data input
37	EXINT0	I	Interrupt input	—		
38	EXINT1	I	Interrupt input	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
39	EXINT2	I	Interrupt input	—		
40	EXINT3	I	Interrupt input	—		
41	EFIQ_N	I	FIQ input	—		
42	RESET_N	I	Reset	—		
43	GND_IO	GND	GND for I/O	—		
44	GND_CORE	GND	GND for CORE	—		
45	OSC0	I	Oscillation input pin	—		
46	OSC1_N	O	Oscillation output pin	—		
47	VDD_CORE	VDD	Power supply for CORE	—		
48	XD[0]	I/O	External memory access data port	—		
49	XD[1]	I/O	External memory access data port	—		
50	XD[2]	I/O	External memory access data port	—		
51	XD[3]	I/O	External memory access data port	—		
52	XD[4]	I/O	External memory access data port	—		
53	XD[5]	I/O	External memory access data port	—		
54	XD[6]	I/O	External memory access data port	—		
55	XD[7]	I/O	External memory access data port	—		
56	GND_IO	GND	GND for I/O	—		
57	XD[8]	I/O	External memory access data port	—		
58	XD[9]	I/O	External memory access data port	—		
59	XD[10]	I/O	External memory access data port	—		
60	XD[11]	I/O	External memory access data port	—		
61	VDD_IO	VDD	Power supply for I/O	—		
62	XD[12]	I/O	External memory access data port	—		
63	XD[13]	I/O	External memory access data port	—		
64	XD[14]	I/O	External memory access data port	—		
65	XD[15]	I/O	External memory access data port	—		
66	GND_IO	GND	GND for I/O	—		
67	XA[0]	O	External memory access address output port	—		
68	XA[1]	O	External memory access address output port	—		
69	XA[2]	O	External memory access address output port	—		
70	XA[3]	O	External memory access address output port	—		
71	XA[4]	O	External memory access address output port	—		
72	XA[5]	O	External memory access address output port	—		
73	XA[6]	O	External memory access address output port	—		
74	XA[7]	O	External memory access address output port	—		
75	XA[8]	O	External memory access address output port	—		
76	GND_IO	GND	GND for I/O	—		
77	VDD_IO	VDD	Power supply for I/O	—		
78	XA[9]	O	External memory access address output port	—		
79	XA[10]	O	External memory access address output port	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
80	XA[11]	O	External memory access address output port	—		
81	XA[12]	O	External memory access address output port	—		
82	GND_CORE	GND	GND for CORE	—		
83	VDD_CORE	VDD	Power supply for CORE	—		
84	XA[13]	O	External memory access address output port	—		
85	XA[14]	O	External memory access address output port	—		
86	XA[15]	O	External memory access address output port	—		
87	XA[16]	O	External memory access address output port	—		
88	XA[17]	O	External memory access address output port	—		
89	GND_IO	O	GND for I/O	—		
90	XA[18]	O	External memory access address output port	—		
91	PIOA[10]	I/O	General-purpose port (with interrupt function)	XA[19]	O	External memory access address output port
92	PIOA[11]	I/O	General-purpose port (with interrupt function)	XA[20]	O	External memory access address output port
93	PIOA[12]	I/O	General-purpose port (with interrupt function)	XA[21]	O	External memory access address output port
94	VDD_IO	VDD	Power supply for I/O			
95	PIOA[13]	I/O	General-purpose port (with interrupt function)	XA[22]	O	External memory access address output port
96	PIOA[14]	I/O	General-purpose port (with interrupt function)	XA[23]	O	External memory access address output port
97	PIOA[15]	I/O	General-purpose port (with interrupt function)	XWR	O	Transfer direction of external bus
98	XOE_N	O	Output enable (excluding SDRAM)	—		
99	XWE_N	O	Write enable	—		
100	GND_IO	GND	GND for I/O			
101	XBWE_N[0]	O	Byte write enable (LSB)	—		
102	XBWE_N[1]	O	Byte write enable (MSB)	—		
103	XROMCS_N	O	External ROM chip select	—		
104	XRAMCS_N	O	External RAM chip select	—		
105	XIOCS_N[0]	O	IO bank 0 chip select	—		
106	XIOCS_N[1]	O	IO bank 1 chip select	—		
107	GND_CORE	GND	GND for CORE	—		
108	VDD_CORE	VDD	Power supply for CORE	—		
109	PIOB[0]	I/O	General-purpose port (with interrupt function)	DREQ0	I	DMA request signal (CH0)
110	PIOB[1]	I/O	General-purpose port (with interrupt function)	DREQCLR0	O	DREQ clear signal (CH0)
111	VDD_IO	VDD	Power supply for I/O	—		
112	PIOB[2]	I/O	General-purpose port (with interrupt function)	DREQ1	I	DMA request signal (CH1)
113	PIOB[3]	I/O	General-purpose port (with interrupt function)	DREQCLR1	O	DREQ clear signal (CH1)
114	PIOB[4]	I/O	General-purpose port (with interrupt function)	TCOUT0	O	DMAC Terminal Count (CH0)
115	PIOB[5]	I/O	General-purpose port (with interrupt function)	TCOUT1	O	DMAC Terminal Count (CH1)
116	GND_IO	GND	GND for I/O	—		
117	PIOB[6]	I/O	General-purpose port (with interrupt function)	PWMOUT[0]	O	PWM output (CH0)
118	PIOB[7]	I/O	General-purpose port (with interrupt function)	PWMOUT[1]	O	PWM output (CH1)
119	XBS_N[0]	O	External bus byte select (LSB)	—		
120	XBS_N[1]	O	External bus byte select (MSB)	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
121	PIOB[8]	I/O	General-purpose port (with interrupt function)	XWAIT	I	
122	PIOB[9]	I/O	General-purpose port (with interrupt function)	XCAS_N	O	Column address strobe (SDRAM)
123	PIOB[10]	I/O	General-purpose port (with interrupt function)	XRAS_N	O	Row address strobe (SDRAM/EDO)
124	PIOB[11]	I/O	General-purpose port (with interrupt function)	XSDCLK	O	Clock for SDRAM
125	PIOB[12]	I/O	General-purpose port (with interrupt function)	XSDCS_N	O	SDRAM chip select
126	PIOB[13]	I/O	General-purpose port (with interrupt function)	XSDCKE	O	Clock enable (To SDRAM)
127	VDD_IO	VDD	Power supply for I/O	—		
128	GND_IO	GND	GND for I/O	—		

PIN DESCRIPTION

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
System					
42	RESET_N	I	Reset input	—	Negative
45	OSC0	I	Crystal oscillator connection or external clock input. Connect a crystal oscillator (16 MHz to 33 MHz), if used, to OSC0 and OSC1_N.	—	
46	OSC1_N	O	Crystal oscillator connection. Leave this pin unconnected if using external clock input.	—	
10	TBE	I	Test pin. Drive at High level	—	Negative
Debugging support. See Appendix A [pending] for specific uses.					
3	DBGRQ	I	Debugging pin. Normally connect to ground.	—	Positive
4	DBGACK	O	Debugging pin. Normally leave open.	—	Positive
9	TCK	I	Debugging pin. Normally connect to ground.	—	—
8	TMS	I	Debugging pin. Normally drive at High level.	—	Positive
7	nTRST	I	Debugging pin. Normally connect to ground.	—	Negative
5	TDI	I	Debugging pin. Normally drive at High level.	—	Positive
6	TDO	O	Debugging pin. Normally leave open.	—	Positive
General-purpose I/O ports					
11-18, 35-36, 91-93, 95-97	PIOA[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
109-110, 112-115, 117-118, 121-126 1-2	PIOB[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use. Note that enabling DRAM controller with MODE[2:0] inputs permanently configures PIOB[15:9] for their secondary functions, making them unavailable for use as port pins.	Primary	Positive
External Bus					
91-93, 95-97	XA[23:19]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM. After a reset, these pins are configured for their primary function (PIOA[14:10]).	Secondary	Positive
67-75, 78-81, 84-88, 90	XA[18:0]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive
48-55, 57-60, 62-65	XD[15:0]	I/O	Data bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
External bus control signals					
103	XROMCS_N	O	ROM bank chip select	—	Negative
104	XRAMCS_N	O	SRAM bank chip select	—	Negative
105	XIOCS_N[0]	O	I/O bank 0 chip select	—	Negative
106	XIOCS_N[1]	O	I/O bank 1 chip select	—	Negative
98	XOE_N	O	Output enable/read enable	—	Negative
99	XWE_N	O	Write enable	—	Negative
119-120	XBS_N[1:0]	O	Byte select: XBS_N[1] for MSB; XBS_N[0] for LSB	—	Negative
101	XBWE_N[0]	O	LSB write enable	—	Negative
102	XBWE_N[1]	O	MSB write enable	—	Negative
97	XWR	O	Data transfer direction for external bus, used when connecting to Motorola I/O devices. This represents the secondary function of pin PIOA[15], produced by setting bit 7 in the port control (GPCTL) register to "1."	Secondary	—
121	XWAIT	I	External I/O bank 0 WAIT signal. This input permits access to devices slower than register settings.	Secondary	Positive
External bus control signals (DRAM)					
123	XRAS_N	O	Row address strobe. Used for both EDO DRAM and SDRAM.	Secondary	Negative
122	XCAS_N	O	Column address strobe signal (SDRAM)	Secondary	Negative
124	XSDCLK	O	SDRAM clock (same frequency as internal system clock)	Secondary	—
126	XSDCKE	O	Clock enable (SDRAM)	Secondary	—
125	XSDCS_N	O	Chip select (SDRAM)	Secondary	Negative
1	XDQM[1]/XCAS_N[1]	O	Connected to SDRAM: DQM (MSB) Connected to EDO DRAM: column address strobe signal (MSB)	Secondary	Positive
2	XDQM[0]/XCAS_N[0]	O	Connected to SDRAM: DQM (LSB) Connected to EDO DRAM: column address strobe signal (LSB)	Secondary	Positive
DMA control signals					
109	DREQ0	I	Ch 0 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
110	DREQCLR0	O	Ch 0 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
114	TCOUT0	O	Indicates to Ch 0 DMA device that last transfer has started	Secondary	Positive
112	DREQ1	I	Ch 1 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
113	DREQCLR1	O	Ch 1 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
115	TCOUT1	O	Indicates to Ch 1 DMA device that last transfer has started	Secondary	Positive

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
SIO					
35	STXD	O	SIO transmit signal	Secondary	Positive
36	SRXD	I	SIO receive signal	Secondary	Positive
UART					
11	SIN	I	Serial data input	Secondary	Positive
12	SOUT	O	Serial data output	Secondary	Positive
13	CTS	I	Clear To Send. Indicates that modem or data set is ready to transfer data. Bit 4 in modem status register reflects this input.	Secondary	Negative
14	DSR	I	Data Set Ready. Indicates that modem or data set is ready to establish a communications link with UART. Bit 5 in modem status register reflects this input.	Secondary	Negative
15	DCD	I	Data Carrier Detect. Indicates that modem or data set has detected data carrier signal. Bit 7 in modem status register reflects this input.	Secondary	Negative
16	DTR	O	Data Terminal Ready. Indicates that UART is ready to establish a communications link with modem or data set. Bit 0 in modem control register controls this output.	Secondary	Negative
17	RTS	O	Request To Send. Indicates that UART is ready to transfer data to modem or data set. Bit 1 in modem control register controls this output.	Secondary	Negative
18	RI	O	Ring Indicator. Indicates that modem or data set has received telephone ring indicator. Bit 6 in modem status register reflects this input.	Secondary	Negative
PWM signals					
117	PWMOUT[0]	O	Ch 0 PWM output	Secondary	Positive
118	PWMOUT[1]	O	Ch 1 PWM output	Secondary	Positive
Analog-to-digital converter					
23	AIN[0]	I	Ch 0 analog input	—	
24	AIN[1]	I	Ch 1 analog input	—	
25	AIN[2]	I	Ch 2 analog input	—	
26	AIN[3]	I	Ch 3 analog input	—	
27	AIN[4]	I	Ch 4 analog input	—	
28	AIN[5]	I	Ch 5 analog input	—	
29	AIN[6]	I	Ch 6 analog input	—	
30	AIN[7]	I	Ch 7 analog input	—	
22	VREF	I	Analog-to-digital converter convert reference voltage	—	
21	AVDD		Analog-to-digital converter power supply	—	
31	AGND		Analog-to-digital converter ground	—	

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
Interrupt signals					
37-40	EXINT[3:0]	I	External interrupt input signals	—	Positive/ Negative
41	EFIQ_N	I	External fast interrupt input signal. Interrupt controller connects this to CPU FIQ input.	—	Negative
MODE					
32-34	MODE[2:0]	I	Operating mode control signals	—	
Power supplies					
20, 47, 83, 108	VDD_CORE		Core power supply	—	
61, 77, 94, 111, 127	VDD_IO		I/O power supply	—	
19, 44, 82, 107,	GND_CORE		Core ground	—	
43, 56, 66, 76, 89, 100, 116, 128	GND_IO		I/O ground	—	

DESCRIPTION OF FUNCTIONS

CPU

CPU core:	ARM7TDMI
Operating frequency:	1 MHz to 33 MHz
Instructions:	ARM instruction (32-bit length) and Thumb instruction (16-bit length) can be mixed.
General register bank:	31 × 32 bits
Built-in barrel shifter:	ALU and barrel shift operations can be executed by one instruction.
Multiplier:	32 bits × 8 bits (Modified Booth's Algorithm)
Built-in debug function:	JTAG interface, break point register

Built-in Memory

RAM:	8 KB (2K × 32 bits) Connected to processor bus (1 cycle access)

Interrupt Controller

Fast interrupt input (FIQ) and interrupt input (IRQ) are employed as interrupt input signals of ARM core. The interrupt controller controls these interrupt signals going to ARM core.

(1) Interrupt sources of ML674000
FIQ: 1 source, external source (external pin: EFIQ_N)
IRQ: 23 sources, internal sources : 19, external sources : 4 (external pins: EXINT [3 : 0])
(2) Interrupt priority level
Priority can be set in 8 levels for each source.
(3) External interrupt pin input
Level sense: Interrupt signal level is selected.
Edge sense: Rise or fall is selected.

Timer

7 channels of 16-bit reload timers are employed. Of these, 1 channel is used as system timer for OS.
The timers of other 6 channels are used in application software.

(1) System timer: 1 channel
16-bit auto reload timer: Used as system timer for OS
(This timer is incorporated in µPLAT-7B.)
(2) Application timer: 6 channels
16-bit auto reload timer
One shot, interval
Clock can be set for each channel

WDT

Possesses the function of interval timer mode in addition to the watch dog timer function.

(1) 16-bit timer
(2) Watch dog timer or interval timer mode can be selected
(3) Interrupt reset generation
(4) Maximum period: 200 msec or longer

PWM

This LSI contains two channels of PWM (Pulse Width Modulation) function which can change the duty in a certain fixed period. The PWM output resolution is 16 bits for each channel.

Serial Interface
This LSI contains two channels of serial interface.

(1) Start-stop synchronous serial interface without FIFO: 1 channel
This serial interface is incorporated in µPLAT-7B.
(2) Start-stop synchronous serial interface with 16-byte FIFO: 1 channel
This is ACE (Asynchronous Communication Element) equivalent in function to 16550A. It has 16-byte FIFO in both sending and receiving.

PIO
This LSI contains two channels 16-bit parallel port.

(1) Input or output can be selected for each bit.
(2) Interrupt can be used for all 16 bits of each channel and interrupt is possible for each channel.
(3) Interrupt mask and interrupt mode (level) can be set for all bits.
(4) Input state immediately after reset.

AD Converter
Successive approximation type AD converter.

(1) 10 bits × 8 channels
(2) Sample hold function
(3) Scan mode and select mode are supported
(4) Interrupt is generated after completion of conversion.
(5) Conversion time: shortest about 5 µs.

DMAC
Two channels of direct memory access controller which transfers data between memory and memory, between I/O and memory and between I/O and I/O.

(1) Number of channels: 2 channels
(2) Channel priority level: Fixed mode
Channel priority level is always fixed (channel 0 > 1).
Roundrobin
Priority level of the channel requested for transfer is kept lowest.
(3) Maximum number of transfers: 65,536 times (64K times)
(4) Data transfer size: Byte (8 bits), half-word (16 bits), word (32 bits)
(5) Bus request system: Cycle steal mode
Bus request signal is asserted for each DMA transfer cycle.
Burst mode
Bus request signal is asserted until all transfers of transfer cycles are complete.
(6) DMA transfer request: Software request
By setting the software transfer request bit inside DMAC, the CPU starts DMA transfer.
External request
DMA transfer is started by external request allocated to each channel.
(7) Interrupt request: Interrupt request is generated in CPU after the end of DMA transfers for the set number of transfer cycles or after occurrence of error.
Interrupt request signal is output separately for each channel.
Interrupt request signal output can be masked for each channel.

External memory controller
Controls access of externally connected devices such as ROM (FLASH), SRAM, SDRAM (EDO DRAM) and IO devices.

(1) ROM (FLASH) access function
Supports 16-bit device
Supports FLASH memory: Byte write (can be written only by IF equivalent to SRAM).
Access timing setting
(2) SRAM access function
Supports 16-bit device
Supports asynchronous SRAM
Access timing setting
(3) DRAM access function
Supports 16-bit device
Supports EDO/SDRAM: Simultaneous connections to EDO-DRAM and SDRAM cannot be made.
Access timing setting
(4) External IO access function
Supports 8-bit/16-bit device
Supports 2 banks independently
Supports external wait input: XWAIT (IO bank 0 only)
Access timing setting (for each bank)

Power Management
HALT and STOP functions are supported as power save functions.

(1) HALT mode
HALT object
CPU, internal RAM, AHB bus control
HALT mode setting: Set by the system control register.
HALT mode cancelling: Reset, interrupt
(2) STOP mode
Stops the clock of entire LSI.
STOP mode setting: Specified by the system control register.
STOP mode cancelling: Reset, external interrupt (other than FIQ)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Conditions	Rating	Unit
Digital power supply voltage (core)	V_{DD_CORE}	GND = AGND = 0 V Ta = 25°C	–0.3 to +3.6	V
Digital power supply voltage (I/O)	V_{DD_IO}		–0.3 to +4.6	
Input voltage	V_I		–0.3 to V_{DD_IO}+0.3	
Output voltage	V_O		–0.3 to V_{DD_IO}+0.3	
Analog power supply voltage	AV_{DD}		–0.3 to V_{DD_IO}+0.3	
Analog reference voltage	V_{REF}		–0.3 to V_{DD_IO}+0.3 and –0.3 to AV_{DD} +0.3	
Analog input voltage	V_{AI}		–0.3 to V_{REF}	
Input current	I_I		–10 to +10	mA
High level output current	I_{OH}		+10	
Low level output current *1	I_{OL}		–20	
Low level output current *2			–30	
Power losses	P_D	Ta = 85°C per package	530	mW
Storage temperature	T_{STG}	—	–50+150	°C

Note

1. All output pins except XA[15:0]
2. XA[15:0]

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Digital power supply voltage (core)	V_{DD_CORE}	$V_{DD\_IO} \geq V_{DD\_CORE}$	2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}		3.0	3.3	3.6	
Analog power supply voltage	AV_{DD}	$A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Analog reference voltage	V_{REF}	$V_{REF} = A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Storage hold voltage	V_{DDH}	f_{OSC} = 0 Hz	2.25	—	3.6	
Operating frequency	f_{OSC}	V_{DD_CORE} = 2.25 to 2.75 V_{DD_IO} = 3.0 to 3.6 *	1	—	33.333	MHz
Ambient temperature	Ta	—	–40	25	+85	°C

Note

Oscillator frequencies between 16 MHz and 33 MHz. Minimum of 2.56 MHz for external SDRAM. Minimum of 6.4 MHz for external EDO DRAM. Minimum of 2 MHz for analog-to-digital converter.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = –40 to +85°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
High level input voltage	V_{IH}	—	2.0	—	V_{DD_IO}+0.3	V
Low level input voltage	V_{IL}		–0.3	—	0.8	
Schmitt input buffer threshold voltage	V_{T+}		—	1.6	2.1	
	V_{T-}		0.7	1.1	—	
	V_{HYS}		0.4	0.5	—	
High level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD}–0.2	—	—	
		I_{OH} = –4 mA	2.4	—	—	
Low level output voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	
Low level output voltage *1		I_{OL} = 4 mA	—	—	0.4	
Low level output voltage *2		I_{OL} = 6 mA	—	—	0.4	
Input leak current *3	I_{IH}/I_{IL}	V_I = 0 V/V_{DD_IO}	–10	—	10	µA
Input leak current *4		V_I = 0 V Pull-up resistance of 50 kΩ	10	66	200	
Output leak current	I_{LO}	V_O = 0 V/V_{DD_IO}	–10	—	10	
Input pin capacitance	C_I	—	—	6	—	pF
Output pin capacitance	C_O	—	—	9	—	
I/O pin capacitance	C_{IO}	—	—	10	—	
Analog reference power supply current	I_{REF}	Analog-to-digital converter operative *5	—	320	650	µA
		Analog-to-digital converter stopped	—	1	2	
Current consumption (STANDBY)	I_{DDS_CORE}	Ta = 25°C *6	—	3	45	µA
	I_{DDS_IO}		—	1	5	
Current consumption (HALT) *7	I_{DDH_CORE}	f_{OSC} = 16 MHz C_L = 50 pF	—	8	15	mA
	I_{DDH_IO}		—	2	5	
Current consumption (RUN)	I_{DD_CORE}		—	15	25	mA
	I_{DD_IO}		—	18	30	

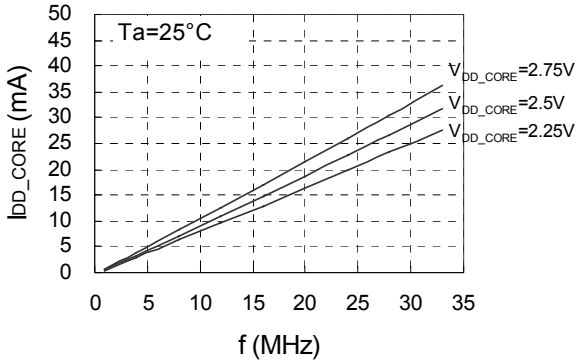
Notes

1. All output pins except XA[15:0]
2. XA[15:0]
3. All input pins except RESET_N
4. RESET_N pin, with 50 kΩ pull-up resistance
5. Analog-Digital Converter operation ratio is 20%
6. V_{DD_IO} or 0 V for input ports; no load for other pins
7. Analog-Digital Converter and DRAM function stop by MODE pin setting

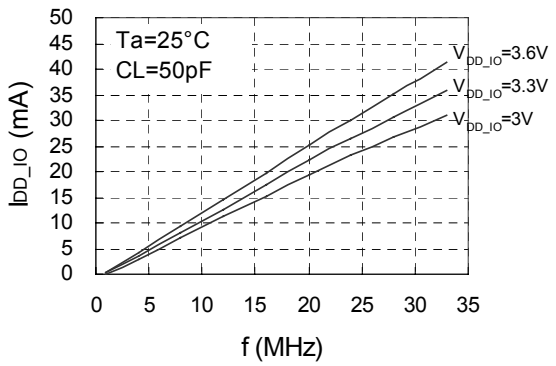
<Power consumption data sample>

Notes: This data is just sampled data. This is not described Maximum/Minimum power consumption.

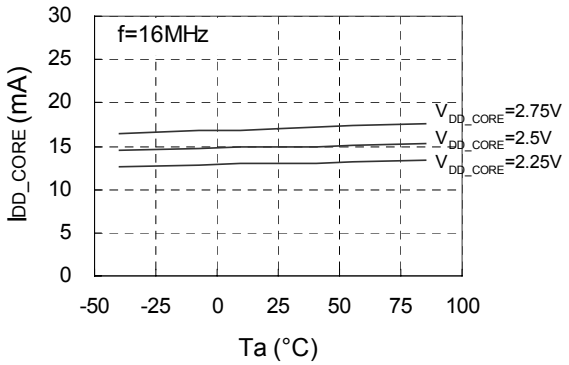
I_{DD_CORE}-f



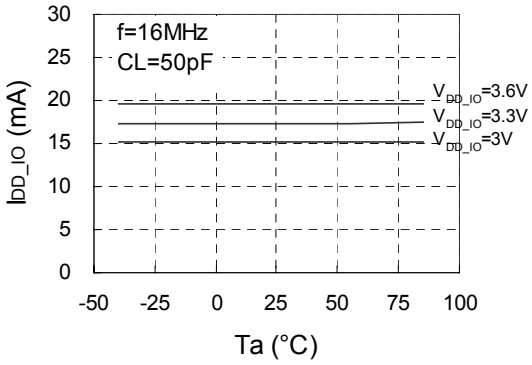
I_{DD_IO}-f



I_{DD_CORE}-Ta



I_{DD_IO}-Ta



AC Characteristics

Clock Timing

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = –40 to +85°C)

Item	Symbol	Condi-tions	Minimum	Typical	Maximum	Unit	Notes
Clock frequency	f_C	—	1	—	33.333	MHz	
Clock cycle time	t_C		30	—	1000	ns	
Clock High level pulse width	t_{CH}		14	—	—		
Clock Low level pulse width	t_{CL}		14	—	—		
Clock Rise time	t_{CR}		—	—	4		
Clock Fall time	t_{CF}		—	—	4		
XSDCLK frequency	f_{SDC}		1	—	33.333	MHz	
XSDCLK cycle time	t_{SDC}		30	—	1000	ns	
XSDCLK High level pulse width	t_{SDCH}		12	—	—		
XSDCLK Low level pulse width	t_{SDCL}		12	—	—		
XSDCLK Rise time	t_{SDCR}		—	—	2		
XSDCLK Fall time	t_{SDCF}		—	—	2		
HCLK frequency	f_{HC}		0.125	—	33.333	MHz	
HCLK cycle time	t_{HC}		30	—	8000	ns	

Item	Symbol	Condi-tions	Minimum	Typical	Maximum	Unit	Notes
RESET_N pulse width 1	t_{RSTW1}	—	20 t_C	—	—	ns	Except for when power is first applied and return from HALT or STANDBY mode
RESET_N pulse width 2	t_{RSTW2}		Oscillation stabilization interval	—	—	—	When power is first applied and return from HALT or STANDBY mode
EFIQ_N pulse width	t_{EFIQW}		2 t_{HC}	—	—	ns	
EXINT pulse width 1	$t_{EXINTW1}$		2 t_{HC}	—	—		Except for STANDBY mode
EXINT pulse width 2	$t_{EXINTW2}$		t_{HC}	—	—		Release from STANDBY mode
DREQCLR0/DREQCLR1 delay 1	t_{DCLRD1}	CL = 50 pF	8 t_{HC} + 9	—	—		
TCOUT0/TCOUT1 delay 1	$t_{TCOUTD1}$		8 t_{HC} + 9	—	—		
DREQCLR0/DREQCLR1 delay 2	t_{DCLRD2}		2 t_{HC} + 9	—	—		
TCOUT0/TCOUT1 delay 2	$t_{TCOUTD2}$		2 t_{HC} + 9	—	—		
DREQ0/DREQ1 hold time	t_{DREQH}	—	t_{HC}	—	—		

Control signal timing

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = –40 to +85°C)

SDRAM							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
XSDCS_N delay (SDRAM)	t_{SDCSD}	CL = 50 pF	$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11	ns	The DRPC register specifies the SDRAM access parameters tRAS, tRCD, tRP. For further details, see the following Table.
XSDCKE delay (SDRAM)	t_{SDCKED}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11		
XDQM[0]/XDQM[1] delay (SDRAM)	t_{DQMD}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11.5		n_{SD1} = tRCD
XRAS_N delay (SDRAM)	t_{SDRASD}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11		n_{SD2} = tRAS
XCAS_N delay (SDRAM)	t_{SDCASD}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11		n_{SD3} = tRP
RASCAS minimum delay (SDRAM)	t_{SDRCD}	—	$n_{SD1}t_{SDC}$	—	—		
RAS active time (SDRAM)	t_{SDRAS}		$n_{SD2}t_{SDC}$	—	—		
RAS precharge time (SDRAM)	t_{SDRP}		$n_{SD3}t_{SDC}$	—	—		
XWE_N delay (SDRAM)	t_{SDWED}	CL = 50 pF	$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 10		
XD[15:0] input setup time (SDRAM)	t_{SDXDIS}	—	10	—	—		
XD[15:0] input hold time (SDRAM)	t_{SDXDIH}		0	—	—		
XD[15:0] output delay (SDRAM)	t_{SDXAD}	CL = 50 pF	$0.5t_{SDC}$	—	$0.5t_{SDC}$ + 11		
XD[15:0] output delay (SDRAM)	t_{SDXDOD}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 10		
XD[15:0] output hold time (SDRAM)	t_{SDXDOH}		$0.5t_{SDC}$ − 1	—	$0.5t_{SDC}$ + 11		
XD[15:0] output enable time (SDRAM)	t_{SDXDOE}		$0.5t_{SDC}$	—	—		
XD[15:0] output disable time (SDRAM)	$t_{SDXDODE}$		$0.5t_{SDC}$ + 4	—	—		

EDODRAM							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
RASCAS delay (EDO DRAM)	t_{EDRCD}	—	$n_{ED1}\ t_{HC} - 1.5$	—	$n_{ED1}\ t_{HC} + 6$	ns	The DRPC register specifies the EDO DRAM access parameters tRAS, tRAH, tCAC, tCAS, tRCD, tRP. For further details, see the following Table.
CAS pulse width (EDO DRAM)	t_{EDCAS}	CL = 50 pF	$n_{ED2}\ t_{HC} - 10$	—	$n_{ED2}\ t_{HC} + 1$		
RAS pulse width (EDO DRAM)	t_{EDRAS}		$n_{ED8}\ t_{HC} - 8.5$	—	$n_{ED8}\ t_{HC} + 2$		
RAS precharge time (EDO DRAM)	t_{EDRP}	—	$n_{ED3}\ t_{HC} - 2$	—	—		
CAS precharge time (EDO DRAM)	t_{EDCP}		$n_{ED4}\ t_{HC} - 1$	—	—		n_{ED1} = tRCD
XRAS_N delay (EDO DRAM)	t_{EDRASD}	CL = 50 pF	$t_{HC} - 6.5$	—	$t_{HC} + 6$		n_{ED2} = tCAS
XOE_N delay 1 (EDO DRAM)	t_{EDOED1}		$n_{ED5}\ t_{HC} - 4.5$	—	$n_{ED5}\ t_{HC} + 0.5$		n_{ED3} = tRP
XOE_N delay 2 (EDO DRAM)	t_{EDOED2}		$n_{ED4}\ t_{HC} - 4.5$	—	$n_{ED4}\ t_{HC} + 1$		n_{ED4} = tCAC + 1 − tCAS
XWE_N delay 1 (EDO DRAM)	t_{EDWED1}		$n_{ED5}\ t_{HC} - 3.5$	—	$n_{ED5}\ t_{HC} + 2$		n_{ED5} = tRAH
XWE_N delay 2 (EDO DRAM)	t_{EDWED2}		$n_{ED4}\ t_{HC} - 2$	—	$n_{ED4}\ t_{HC} + 2.5$		n_{ED6} = tRCD − tRAH
Row address hold time (EDO DRAM)	t_{EDRAH}		$n_{ED5}\ t_{HC} - 6$	—	$n_{ED5}\ t_{HC} + 6.5$		n_{ED7} = tCAC + 1
Column address delay (EDO DRAM)	t_{EDCAD}		$n_{ED6}\ t_{HC} - 6$	—	$n_{ED6}\ t_{HC} + 7$		n_{ED8} = tRCD + N(tCAC + 1)
Column address hold time (EDO DRAM)	t_{EDCAH}		$n_{ED2}\ t_{HC} - 7.5$	—	$n_{ED2}\ t_{HC} + 6$		N = Data Size/Bus Width
XD[15:0] sampling timing delay (EDO DRAM)	$t_{EDXDSMPLD}$	—	$n_{ED7}\ t_{HC}$	—	$n_{ED7}\ t_{HC}$		n_{ED9} = −(tRAH + 1)
XD[15:0] input setup time (EDO DRAM)	t_{EDXDIS}		21.5	—	—		
XD[15:0] input hold time (EDO DRAM)	t_{EDXDIH}		0	—	—		
XD[15:0] output delay 1 (EDO DRAM)	$t_{EDXDOD1}$	CL = 50 pF	−4	—	8		
XD[15:0] output delay 2 (EDO DRAM)	$t_{EDXDOD2}$		−3	—	9.5		
XD[15:0] output hold time (EDO DRAM)	t_{EDXDOH}		$t_{HC} - 8$	—	$t_{HC} + 7$		
XD[15:0] output enable time (EDO DRAM)	t_{EDXDOE}		$n_{ED9}\ t_{HC} - 2$	—	—		
XD[15:0] output disable time (EDO DRAM)	$t_{EDXDODE}$		$n_{ED7}\ t_{HC} - 2$	—	—		

■ DRPC Register Settings and Parameters tRAS, tRAH, tCAC, tCAS, tRCD, and tRP

The DRAMSPEC bits specify the combination of DRAM access parameters.

DRAMSPEC[3:0] setting for EDO DRAM		tRAH tCAS	tRCD	tCAC tOEZ	tRP		
	0000	1	2	1	1	High-speed DRAM	Low frequency
	0001	1	2	1	2	↑	↑
	0010	1	3	1	2	|	|
	0011	1	3	1	3	|	|
	0100	1	3	2	3	|	|
	0101	1	4	2	4	|	|
	0110	1	5	2	5	|	|
	0111	2	4	2	4	|	|
	1000	2	5	2	5	|	|
	1001	2	6	2	6	↓	↓
	1010	3	8	3	7	Low-speed DRAM	High frequency
	1011	(reserved)				Operation is not guaranteed for a setting labeled “reserved.”	
	|	|				|	
	1111	(reserved)				Operation is not guaranteed for a setting labeled “reserved.”	

SRAM/ROM							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
XROMCS_N/XRAMCS_N access time (SRAM/ROM)	t_{CS}	CL = 50 pF	$(n_{R1} + n_{R3})$ t_{HC} − 9	—	$(n_{R1} + n_{R3})$ t_{HC} + 4	ns	The ROMAC and RAMAC registers specify the OE/WE pulse width and read off time for ROM and SRAM access, respectively. For further details, see the following Tables.
XA[23:0] access time (SRAM/ROM)	t_{XACC}		$(n_{R1} + n_{R3})$ t_{HC} − 9.5	—	$(n_{R1} + n_{R3})$ t_{HC} + 1.5		
XBS_N[1:0] access time (SRAM/ROM)	t_{BS}		$(n_{R1} + n_{R3})$ t_{HC} − 9	—	$(n_{R1} + n_{R3})$ t_{HC} + 3		
XOE_N delay (SRAM/ROM)	t_{OED}		n_{R1} t_{HC} − 6.5	—	n_{R1} t_{HC} + 7		n_{R1} = 0 (CPU Access)
XWE_N delay (SRAM/ROM)	t_{WED}		n_{R2} Tc – 10.5	—	n_{R2} t_{HC} + 0.5		n_{R1} = 1 (DMA Access))
XBWE_N[1:0] delay (SRAM/ROM)	t_{WELHD}		n_{R2} t_{HC} – 11	—	n_{R2} t_{HC}		n_{R2} = 0.5 (CPU Access)
XBWE_N[1:0] hold time (SRAM/ROM)	t_{WELHH}		−2	—	1.5		n_{R2} = 1.5 (DMA Access)
XOE_N, XWE_N pulse width (SRAM/ROM)	$t_{OE/WEW}$		n_{R3} t_{HC} – 8	—	n_{R3} t_{HC} + 2		n_{R3} = OE/WE pulse width
XOE_N pulse width 2 (SRAM/ROM)	t_{OEW2}		$n_{R4}n_{R3}$ t_{HC} – 8	—	$n_{R4}n_{R3}$ t_{HC} + 2		n_{R4} = 2 (16 bit bus width & word access)
XBS_N[1:0] delay (SRAM/ROM)	t_{BSBD}		−4	—	3		
XBS_N[1:0] output hold time 1 (SRAM/ROM)	t_{BSBH1}		−2	—	—		
XBS_N[1:0] output hold time 2 (SRAM/ROM)	t_{BSBH2}		0.5 t_{HC} – 2	—	—		
XA[23:0] delay (SRAM/ROM)	t_{XAD}		−7	—	7.5		
XA[23:0] output hold time 1 (SRAM/ROM)	t_{XAH1}		−1.5	—	—		
XA[23:0] output hold time 2 (SRAM/ROM)	t_{XAH2}		0.5 t_{HC} + 1	—	—		
XD[15:0] input setup time (SRAM/ROM)	t_{XDIS}	—	18	—	—		
XD[15:0] input hold time (SRAM/ROM)	t_{XDIH}		0	—	—		
XD[15:0] output delay1 (SRAM/ROM)	t_{XDOD1}	CL = 50 pF	−7	—	9.5		
XD[15:0] output delay 2 (SRAM/ROM)	t_{XDOD2}		−6.5	—	8.5		
XD[15:0] output delay3 (SRAM/ROM)	t_{XDOD3}		−7.5	—	7		

SRAM/ROM (continued)							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
XD[15:0] output Enable time1 (SRAM/ROM)	t_{XDOE1}		0	—	—		
XD[15:0] output Enable time2 (SRAM/ROM)	t_{XDOE2}		−2	—	—		
XD[15:0] output Enable time3 (SRAM/ROM)	t_{XDOE3}		−1	—	—		
XD[15:0] output Disable time1 (SRAM/ROM)	t_{XDODE1}	CL = 50 pF	−5	—	—		
XD[15:0] output Disable time2 (SRAM/ROM)	t_{XDODE2}		−5	—	—		
XD[15:0] output Disable time3 (SRAM/ROM)	t_{XDODE3}		−6	—	—		
XD[15:0] output hold time (SRAM/ROM)	t_{XDOH}		0.5 t_{HC} – 0.5	—	—		
XROMCS_N, XRAMCS_N output hold time 1 (SRAM/ROM)	t_{CSH1}		−3.5	—	—		
XROMCS_N, XRAMCS_N Output hold time 2 (SRAM/ROM)	t_{CSH2}		0.5 t_{HC} − 2	—	—		

■ ROMAC Register Settings for Timing Parameters OE/WE Pulse Width and Read Off Time

ROMTYPE[2:0]: Timing parameter combination

ROMTYPE[2:0]	OE/WE pulse width	Read off time	Notes
000	1	0	
001	2	0	
010	3	2	
011	4	2	
100, 101, 110	—	—	Operation is not guaranteed
111	8	4	

■ RAMAC register Settings for Timing Parameters OE/WE Pulse Width and Read Off Time

RAMTYPE[2:0]: Timing parameter combination

RAMTYPE[2:0]	OE/WE pulse width	Read off time	Notes
000	1	0	
001	2	0	
010	3	2	
011	4	2	
100, 101, 110	—	—	Operation is not guaranteed
111	8	4	

IO0/IO1							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
XIOCS_N[0]/XIOCS_N[1] access time (external I/O banks 0 and 1)	t_{XIOCS}	—	n_{IO3} t_{HC} – 7.5	—	n_{IO3} t_{HC} + 2.5	ns	The IO0AC and IO1AC registers specify the OE/WE pulse width and read off time for accessing external I/O banks 0 and 1, respectively. For further details, see the following Table. n_{IO1} = (Address Setup) + (OE/WE Pulse width) n_{IO2} = (Address Setup) + 1 + (OE/WE Pulse width) n_{IO3} = (Address Setup) n_{IO4} = (Address Setup) + 1 N_{IO5} = (OE/WE pulse width)
XA[23:0] access time (external I/O banks 0 and 1)	$t_{XIOXACC}$		n_{IO3} t_{HC} – 10	—	n_{IO3} t_{HC} + 2		
XBS_N[1:0] access time (external I/O banks 0 and 1)	t_{XIOBS}		n_{IO3} t_{HC} – 8	—	n_{IO3} t_{HC} + 2		
XWR delay (external I/O banks 0 and 1)	$t_{XIOXWRD}$	CL = 50 pF	−6.5	—	3.5		
XWAIT sampling timing delay 1 (external I/O banks 0 and 1)	$t_{XIOXWAITD1}$	—	n_{IO1} t_{HC}	—	n_{IO1} t_{HC}		
XWAIT sampling timing delay 2 (external I/O banks 0 and 1)	$t_{XIOXWAITD2}$		n_{IO2} t_{HC}	—	n_{IO2} t_{HC}		
XWAIT setup time (external I/O banks 0 and 1)	$t_{XIOXWAITS}$		21	—	—		
XWAIT hold time (external I/O banks 0 and 1)	$t_{XIOXWAITH}$		0	—	—		
XOE_N delay (external I/O banks 0 and 1)	t_{XIOOED}	CL = 50 pF	n_{IO3} t_{HC} – 7.5	—	n_{IO3} t_{HC} + 4.5		
XWE_N delay (external I/O banks 0 and 1)	t_{XIOWED}		n_{IO4} t_{HC} – 7.5	—	n_{IO4} t_{HC} + 3.5		
XBWE_N[1:0] delay (external I/O banks 0 and 1)	$t_{XIOWELHD}$		n_{IO4} t_{HC} – 8.5	—	n_{IO4} t_{HC} +2.5		
XOE_N, XWE_N pulse width (external I/O banks 0 and 1)	$t_{XIOE/WEW}$		n_{IO5} t_{HC} – 8	—	n_{IO5} t_{HC} + 2		
XBWE_N[1:0] hold time (external I/O banks 0 and 1)	$t_{XIOWELHH}$		−2		1.5		
XBS_N[1:0] delay (external I/O banks 0 and 1)	t_{XIOSBD}		−2	—	2.5		
XBS_N[1:0] output hold time (external I/O banks 0 and 1)	t_{XIOSBH}		t_{HC} – 2	—	—		
XA[23:0] delay (external I/O banks 0 and 1)	t_{XIOXAD}		−4	—	7.5		
XA[23:0] output hold time 1 (external I/O banks 0 and 1)	$t_{XIOXAH1}$		−2	—	—		
XA[23:0] output hold time 2 (external I/O banks 0 and 1)	$t_{XIOXAH2}$		t_{HC} – 0.5	—	—		
XD[15:0] input setup time (external I/O banks 0 and 1)	t_{XIODIS}	—	16	—	—		
XD[15:0] input hold time (external I/O banks 0 and 1)	t_{XIODIH}		0	—	—		

IO0/IO1 (continued)							
Item	**Symbol**	**Condi-tions**	**Minimum**	**Typical**	**Maximum**	**Unit**	**Notes**
XD[15:0] output delay 1 (external I/O banks 0 and 1)	$t_{XIODOD1}$	CL = 50 pF	t_{HC} – 3	—	t_{HC} + 9.5		
XD[15:0] output delay 2 (external I/O banks 0 and 1)	$t_{XIODOD2}$		t_{HC} – 3	—	t_{HC} + 9		
XD[15:0] output delay 3 (external I/O banks 0 and 1)	$t_{XIODOD3}$		t_{HC} – 7.5	—	t_{HC} + 7		
XD[15:0] output Enable time 1 (external I/O banks 0 and 1)	$t_{XIODOE1}$		t_{HC}	—	—		
XD[15:0] output Enable time 2 (external I/O banks 0 and 1)	$t_{XIODOE2}$		t_{HC} − 1	—	—		
XD[15:0] output Enable time 3 (external I/O banks 0 and 1)	$t_{XIODOE3}$		t_{HC}	—	—		
XD[15:0] output Disable time 1 (external I/O banks 0 and 1)	$t_{XIODODE1}$	CL = 50 pF	t_{HC} − 2	—	—		
XD[15:0] output Disable time 2 (external I/O banks 0 and 1)	$t_{XIODODE2}$		−3	—	—		
XD[15:0] output Disable time 3 (external I/O banks 0 and 1)	$t_{XIODODE3}$		−1	—	—		
XD[15:0] output hold time (external I/O banks 0 and 1)	t_{XIODOH}		t_{HC} – 1.5	—	—		
XIOCS_N[1:0] output hold time (external I/O banks 0 and 1)	t_{XIOCSH}		t_{HC} − 3	—	t_{HC} – 1.5		

■ IO0AC/IO1AC Register Settings and Parameters Address Setup, OE/WE Pulse Width, and Read Off Time

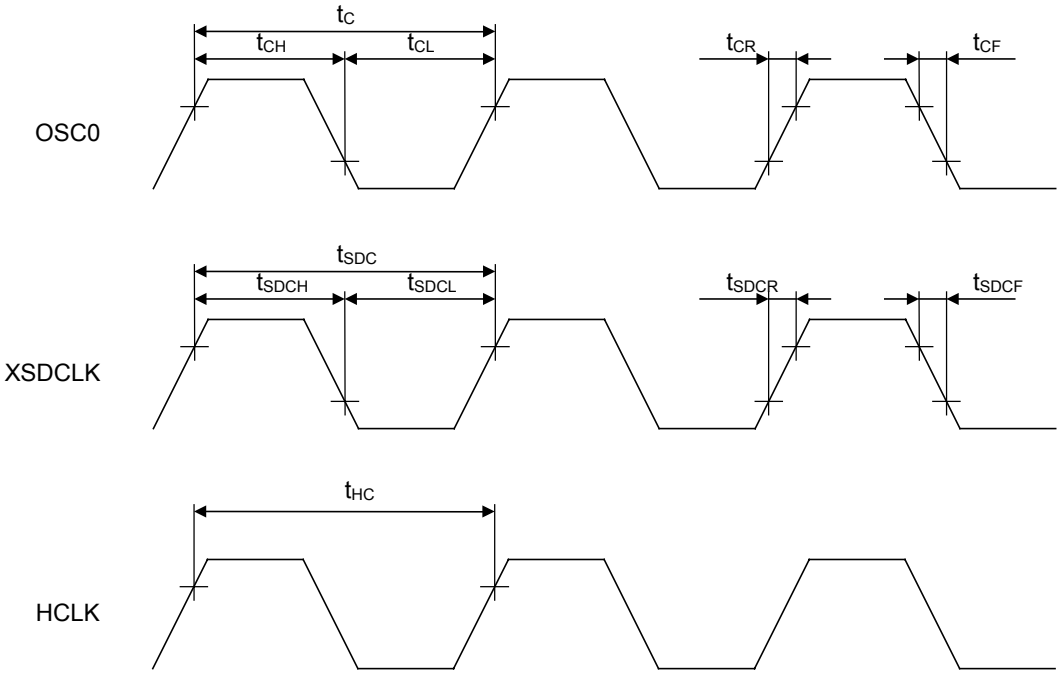
IOTYPE[2:0]: Timing parameter combination

IOTYPE[2:0]	AS	R/W	OF	Notes
000	1	1	1	
001	1	4	3	
010	—	—	—	Operation is not guaranteed
011	2	8	5	
100	2	12	7	
101	2	16	8	
110	—	—	—	Operation is not guaranteed
111	4	24	11	

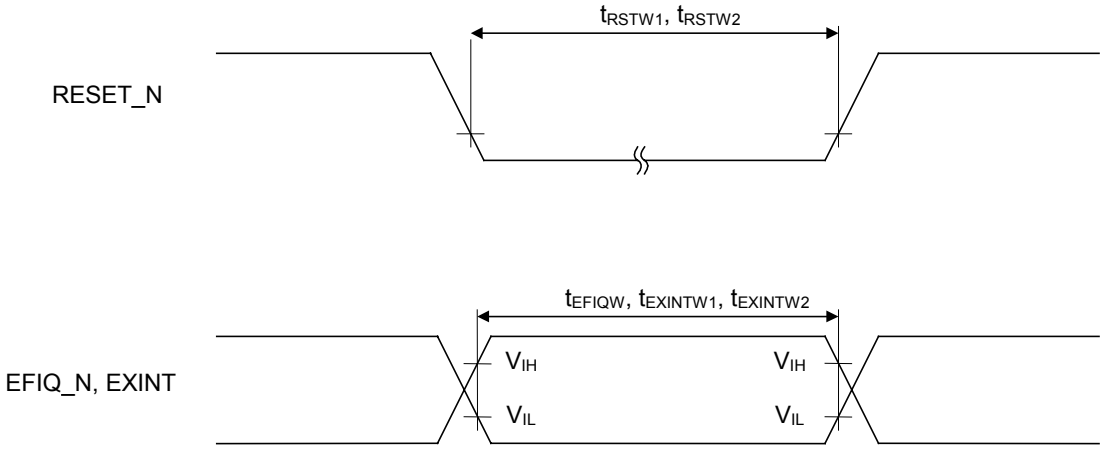
AS = address setup; R/W = OE/WE pulse width; OF = read off time

TIMING DIAGRAMS

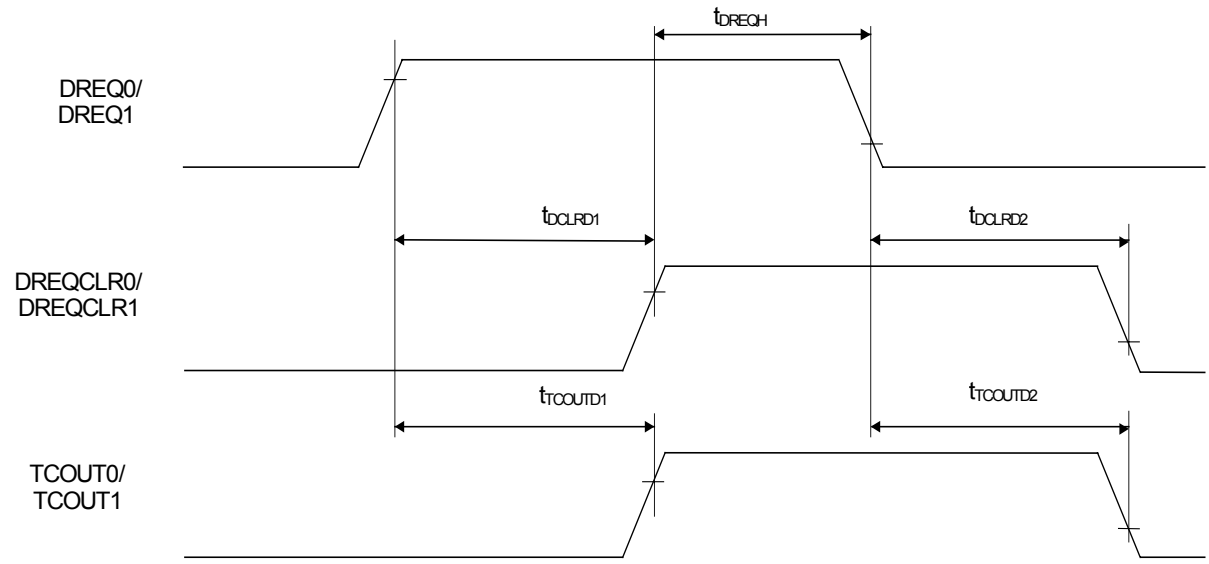
Clock Timing



Control Signal Timing

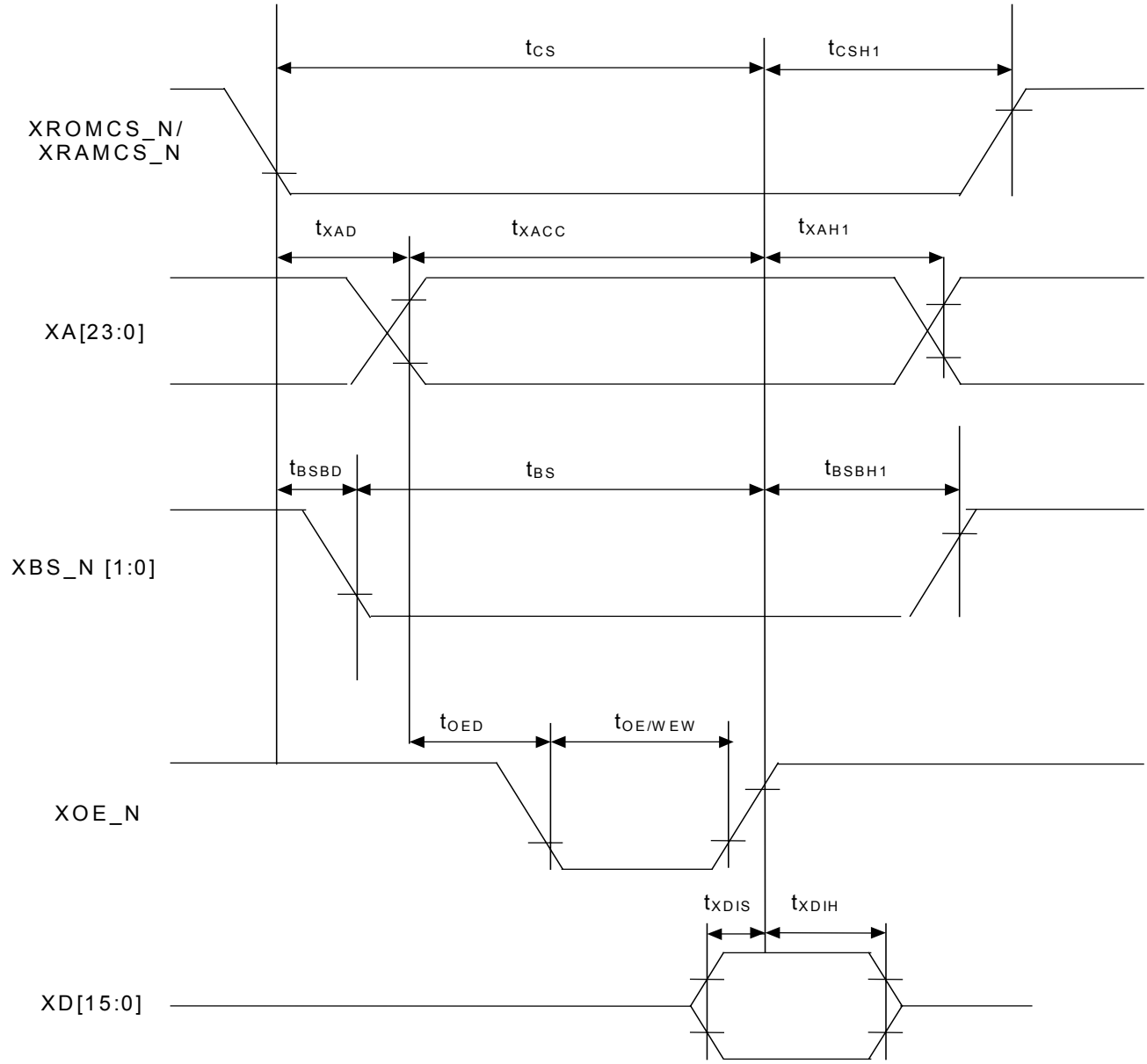


DMA Timing

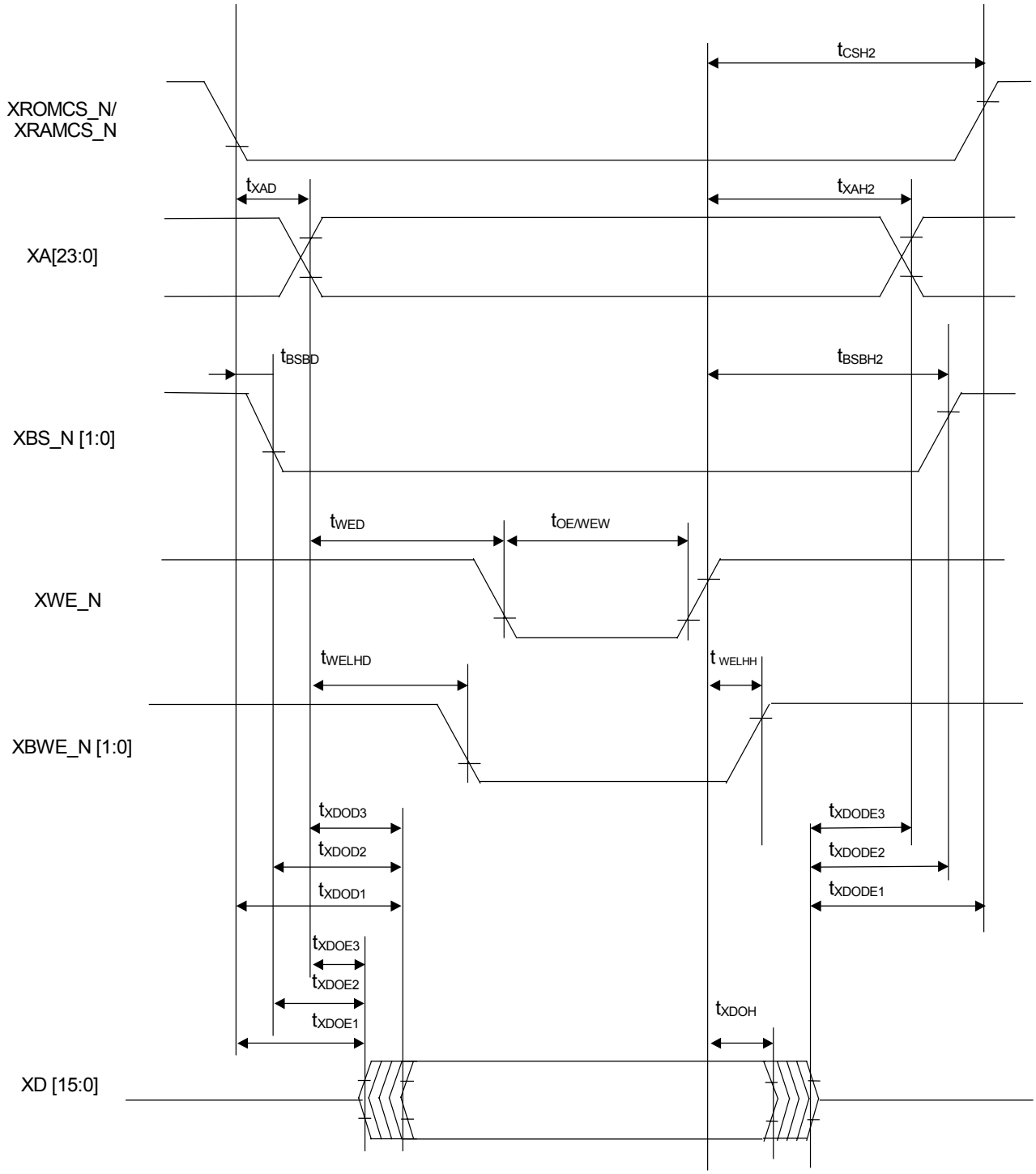

tDREQH
DREQ0/
DREQ1
tDCLRD1
tDCLRD2
DREQCLR0/
DREQCLR1
tTCOUTD1
tTCOUTD2
TCOUT0/
TCOUT1

External Bus Timing

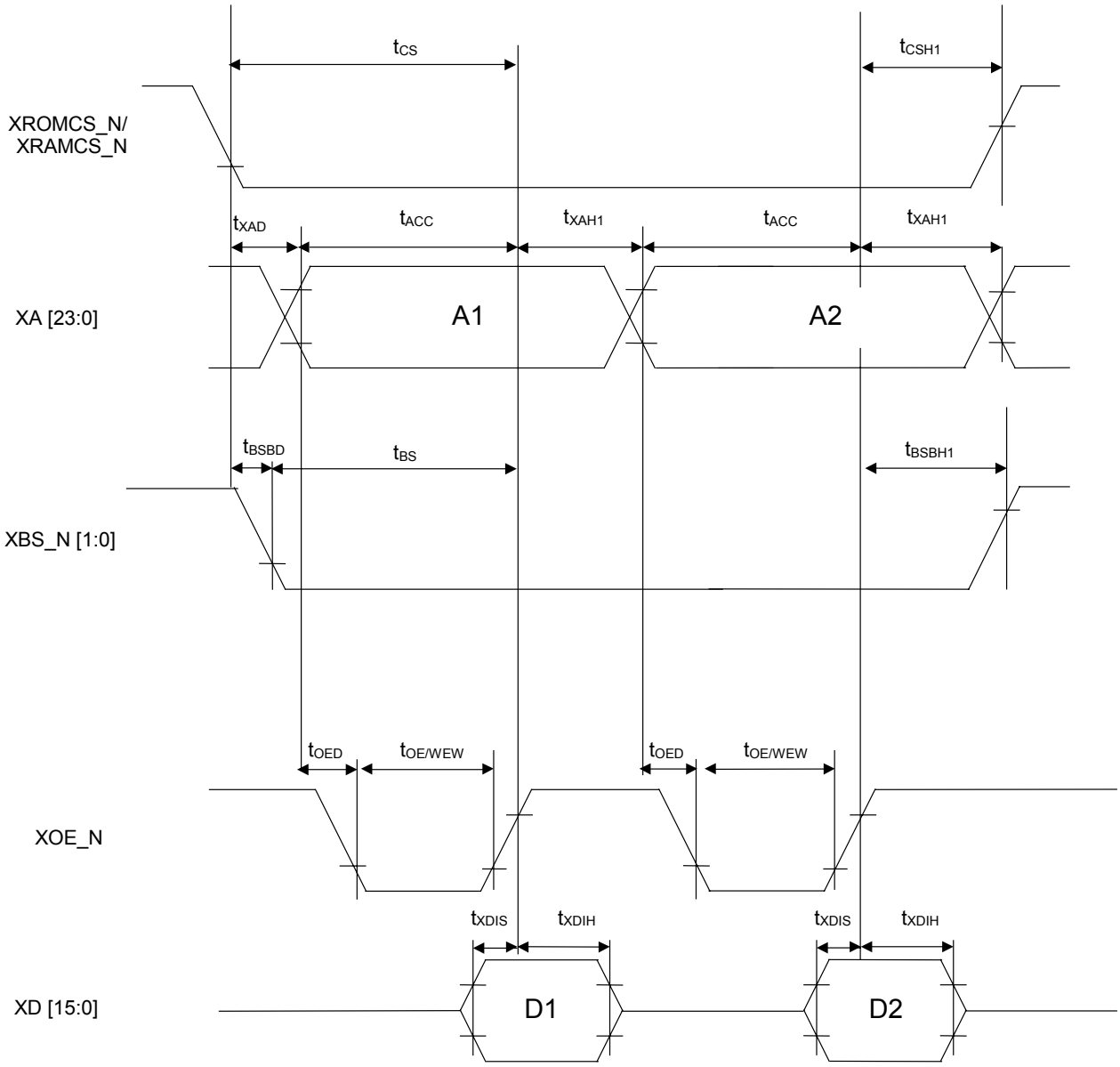
External ROM/RAM Read Cycle
(Bus Width 16 bit External ROM/RAM Byte/Half Word Access)



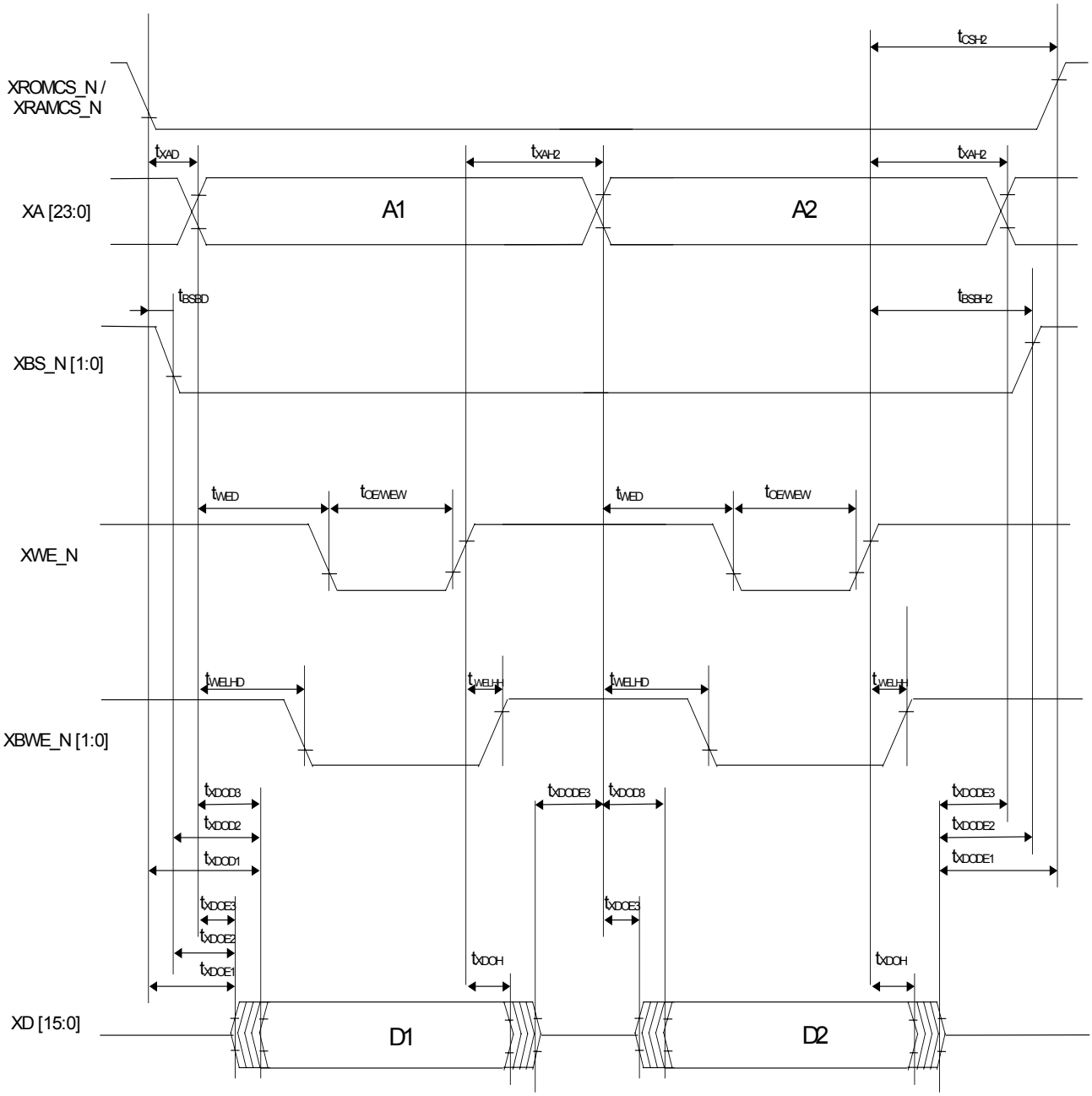
External ROM/RAM Write Cycle
(Bus Width16 bit External ROM/RAM Byte/Half Word Access)



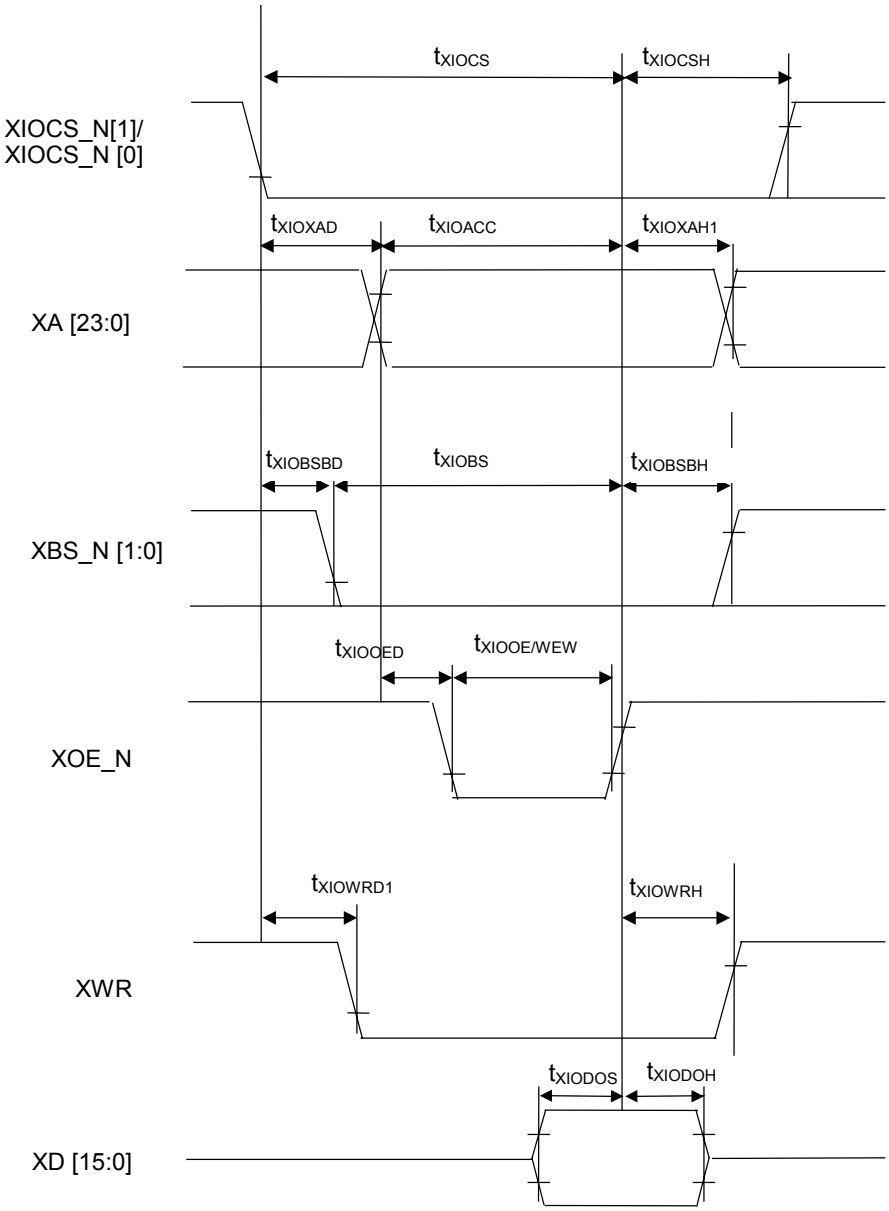
External ROM/RAM Read Cycle
(Bus Width16 bit External ROM/RAM Word Access)



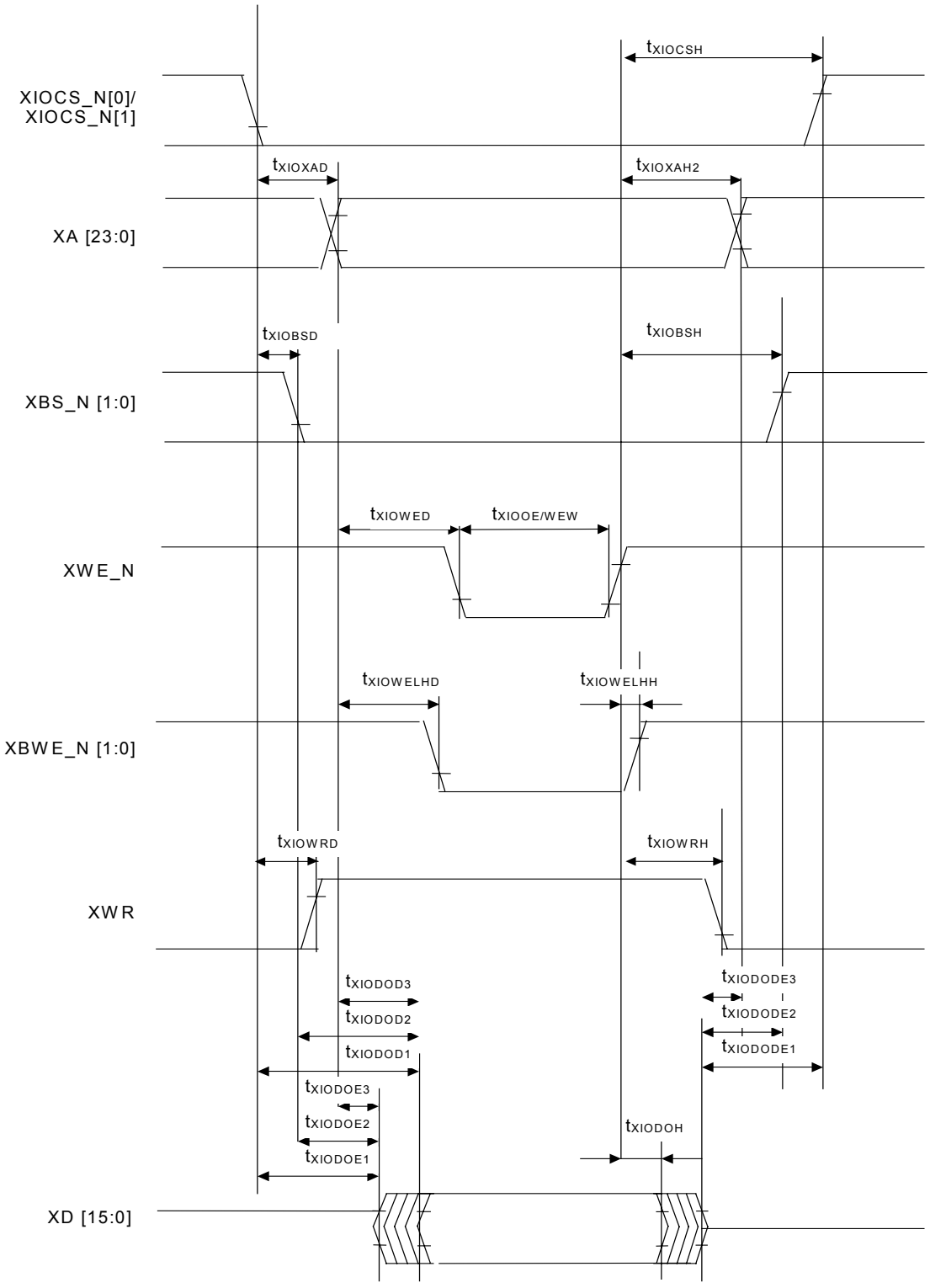
External ROM/RAM Write Cycle
(Bus Width 16 bit External ROM/RAM Word Access)



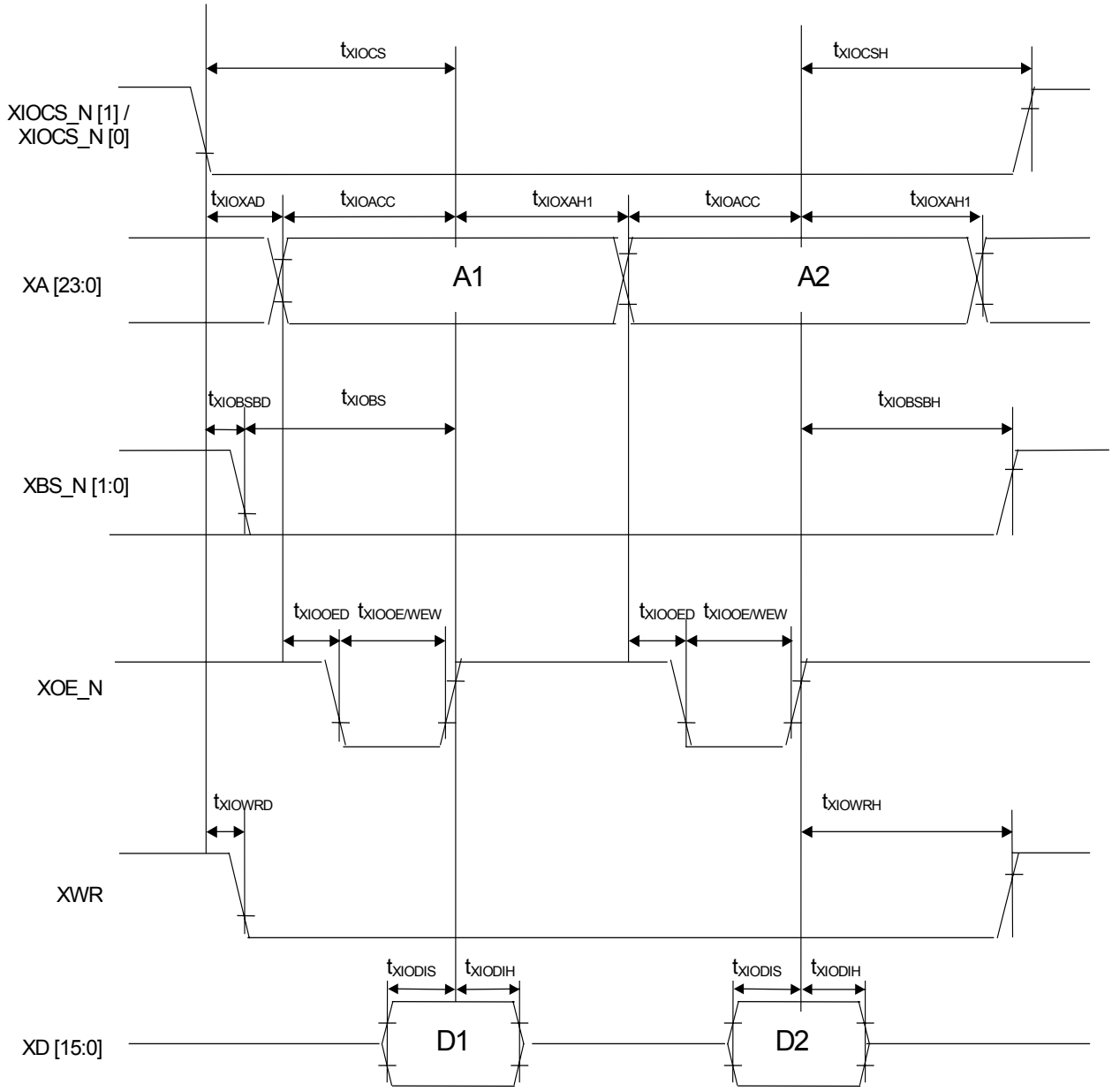
External I/O Banks 0 and 1 Read Cycle
(Bus Width 16 bit External I/O Banks 0 and 1 Byte/Half Word Access)



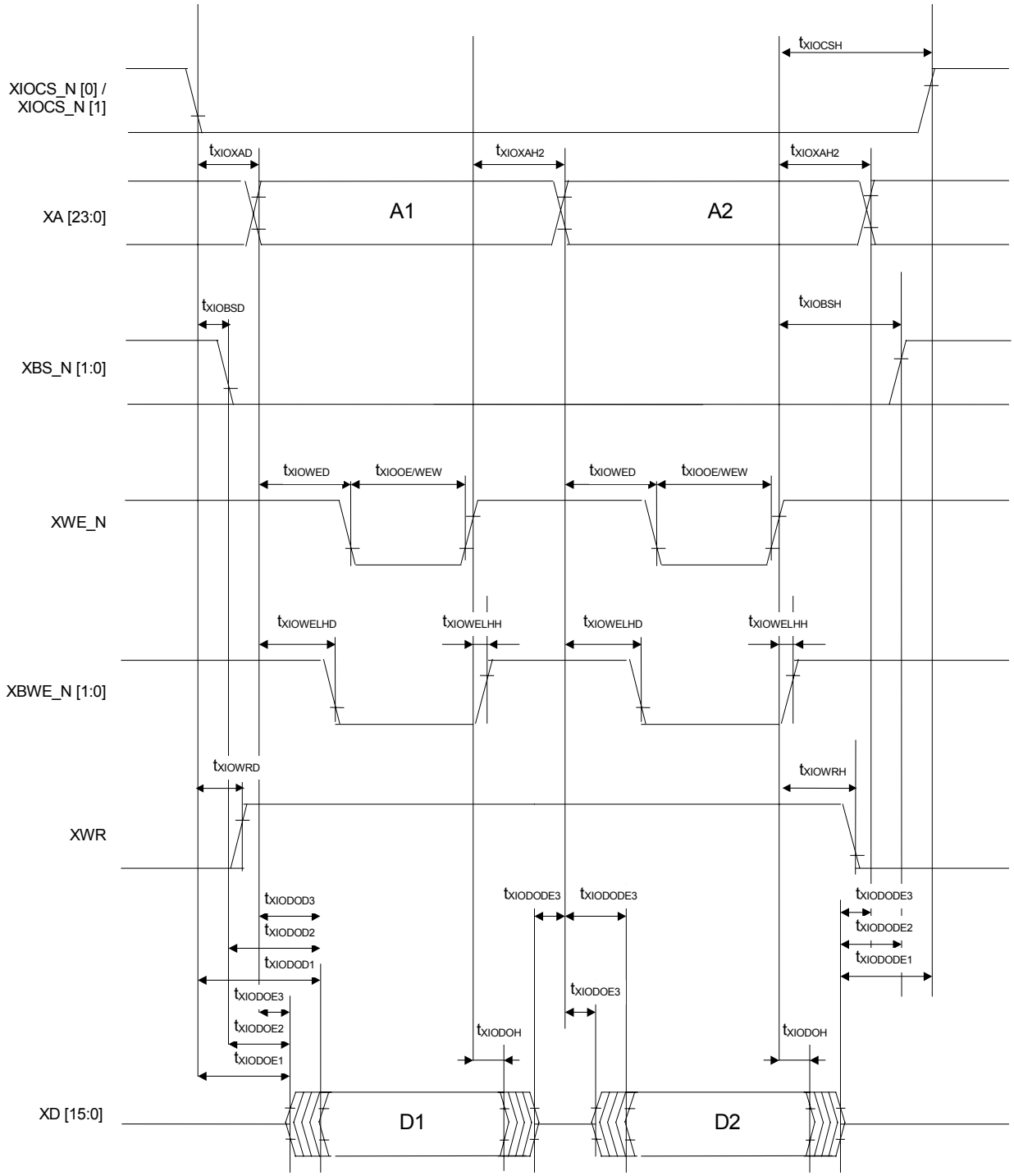
External I/O Banks 0 and 1 Write Cycle
(Bus Width 16 bit External I/O Banks 0 and 1 Byte/Half Word Access)



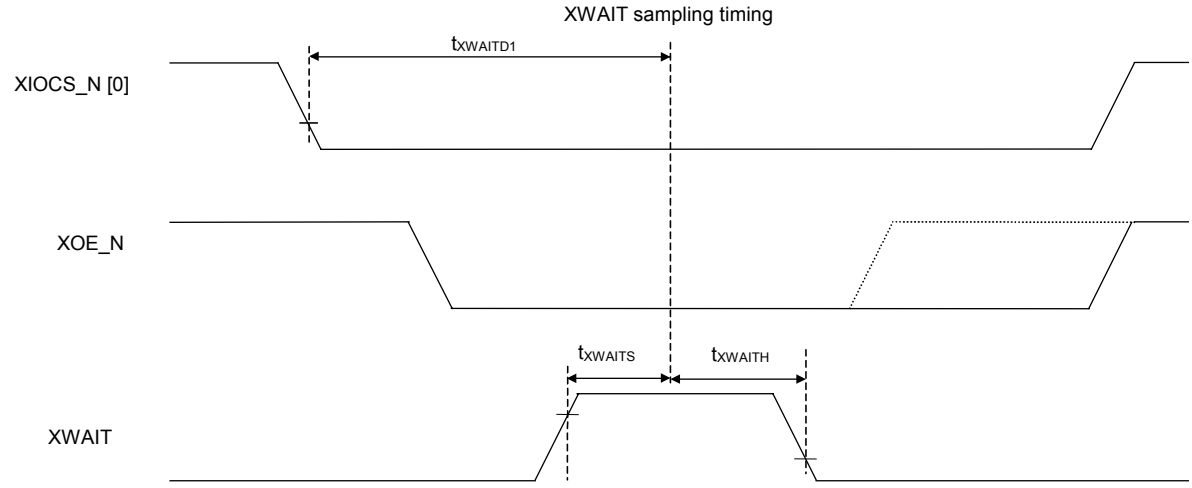
External I/O Banks 0 and 1 Read Cycle
(Bus Width 16 bit External I/O Banks 0 and 1 Word Access/
Bus Width 8 bit External I/O Banks 0 and 1 Half Word Access)



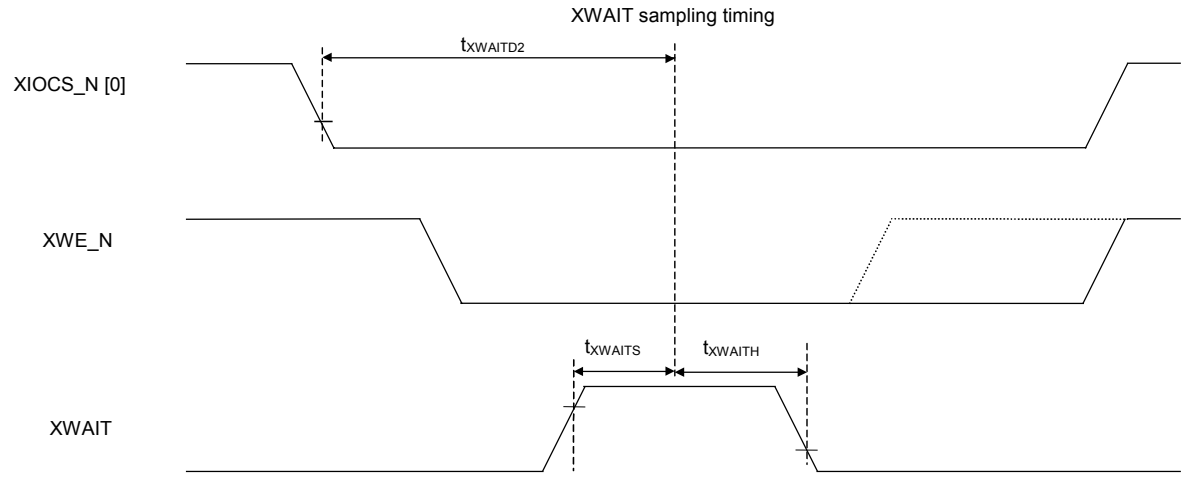
External I/O Banks 0 and 1 Write Cycle
(Bus Width 16 bit External I/O Banks 0 and 1 Word Access/
Bus Width 8 bit External I/O Banks 0 and 1 Half Word Access)



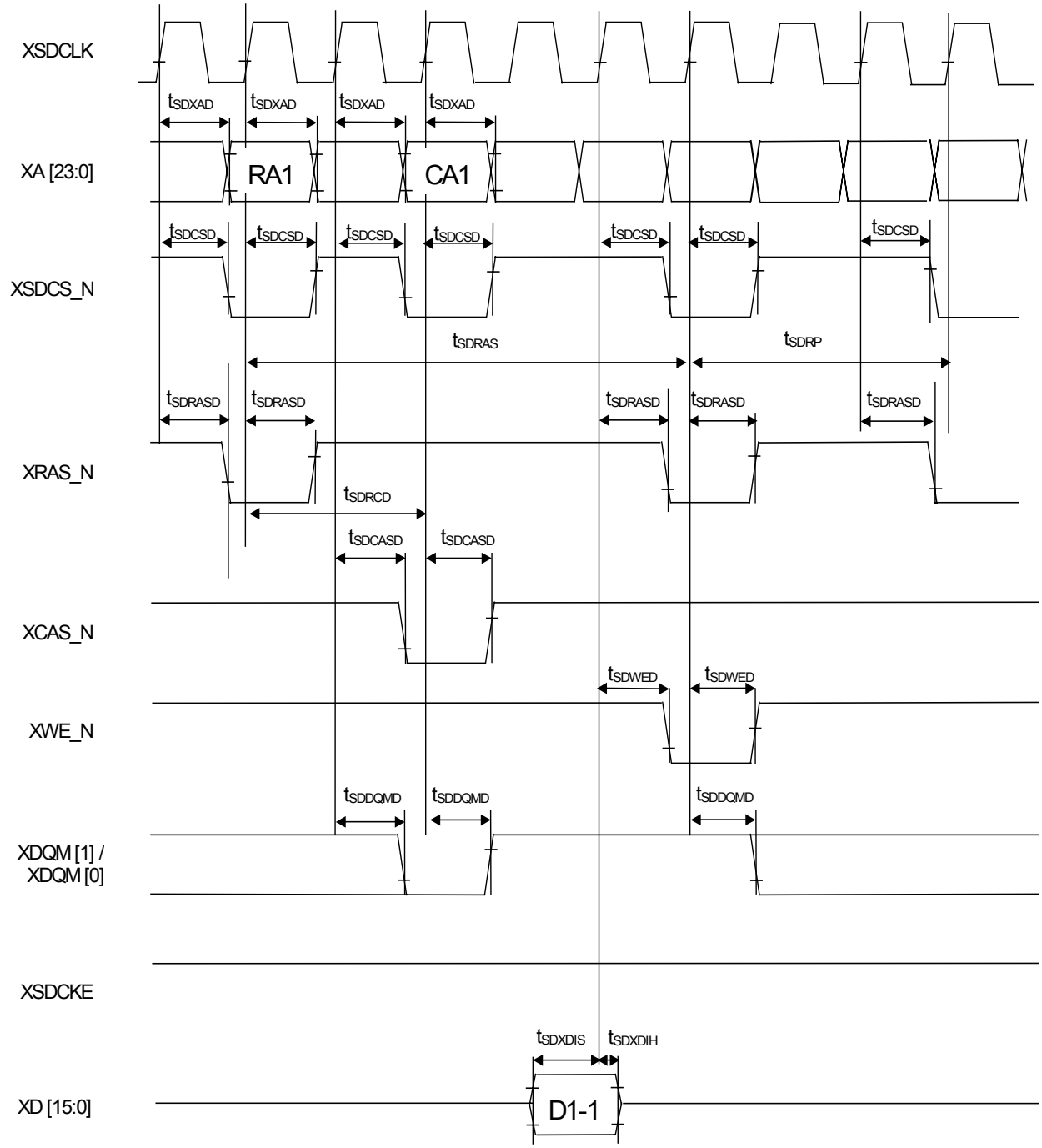
XWAIT Signal Input Timing



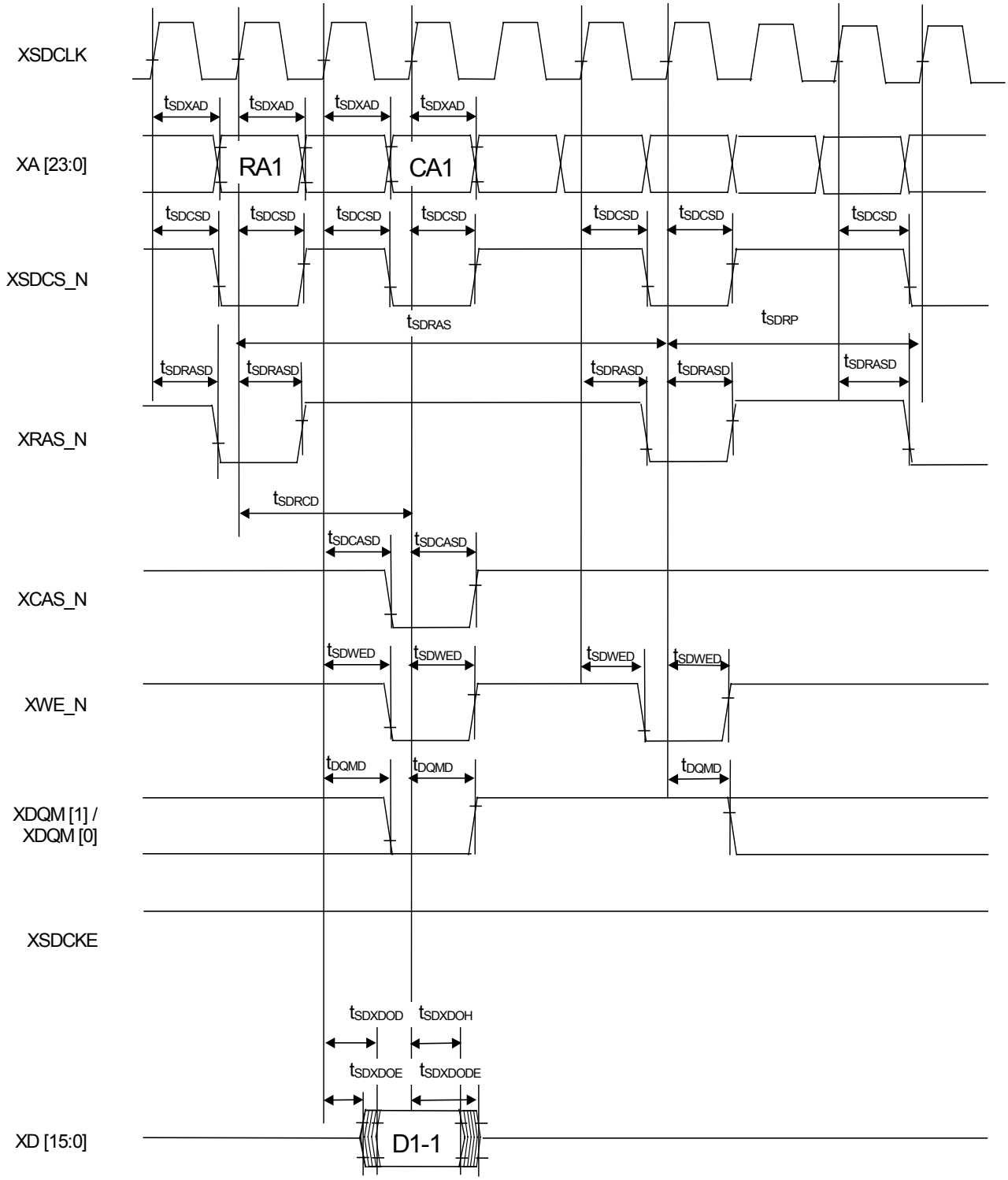
XWAIT Signal Input Timing



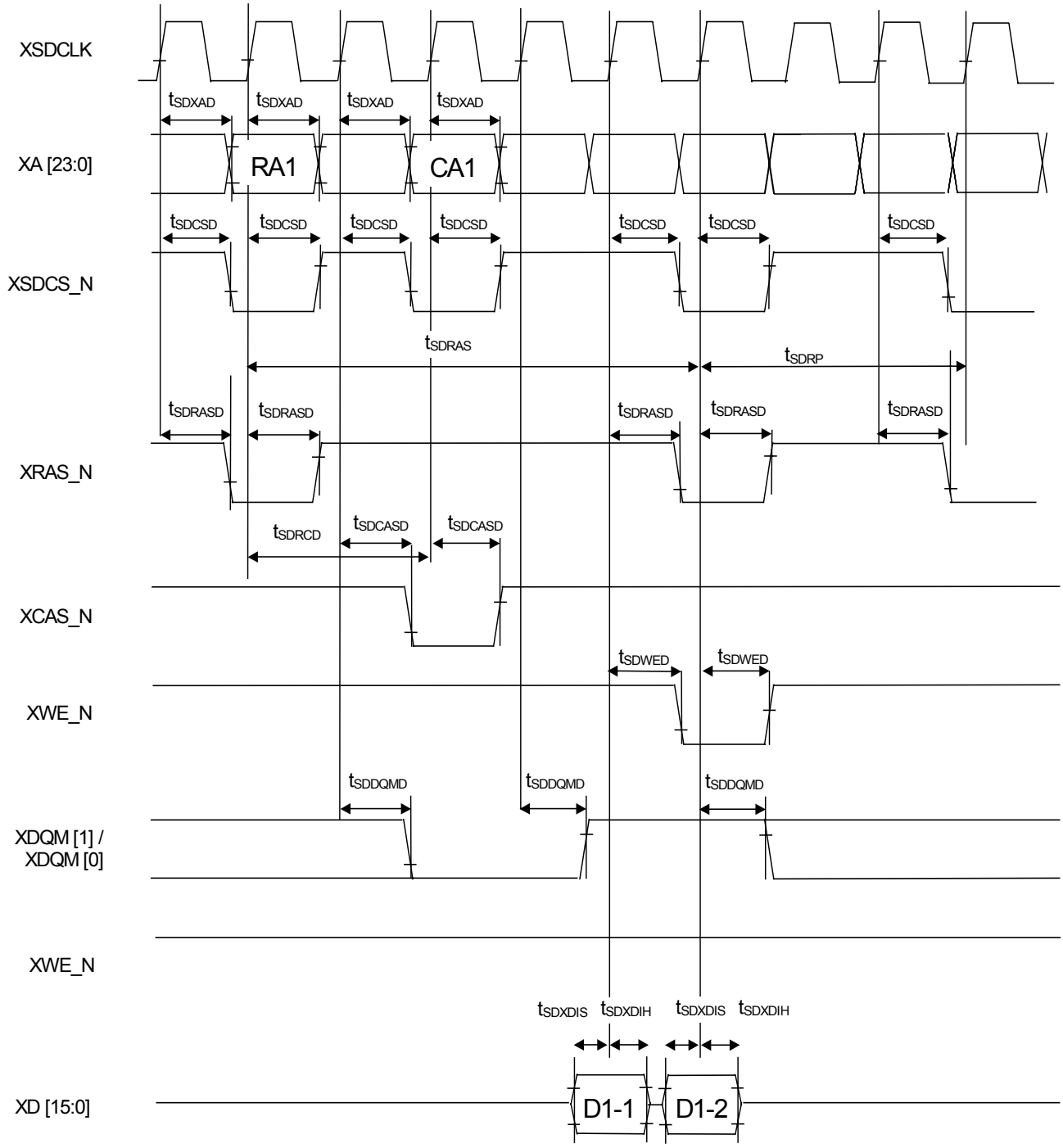
SDRAM Read Cycle
(Bus Width 16 bit SDRAM Byte/Half Word Access)



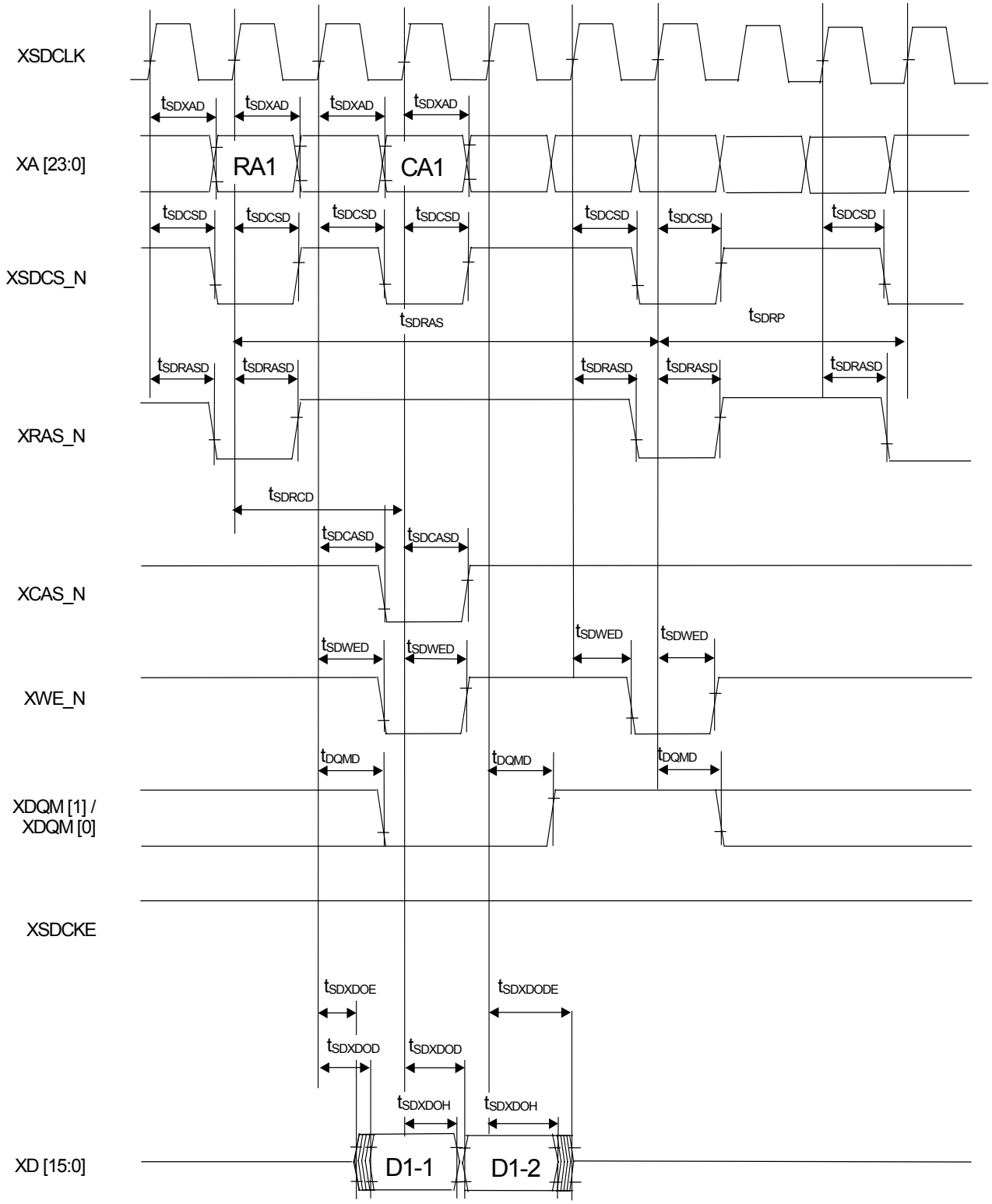
SDRAM Write Cycle
(Bus Width 16 bit SDRAM Byte/Half Word Access)



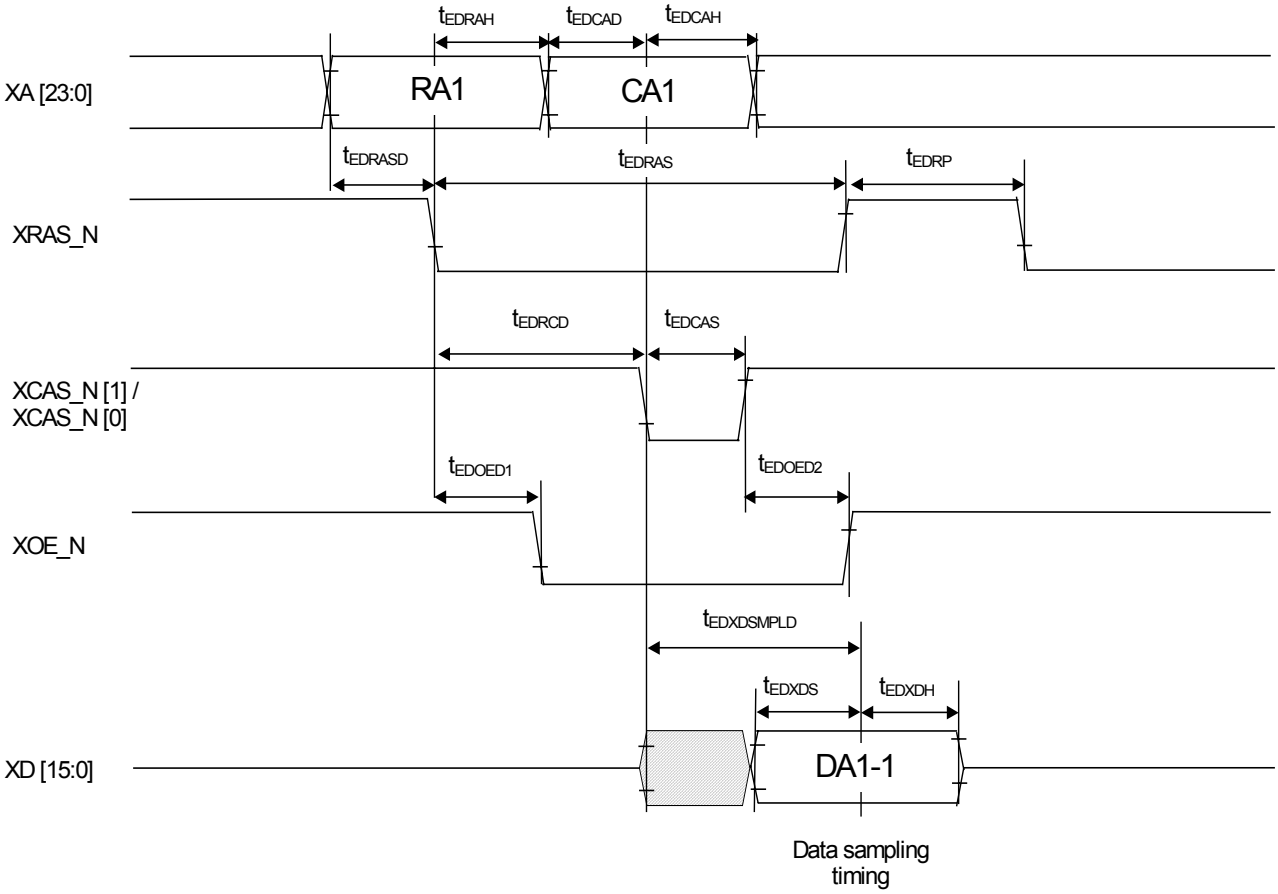
SDRAM Read Cycle
(Bus Width 16 bit SDRAM Word Access)



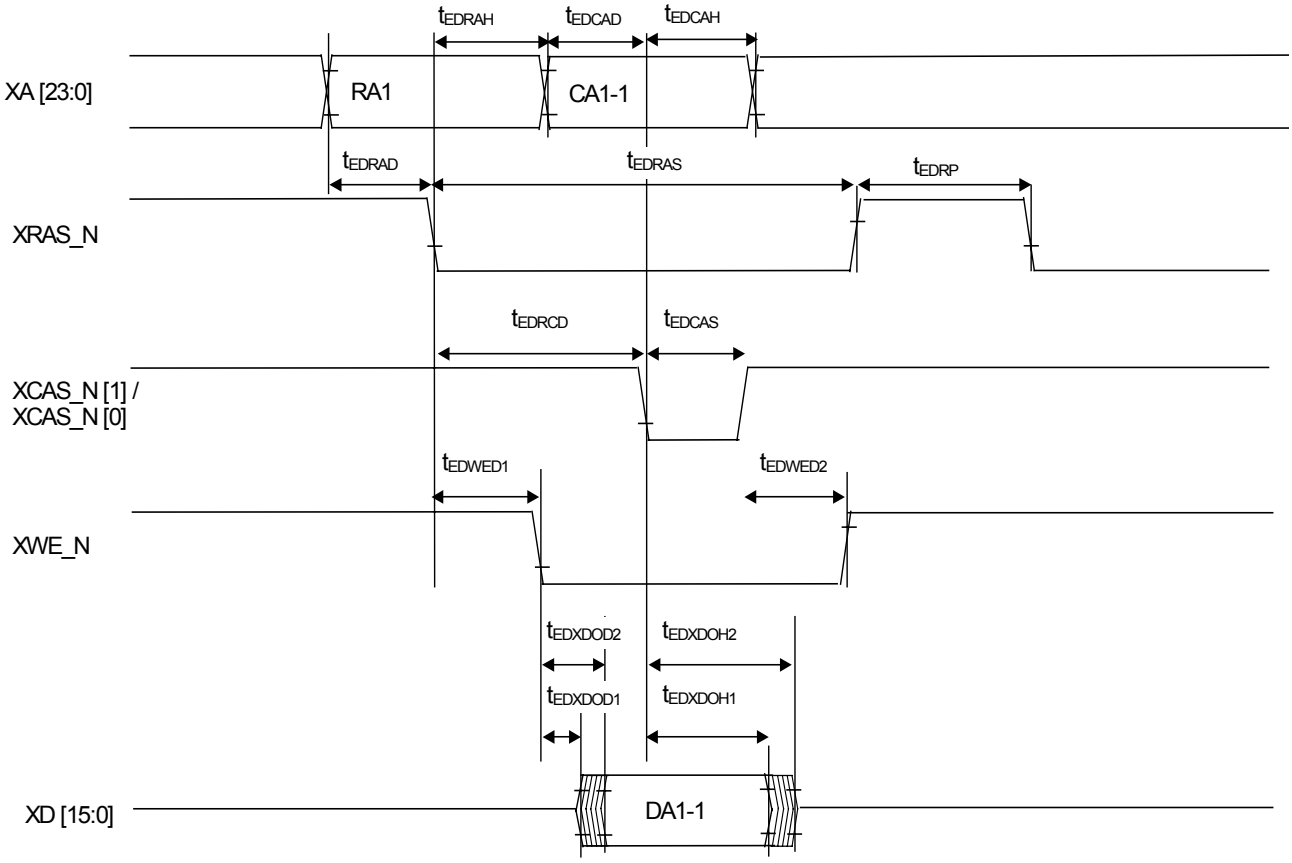
SDRAM Write Cycle
(Bus Width 16 bit SDRAM Word Access)



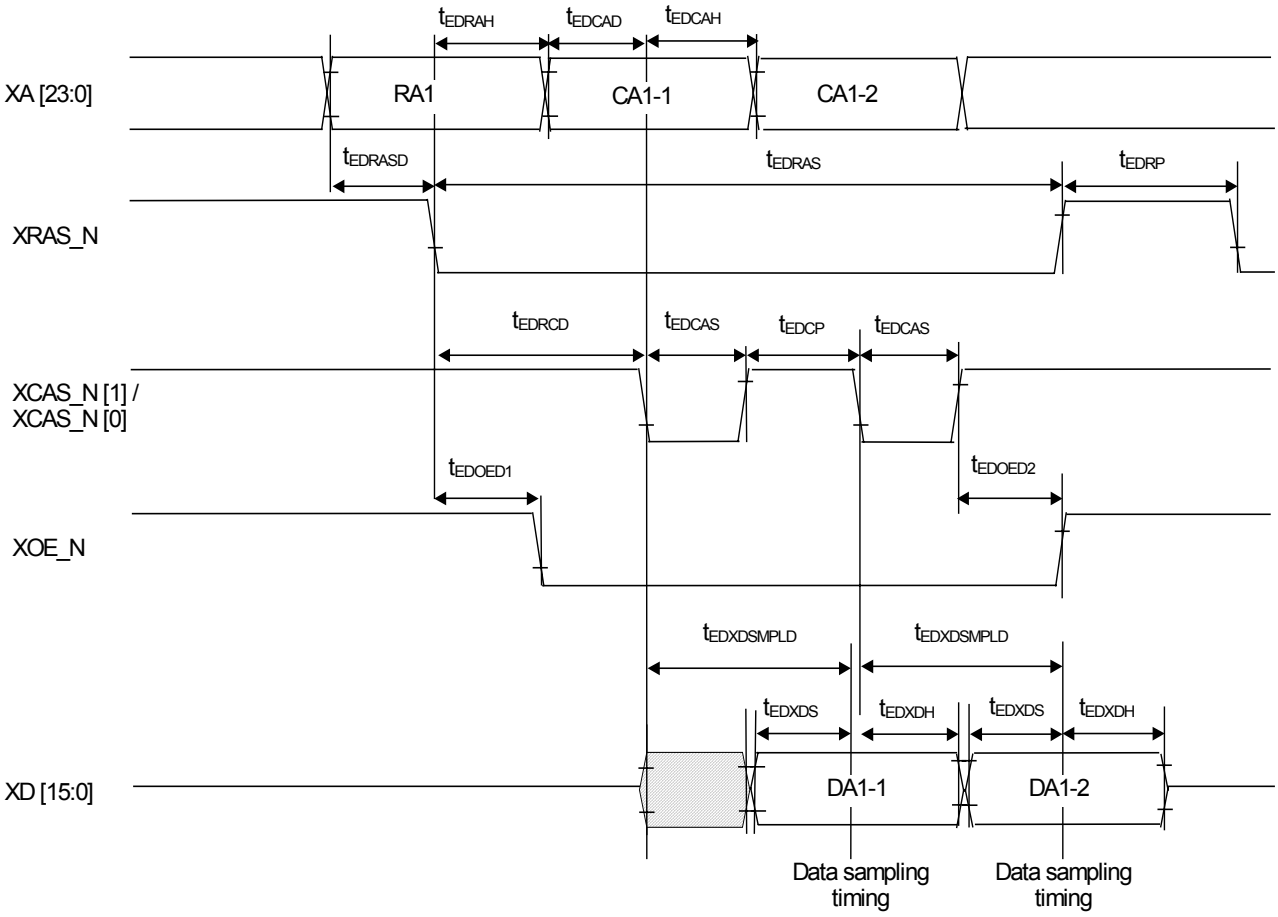
EDO DRAM Read Cycle
(Bus Width 16 bit EDO DRAM Byte/Half Word Access)



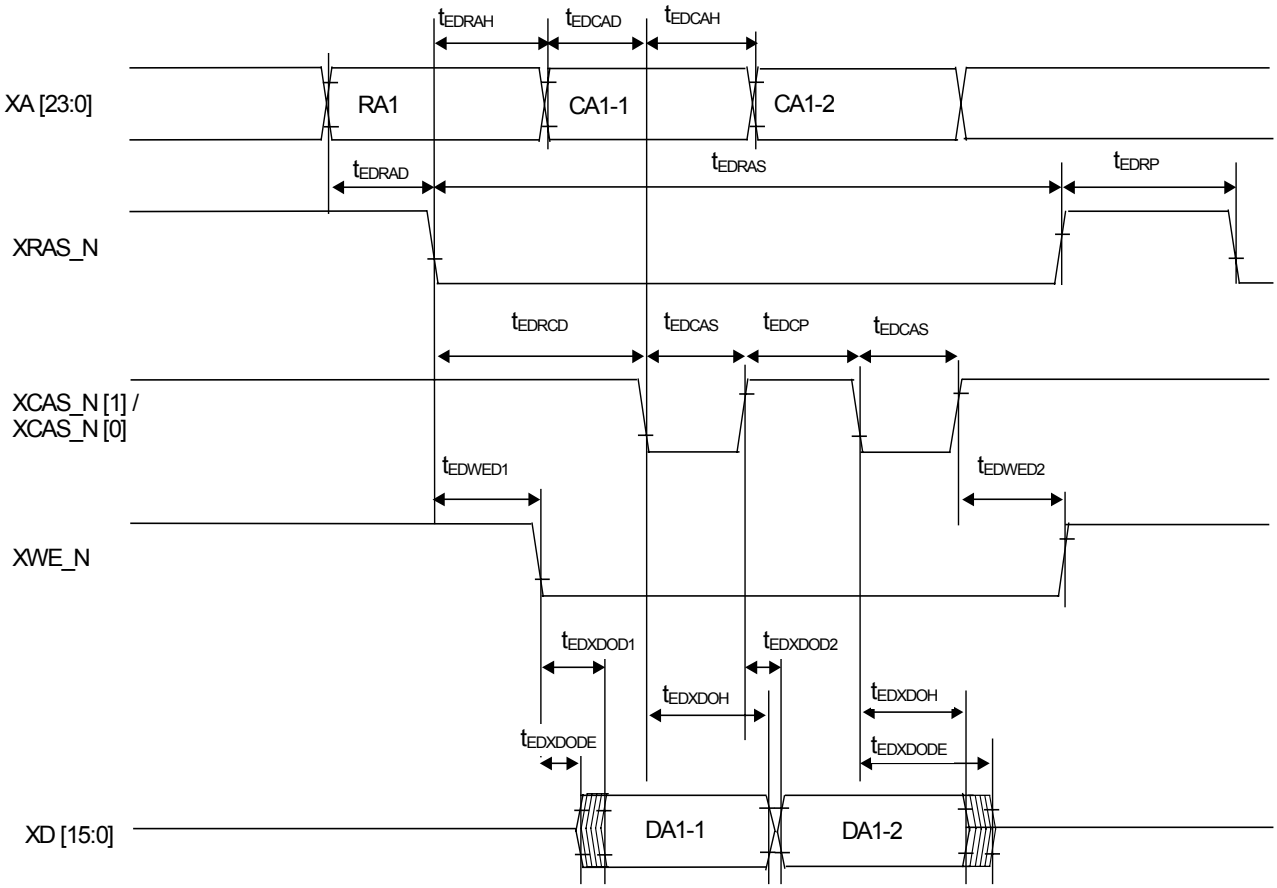
EDO DRAM Write Cycle
(Bus Width 16 bit EDO DRAM Byte/Half Word Access)



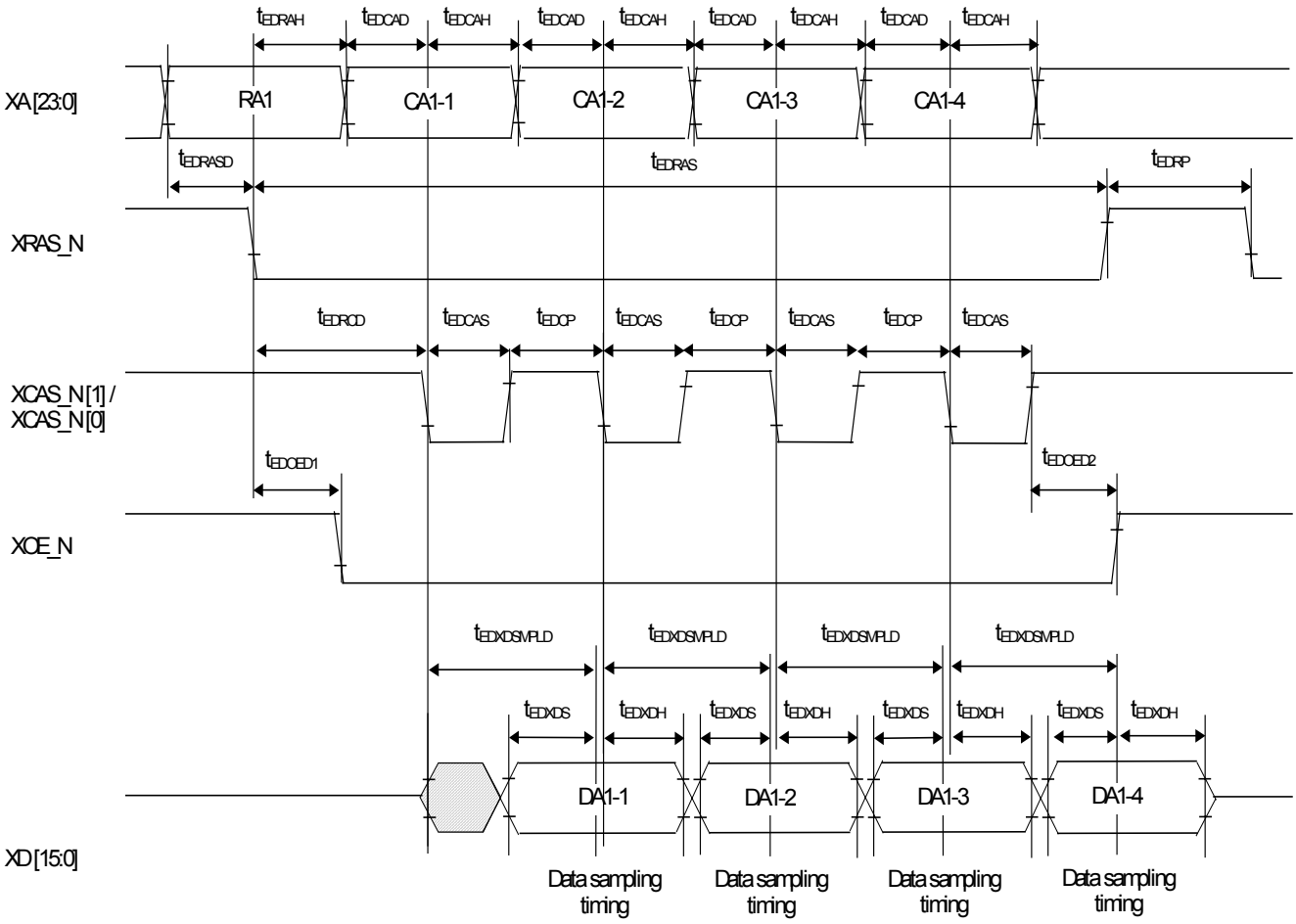
EDO DRAM Read Cycle
(Bus Width 8 bit EDO DRAM Half Word Access/
Bus Width 16 bit EDO DRAM Word Access)



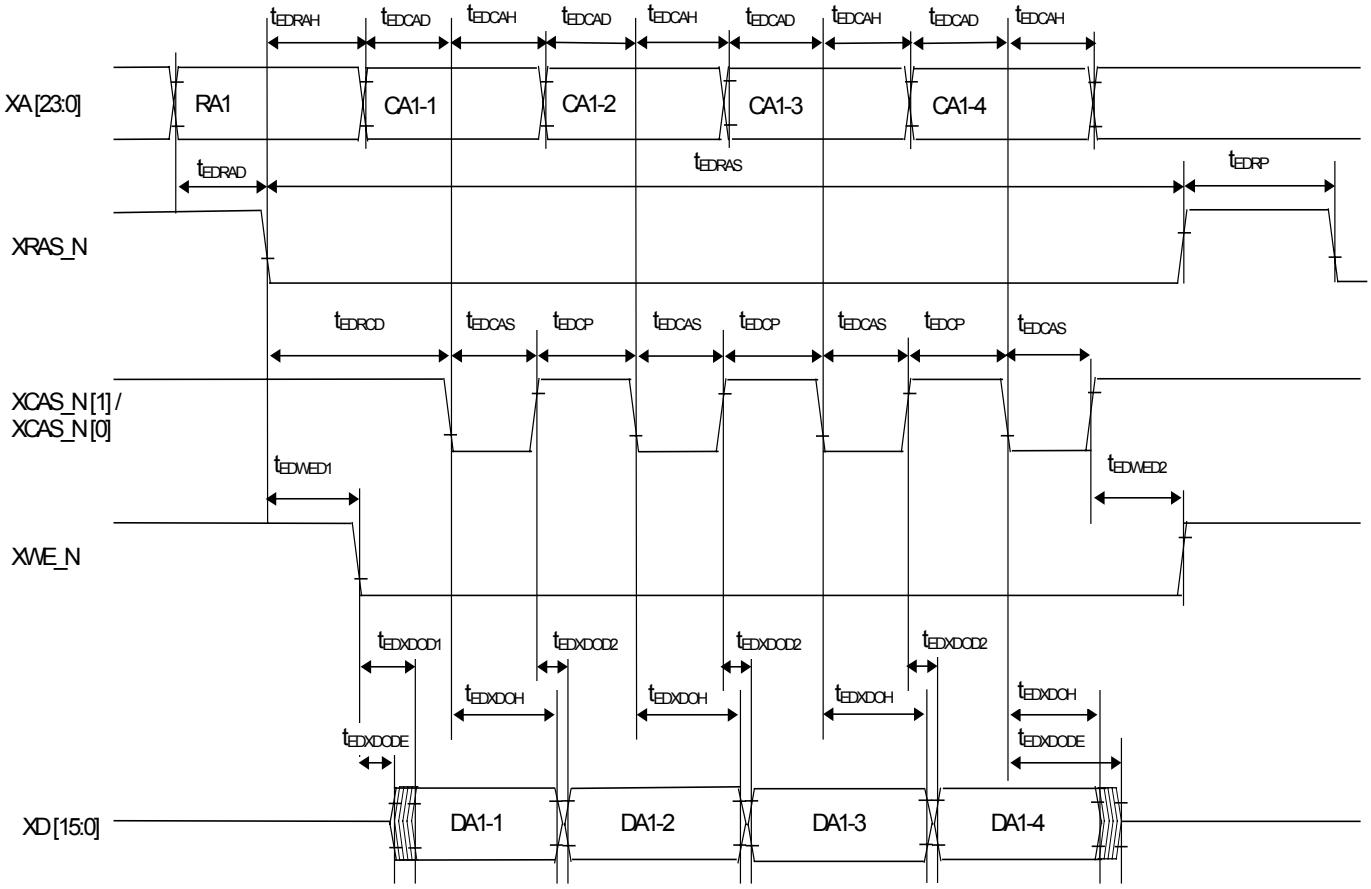
EDO DRAM Write Cycle
(Bus Width 8 bit EDO DRAM Half Word Access/
Bus Width 16 bit EDO DRAM Word Access)



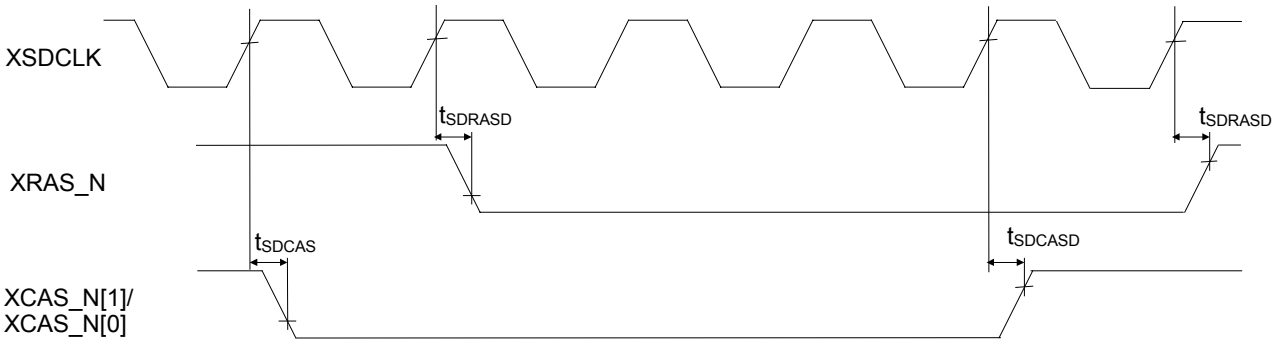
EDO DRAM Read Cycle
(Bus Width 8 bit EDO DRAM Word Access)



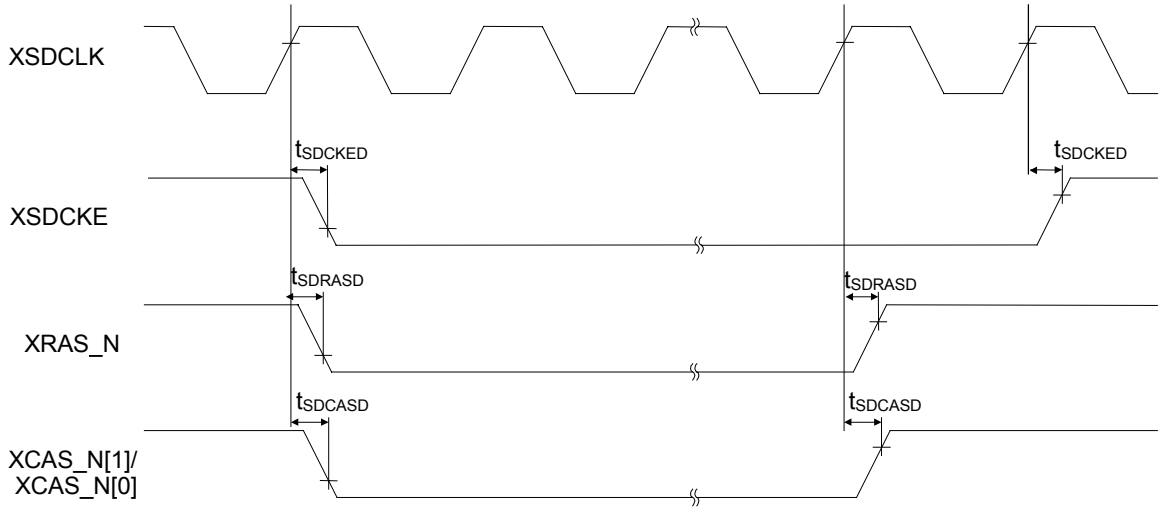
EDO DRAM Write Cycle
(Bus Width 8 bit EDO DRAM Word Access)



CAS before RAS (CBR) Refresh Operation



Self Refresh Operation



Analog-to-Digital Converter Characteristics

(V_{DD_CORE} = 2.50 V, V_{DD_IO} = 3.3 V, Ta = 25°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Resolution	n	—	—	—	10	bit
Linearity error	E_L	Analog input source impedance Ri ≤ 1kΩ	—	±3	—	LSB
Differential linearity error	E_D		—	±3	—	
Zero scale error	E_{ZS}		—	±6	—	
Full scale error	E_{FS}		—	±6	—	
Conversion time	t_{CONV}	—	5	—	—	µs
Throughput		—	10	—	200	kHz

Notes: VDD_io and AVDD should be supplied separatedly

- Definition of Terms

(1) Resolution: Minimum input analog value recognized. For 10-bit resolution, this is (VREF – Aground) ÷ 1024.

(2) Linearity error: Difference between the theoretical and actual conversion characteristics. (Note that it does not include quantization error.) The theoretical conversion characteristic divides the voltage range between VREF and AGND into 1024 equal steps.

(3) Differential linearity error: Difference between the theoretical and actual input voltage change producing a 1-bit change in the digital output anywhere within the conversion range. This is an indicator of conversion characteristic smoothness. The theoretical value is (VREF – Aground) ÷ 1024.

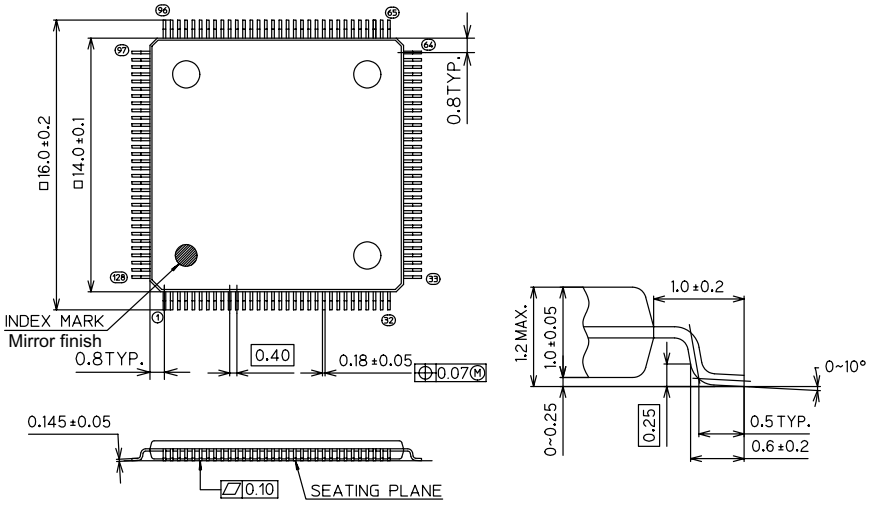
(4) Zero scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “000H” to “001H.”

(5) Full scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “3FEH” to “3FFH.”

PACKAGE DIMENSIONS

(Unit : mm)

TQFP128-P-1414-0.40-K



Oki Electric Industry Co., Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Nov. 18, 1999

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL674000-01	Oct., 2001	–	–	Preliminary edition 1
PEDL674000-02	May 17, 2002	–	–	Preliminary edition 2
		1	1	Feature Table rewritten.
		2-13	2-12	Pin names are changed.
		14-16	13-15	Description rewritten.
		17	16-37	Electrical characteristics added.
FEDL674000-01	Aug. 8, 2002	–	–	Final edition 1
		1	1	Number of interrupt sources corrected.
		8	8	TBE signal description corrected.
		8	8	Pin numbers of XA[23:19] and XA[18:0] corrected.
		15-36	15-50	Description rewritten.

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

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