National Semiconductor

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MM145453
Liquid Crystal Display Driver

General Description

The MM145453 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. The chip can drive up to 33 LCD segments and can be paralleled to increase this number. The chip is capable of driving a 4½ digit 7-segment display with minimal interface between the display and the data source.

The MM145453 stores display data in latches after it is clocked in, and holds the data until new display data is received.

The MM145453 is available in a molded 44 pin surface mount PLCC package. The MM145453 is pin out and functionally compatible with the MC145453.

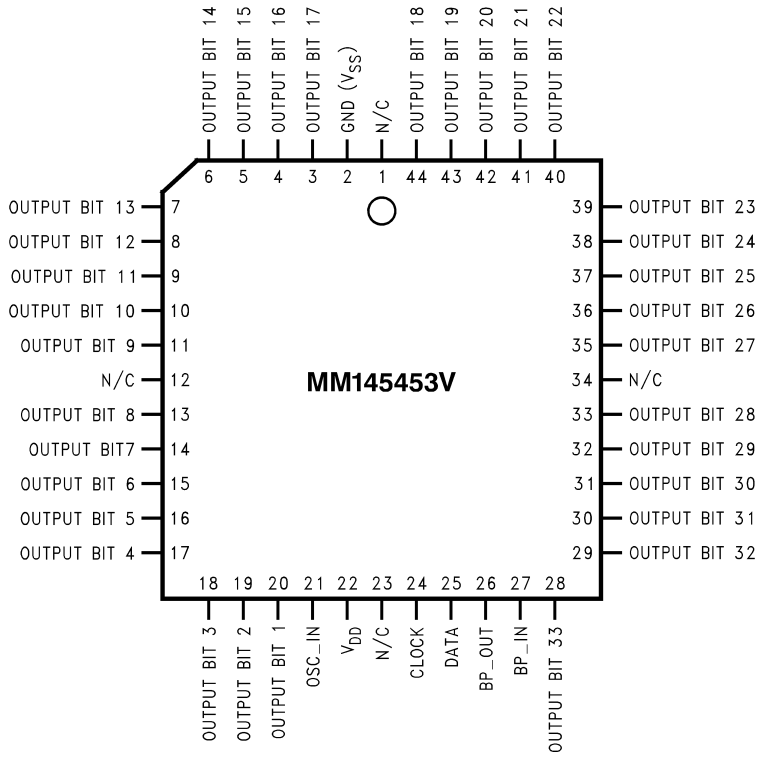
Features

- Serial Data Input
- Wide Power Supply operation
- TTL Compatibility
- Up to 33 LCD Segments
- Alphanumeric or Bar Graph capability
- Cascaded operation capability
- Pin Compatible with MC145453

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation displays
- Remote displays

Connection Diagram



Top View
Order Number MM145453V
See NS Package Number V44A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin, Referenced to Gnd	-0.3V to +10V
Storage Temperature	-65˚C to +150˚C
Power Dissipation at 25˚C	350mW
Power Dissipation at 70˚C	300mW
Junction Temperature	+150˚C
Lead Temperature (Soldering, 10s)	300˚C

Recommended Operating Conditions

V_{DD}	3V to 10V
Operating Temperature	−40˚C to 85˚C

Electrical Characteristics

The following specifications apply for T_A within operation range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified.

Parameter	Conditions	Min	Typical	Max	Units
Supply Voltage, V_{DD}		3		10	V
Average Supply Current, I_{DD}	All Outputs Open, Clock=Gnd, Data=Gnd,OSC=Gnd, BP_IN 32Hz				
	V_{DD}= 5V			10	µA
	V_{DD}= 10V			40	µA
Input Logical '0' Voltage, V_{IL}	V_{DD}= 3V			0.4	V
	V_{DD}= 5V			0.8	V
	V_{DD}= 10V			0.8	V
Input Logical '1' Voltage, V_{IH}	V_{DD}= 3V	2.0			V
	V_{DD}= 5V	2.0			V
	V_{DD}= 10V	8.0			V
Segment Sink Current, I_{OL}	V_{DD}= 3V, V_{OUT}= 0.3V	-20	-40		µA
Segment Source Current, I_{OH}	V_{DD}= 3V, V_{OUT}= 2.7V	20	40		µA
Backplane Out Sink Current, I_{OL}	V_{DD}= 3V, V_{OUT}= 0.3V	-320	-500		µA
Backplane Out Source Current, I_{OH}	V_{DD}= 3V, V_{OUT}= 2.7V	320	500		µA
Segment Output Offset Voltage	Segment Load = 250pF (Note 2)			+/-50	mV
Backplane Output Offset Voltage	Backplane Load = 8750pF (Note 2)			+/-50	mV
Backplane Out Frequency	R_{OSC_IN}= 50kΩ, C_{OSC_IN}= 0.01µF		75		Hz
Clock Input Frequency, f_{CLOCK}	V_{DD}= 3V (Notes 2, 3)			500	kHz
	V_{DD}= 5V (Note 2)			750	kHz
	V_{DD}= 10V (Note 2)			1.0	MHz
Clock Input Duty Cycle		40		60	%
Data Input Set-Up Time, t_{DS}		300			ns
Data Input Hold Time, t_{DH}		300			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: This parameter is guaranteed (but not production tested) over the operating temperature range and the operating supply voltage range. Not to be used in Q.A. testing.

Note 3: AC input waveform for test purposes: t_r≤ 20ns, t_f≤ 20ns, f_{CLOCK}= 500kHz, Duty Cycle = 50% ±10%

Note 4: Clock input rise time (t_r) and fall time (t_f) must not exceed 300ns

Electrical Characteristics (Continued)

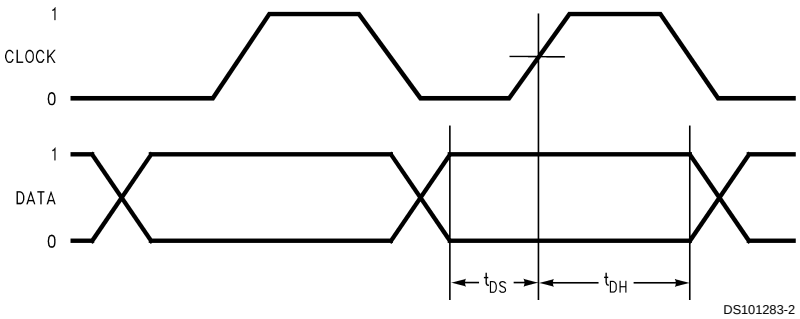


FIGURE 1.

Block Diagram

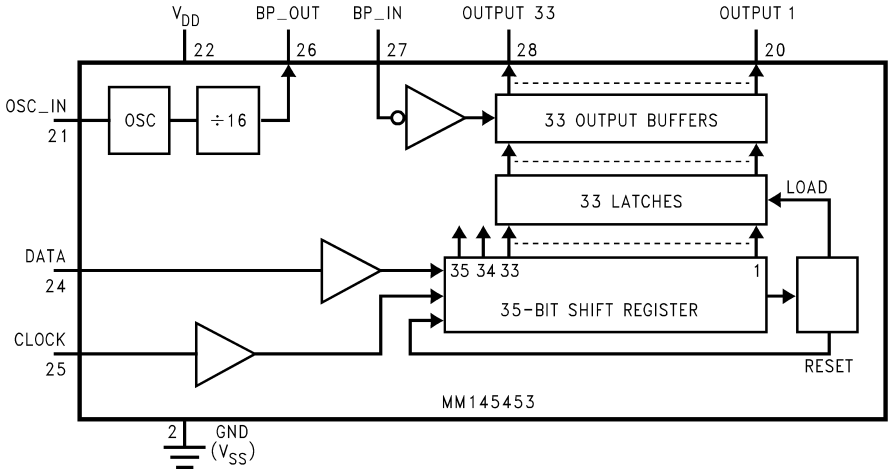


FIGURE 2.

Applications Information

The MM145453 is specifically designed to operate 4½ digit 7-segment displays with minimal interface with the display and data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial Data and Clock. Using a format of a leading ″1″ followed by the 33 data bits and 2 trailing don't care bits, allows data transfer without the need of an additional Data Load signal. Since the MM145453 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM145453. The transfer of the 33 data bits is complete at the falling edge of the 36th clock cycle, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Figure 3 shows the data input format. A single start bit of logical '1' precedes the 33 bits of segment data for a total of 34 bits that need to be defined and clocked in. After the 34 bits are clocked in, 2 additional clock cycles are required. At the 36th clock cycle an internal LOAD signal is generated synchronously with the rising edge of the Clock In signal, which loads the 33 bits of segment data in the shift register into the latches. At the falling edge of the 36th clock cycle an internal RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation. The data during the 35th and 36th clock cycles is ″don't care″, but setting data to logical '0' for these two clock cycles is the preferred format.

The data input bits map directly to the segment output pins and the display. The MM145453 does not have any format restrictions, as all outputs are controllable.

The MM145453 has an internal oscillator which can generate the required clock signal to drive the LCD back plane. The frequency of the internal oscillator is set by a pull-up resistor (R_{OSC_IN}) connected from the OSC_IN pin to V_{DD}, and a capacitor (C_{OSC_IN}) connected from the OSC_IN pin to Ground. Due to the current sink limitations of the OSC_IN circuitry, the lowest recommended resistor value for setting the oscillator frequency is 9kΩ. It will typically take 2 to 4 RC time constants to charge the OSC_IN pin from near 0V to within 1V of V_{DD} which is the high threshold voltage point for the OSC_IN circuitry. An approximate calculation of f_{OSC} is:

$f_{OSC} = 1 / (\ln(V_{DD}/1V) \times R_{OSC\_IN} \times C_{OSC\_IN})$

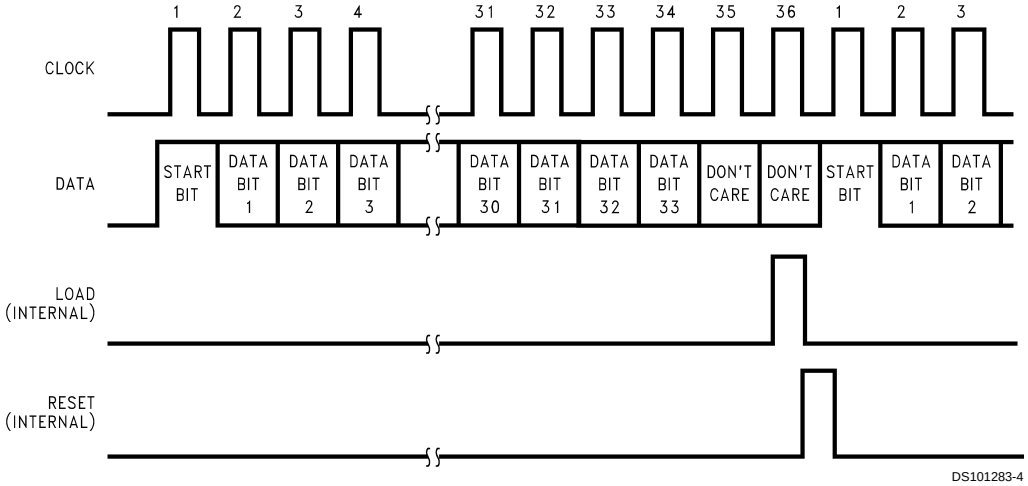
A R_{OSC_IN} resistor value of 50kΩ with a C_{OSC_IN} capacitor value of 0.01µF and a V_{DD} value of 5.00V would produce a typical oscillator frequency (f_{OSC}) of about 1200Hz. The f_{OSC} signal is divided by 16 before it is presented at the BP_OUT pin. For this example the approximate BP_OUT frequency will be $f_{OSC}/16$, or about 75Hz.

Applications Information (Continued)

The BP_IN pin of the MM145453 can be used with an externally supplied signal, provided it has a duty cycle of 50%. Any deviation from a precise 50% duty cycle will result in an offset voltage on the LCD. The use of an external clock allows synchronizing the display drive with AC power, other internal clocks, or DVM integration time to reduce interference from the display. When using an external clock for the back plane drive the internal oscillator should be disabled by connecting the OSC_IN pin directly to ground. This will prevent possible internal oscillations, and reduce device dissipation.

The MM145453 is a pin out variation of the MM5453. For additional applications information please refer to the MM5453 data sheet.

Input Data Format



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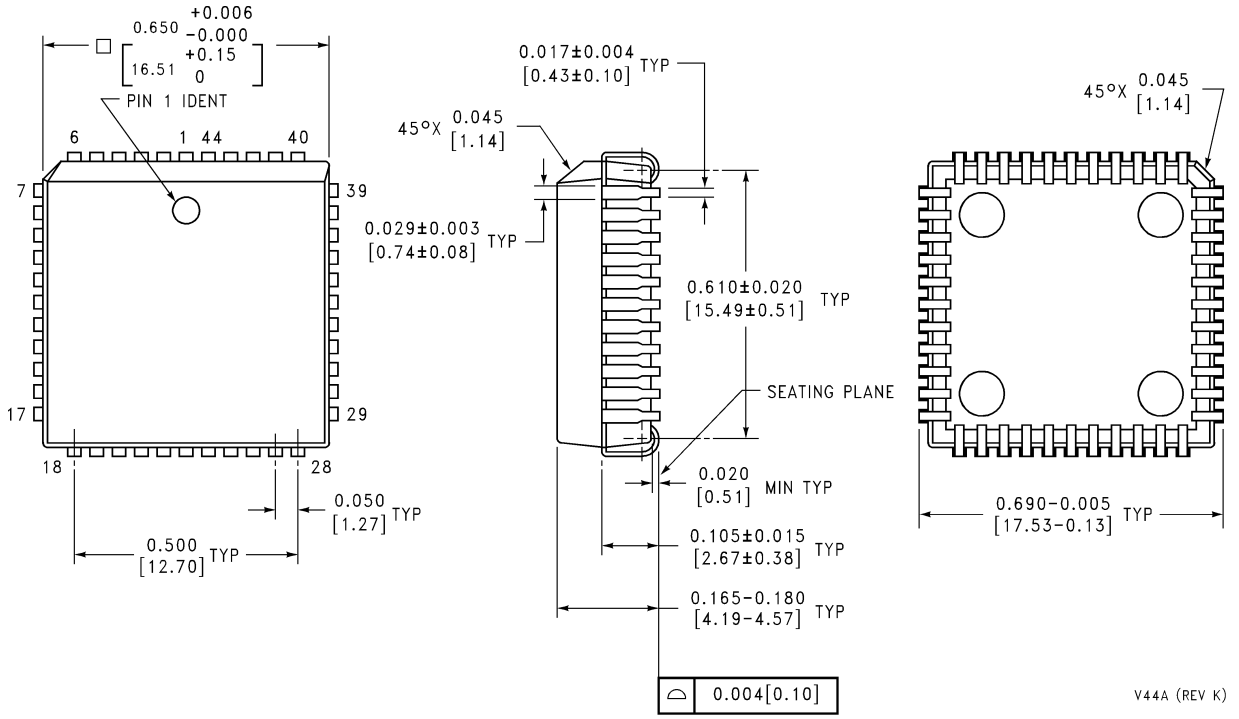
Physical Dimensions inches (millimeters) unless otherwise noted



Top View
Order Number MM145453V
See NS Package Number V44A

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