National Semiconductor

February 1995

# MM5450/MM5451 LED Display Drivers

## General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. The MM5450/MM5451 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to $V_{DD}$.

## Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

## Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability
- $\theta_{JA}$ DIP — Board = 49°C/W, Socket = 54°C/W

## Block Diagram

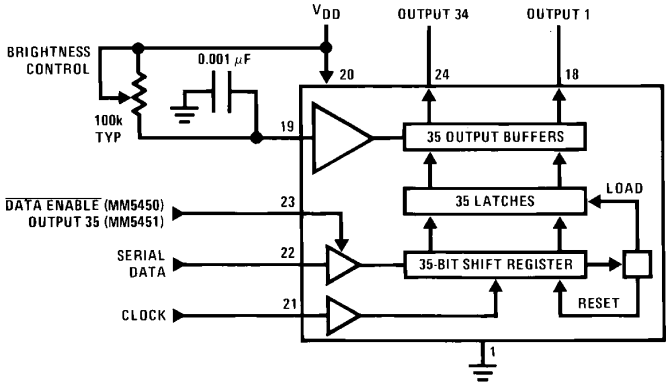


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**FIGURE 1**

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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $V_{SS} - 0.3V$ to $V_{SS} + 12V$ |
| Operating Temperature | $-25°C$ to $+85°C$ |
| Storage Temperature | $-65°C$ to $+150°C$ |
| Junction Temperature | $+150°C$ |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Power Dissipation at $+25°C$

| | |
|---|---|
| Molded DIP Package, Board Mount | 2.5W* |
| Molded DIP Package, Socket Mount | 2.3W** |

*Molded DIP Package board mount, $\theta_{JA} = 49°C/W$, Derate 20.4 mW/°C above 25°C.

**Molded DIP Package, socket mount, $\theta_{JA} = 54°C/W$, Derate 18.5 mW/°C above 25°C.

## Electrical Characteristics $T_A$ within operating range, $V_{DD} = 4.75V$ to 11.0V, $V_{SS} = 0V$ unless otherwise specified

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply | | 4.75 | | 11 | V |
| Power Supply Current | Excluding Output Loads | | | 7 | mA |
| Input Voltages | | | | | |
| Logical "0" Level ($V_L$) | $\pm 10\ \mu A$ Input Bias | $-0.3$ | | 0.8 | V |
| Logical "1" Level ($V_H$) | $4.75V \le V_{DD} \le 5.25V$ | 2.2 | | $V_{DD}$ | V |
| | $V_{DD} > 5.25V$ | $V_{DD} - 2V$ | | $V_{DD}$ | V |
| Brightness Input (Note 2) | | 0 | | 0.75 | mA |
| Output Sink Current | | | | | |
| Segment OFF | $V_{OUT} = 3.0V$ | | | 10 | $\mu A$ |
| Segment ON | $V_{OUT} = 1V$ (Note 3) | | | | |
| | Brightness Input $= 0\ \mu A$ | 0 | | 10 | $\mu A$ |
| | Brightness Input $= 100\ \mu A$ | 2.0 | 2.7 | 4 | mA |
| | Brightness Input $= 750\ \mu A$ | 15 | | 25 | mA |
| Brightness Input Voltage (Pin 19) | Input Current $750\ \mu A$ | 3.0 | | 4.3 | V |
| Output Matching (Note 1) | | | | $\pm 20$ | % |
| Clock Input | (Notes 5 and 6) | | | | |
| Frequency, $f_C$ | | | | 500 | kHz |
| High Time, $t_h$ | | 950 | | | ns |
| Low Time, $t_l$ | | 950 | | | ns |
| Data Input | | | | | |
| Set-Up Time, $t_{DS}$ | | 300 | | | ns |
| Hold Time, $t_{DH}$ | | 300 | | | ns |
| Data Enable Input | | | | | |
| Set-Up Time, $t_{DES}$ | | 100 | | | ns |

**Note 1:** Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

**Note 2:** With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

**Note 3:** See *Figures 5, 6,* and *7* for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

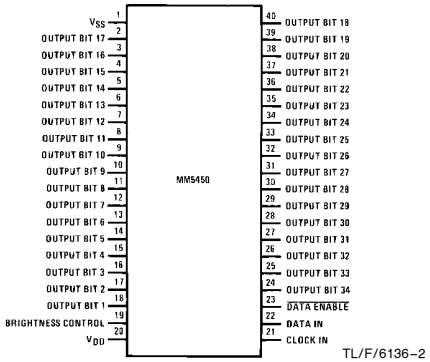
**Note 4:** The $V_{OUT}$ voltage should be regulated by the user. See *Figures 6* and *7* for allowable $V_{OUT}$ vs $I_{OUT}$ operation.

**Note 5:** AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% $\pm$10% duty cycle.

**Note 6:** Clock input rise and fall times must not exceed 300 ns.

## Connection Diagrams

**Dual-In-Line Package**

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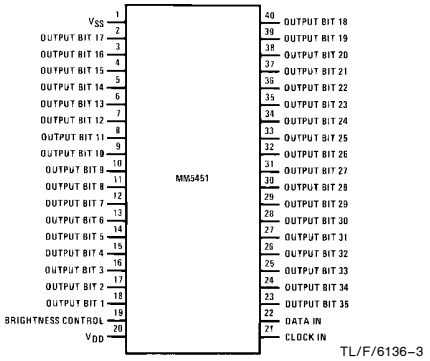
**Top View**

**FIGURE 2a**

**Dual-In-Line Package**

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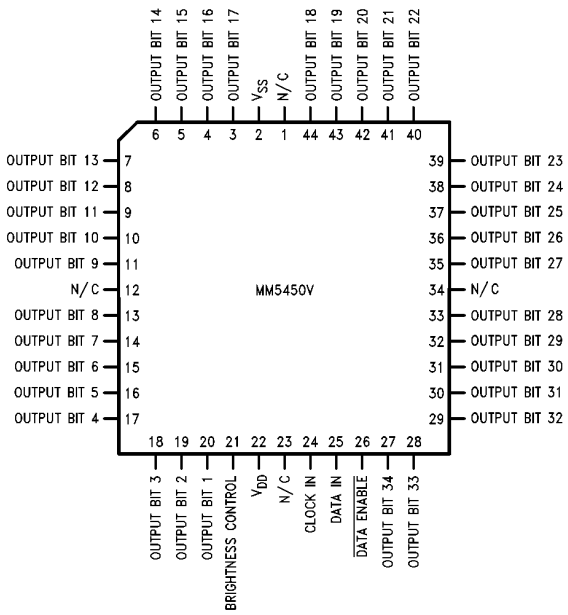
**Top View**

**FIGURE 2b**

**Order Number MM5450N, MM5451N, MM5450V or MM5451V**
**See NS Package Number N40A or V44A**

## Connection Diagrams (Continued)

**Plastic Chip Carrier**

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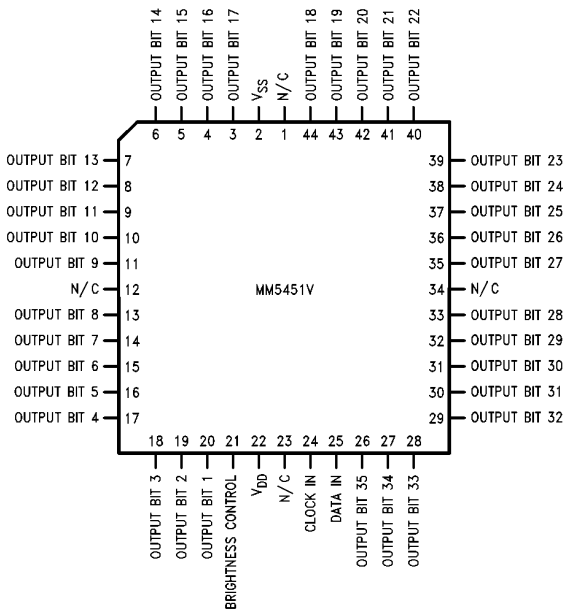
**Top View**

**Plastic Chip Carrier**

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**Top View**

## Functional Description

Both the MM5450 and the MM5451 are specifically designed to operate 4- or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading ''1'' followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. For the MM5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the MM5450. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

*Figure 4* shows the input data format. A start bit of logical ''1'' precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

*Figure 2* shows the pin-out of the MM5450 and MM5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical ''1'' at the input will turn on the appropriate LED.

*Figure 3* shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V $V_{OUT}$. The following equation can be used for calculations.

$T_j = (V_{OUT})\ (I_{LED})$ (No. of segments)$(\theta_{JA}) + T_A$

where:

$T_j$ = junction temperature, 150°C max

$V_{OUT}$ = the voltage at the LED driver outputs

$I_{LED}$ = the LED current

$\theta_{JA}$ = thermal coefficient of the package

$T_A$ = ambient temperature

$\theta_{JA}$ (Socket Mount) = 54°C/W

$\theta_{JA}$ (Board Mount) = 49°C/W

The above equation was used to plot *Figure 5, Figure 6* and *Figure 7.*

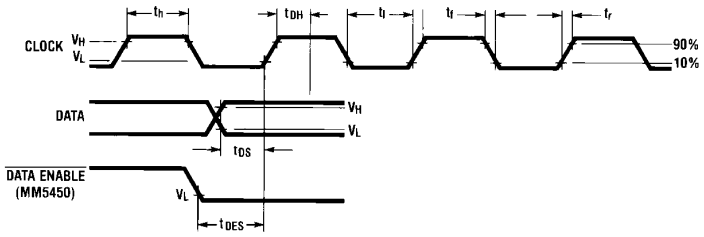


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**FIGURE 3**

## Functional Description (Continued)

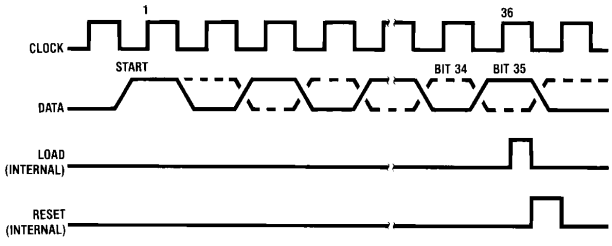


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**FIGURE 4. Input Data Format**

## Typical Performance Characteristics

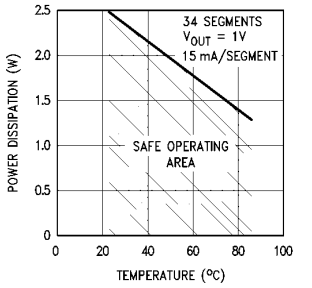


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**FIGURE 5**

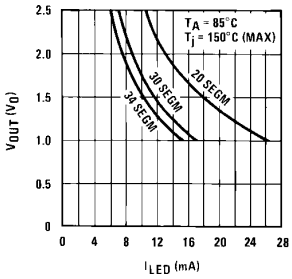


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**FIGURE 6**

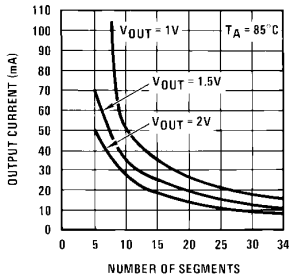


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**FIGURE 7**

## Typical Applications

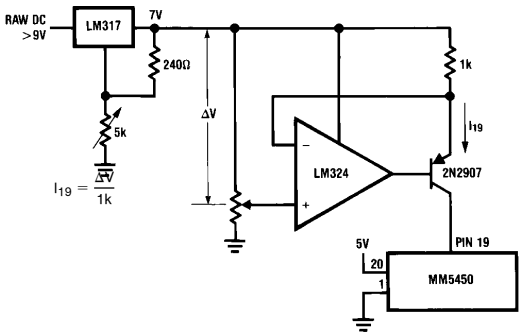


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**FIGURE 8. Typical Application of Constant Current Brightness Control**

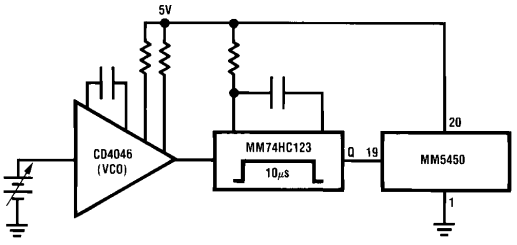


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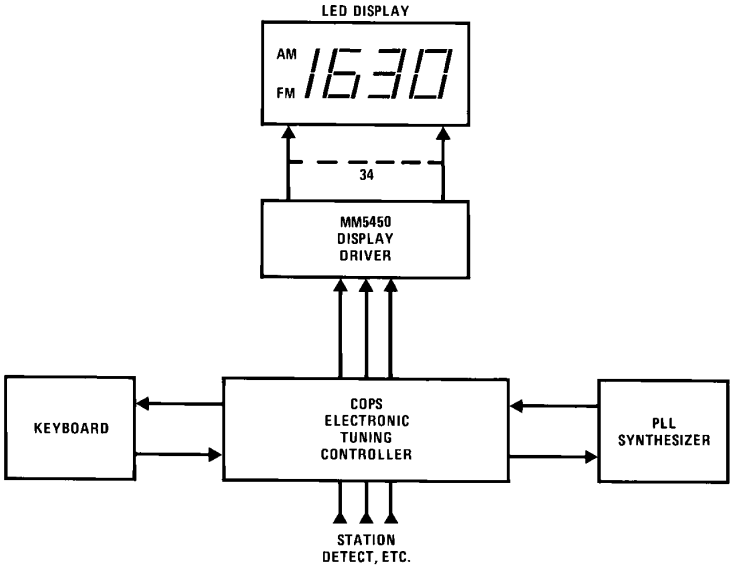
**FIGURE 9. Brightness Control Varying the Duty Cycle**

## Typical Applications (Continued)

**Basic Electronically Tuned Radio System**

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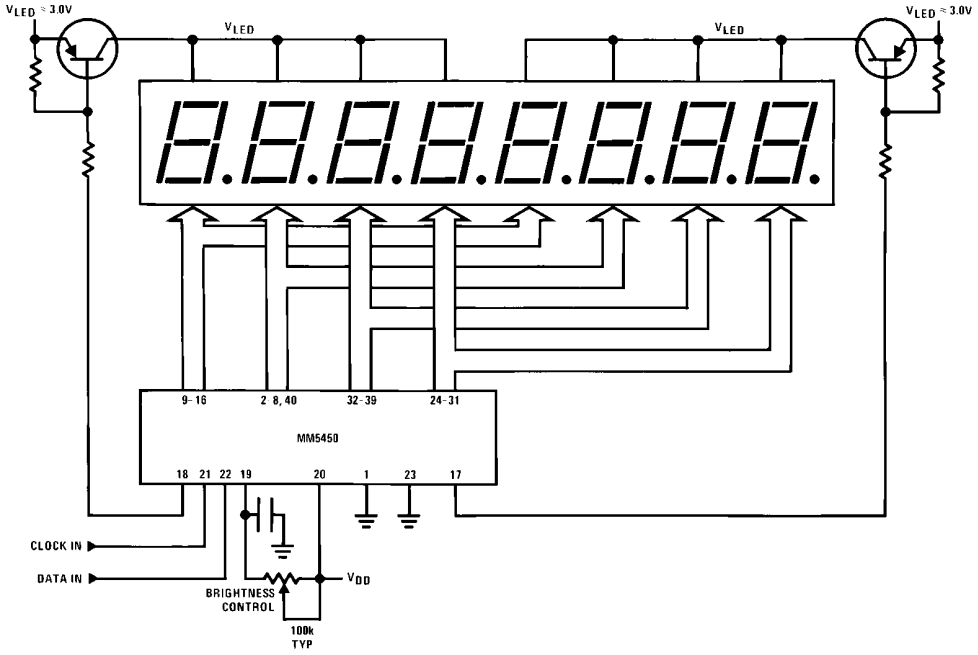
**Duplexing 8 Digits with One MM5450**

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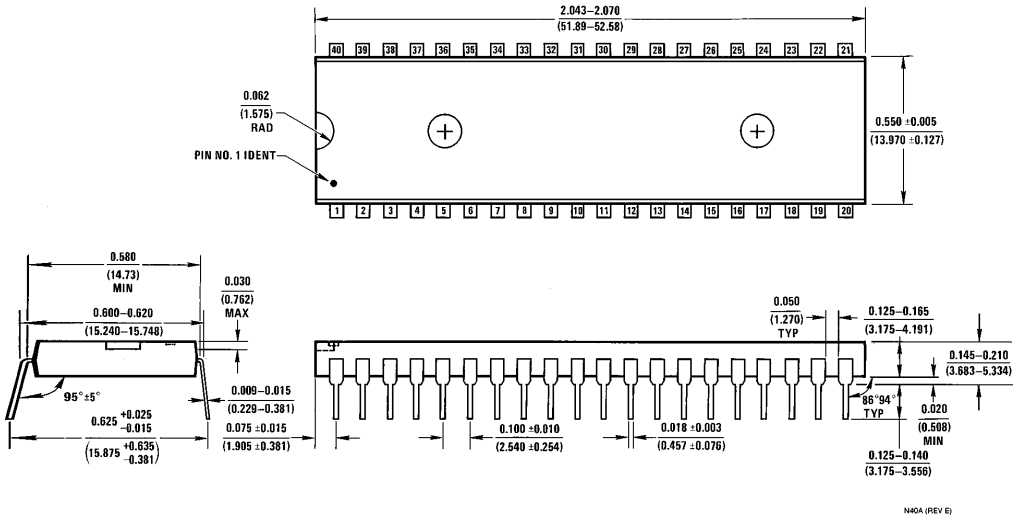
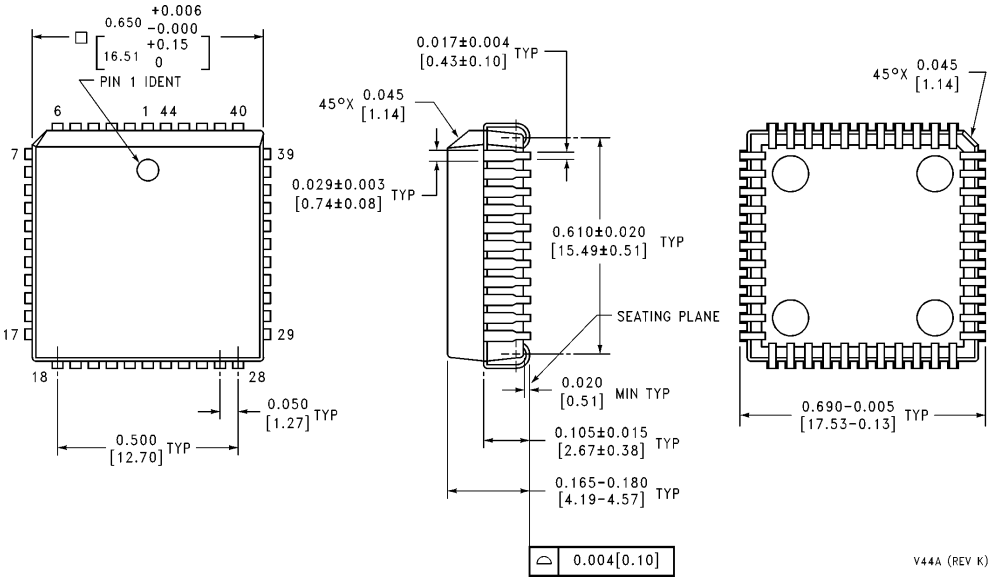
## Physical Dimensions inches (millimeters)




**Molded Dual-In-Line Package (N)**
**Order Number MM5450N or MM5451N**
**NS Package Number N40A**

## Physical Dimensions inches (millimeters) (Continued)




**Plastic Chip Carrier (V)**
**Order Number MM5450V or MM5451V**
**NS Package Number V44A**

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**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

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