National Semiconductor

MM5484 16-Segment LED Display Driver

General Description

The MM5484 is a low threshold N-channel metal gate circuit using low threshold enhancement and ion implanted depletion devices. The MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments. The MM5484 is designed to drive common anode separate cathode LED displays.

Features

- Serial data input
- Wide power supply operation
- 16 output, 15 mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

Block and Connection Diagrams

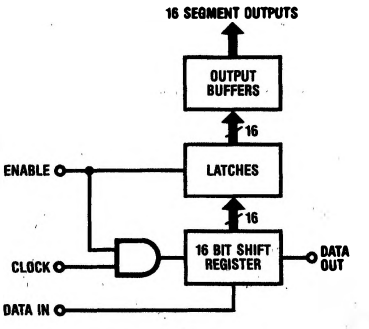

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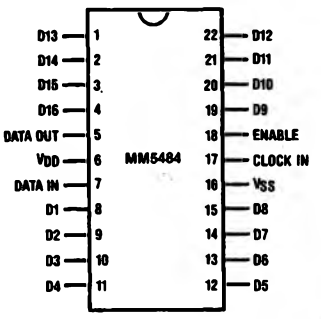
FIGURE 1. MM5484

Dual-In-Line Package



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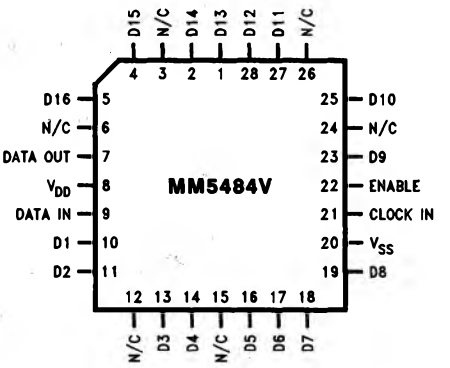
Top View

Order Number MM5484N
See NS Package Number N22A

PLCC



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Top View

Order Number MM5484V
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at LED Outputs	V_{SS} − 0.5V to V_{SS} + 12V
Voltage at Other Pins	V_{SS} − 0.5V to V_{SS} + 10V

Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, board mount	2W*
Molded DIP Package, socket mount	1.8W**
*Molded DIP Package, board mount, derate 15.8m W/°C above 25°C.	θ_{JA} = 63°C/W,
**Molded DIP Package, socket mount, derate 14.5m W/°C above 25°C.	θ_{JA} = 69°C/W,
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		4.5		9	V
Supply Current			5	10	mA
Logic One					
Input High Level V_{IH}		2.4		V_{DD} + 0.5	V
Logic Zero					
Input Low Level V_{IL}		0		0.8	V
Input Current	High or Low Level			±1	μA
Input Capacitance				7.5	pF
OUTPUTS					
Data Output Voltage					
High Level V_{OH}	I_{OUT} = 0.1 mA	V_{DD} − 0.5			V
Low Level V_{OL}	I_{OUT} = −0.1 mA			0.5	V
Segment Off	V_{OUT} = 12V			50	μA
(Logic Zero on Input)	R_{EXT} = 400Ω				
Output Current Segment On					
(Logic One on Input)	I_{OUT} = 15 mA		0.5	1.0	V
Output Voltage	V_{DD} ≥ 6V				

AC Electrical Characteristics

(See *Figure 3.*) V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Frequency				0.5	MHz
t_h	High Time		0.95			μs
t_l	Low Time		0.95			μs
t_{S1}	Data Setup Time		0.5			μs
t_{H1}	Data Hold Time		0.5			μs
t_{S2}	Enable Setup Time		0.5			μs
t_{H2}	Enable Hold Time		0.5			μs
t_{pd}	Data Out Delay				0.5	μs

Note 1: Under no condition should the power dissipated by the segment driver exceed 50 mW nor the entire chip power dissipation exceed 500 mW.

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 500 ns.

Functional Description

The MM5484 is designed to drive LED displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, DATA IN, CLOCK and ENABLE. The signal ENABLE acts as an envelope and only while this signal is at a logic '1' do the circuits recognize the clock signal.

While ENABLE is high, data on the serial data input is transferred and shifted in the internal shift register on the rising clock edge, i.e. a logic '0' to logic '1' transition.

When the ENABLE signal goes to a low (logic zero state), the contents of the shift register is latched and the display will show the new data. While new data is being loaded into the SR the display will continue to show the old data.

For the MM5484, data is output from the serial DATA OUT pin on the falling edge of clock so cascading is made simple with race hazards eliminated.

When the chip first powers on, an internal power on reset signal is generated which resets the SR and latches to zero so that the display will be off.

Timing Diagram

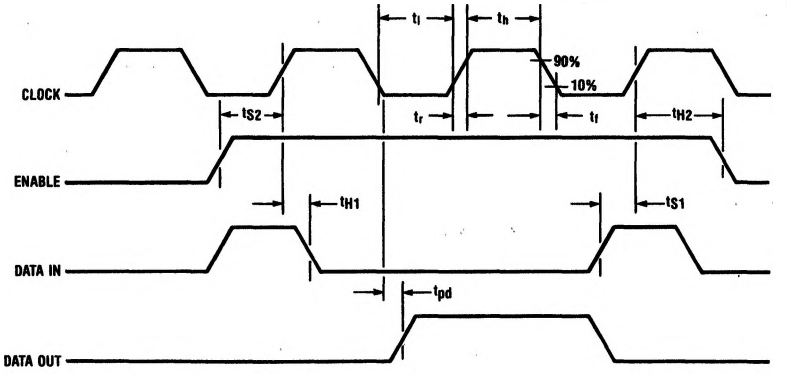

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FIGURE 3