MM54C165,MM74C165

MM54C165 MM74C165 Parallel-Load 8-Bit Shift Register

Literature Number: SNOS323A

National Semiconductor

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MM54C165/MM74C165
Parallel-Load 8-Bit Shift Register

General Description

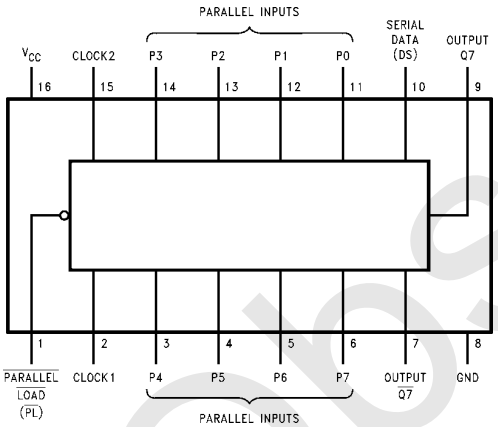
The MM54C165/MM74C165 functions as an 8-bit parallel-load, serial shift register. Data is loaded into the register independent of the state of the clock(s) when PARALLEL LOAD ($\overline{PL}$) is low. Shifting is inhibited as long as $\overline{PL}$ is low. Data is sequentially shifted from complementary outputs, Q_7 and $\overline{Q_7}$, highest-order bit (P7) first. New serial data may be entered via the SERIAL DATA (Ds) input. Serial shifting occurs on the rising edge of CLOCK1 or CLOCK2. Clock inputs may be used separately or together for combined clocking from independent sources. Either clock input may be used also as an active-low clock enable. To prevent double-clocking when a clock input is used as an enable, the enable must be changed to a high level (disabled) only while the clock is high.

Features

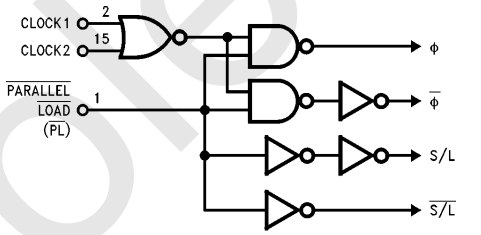
■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Parallel loading independent of clock	
■ Dual clock inputs	
■ Fully static operation	

Connection and Block Diagrams

Dual-In-Line Package



TL/F/5897–1

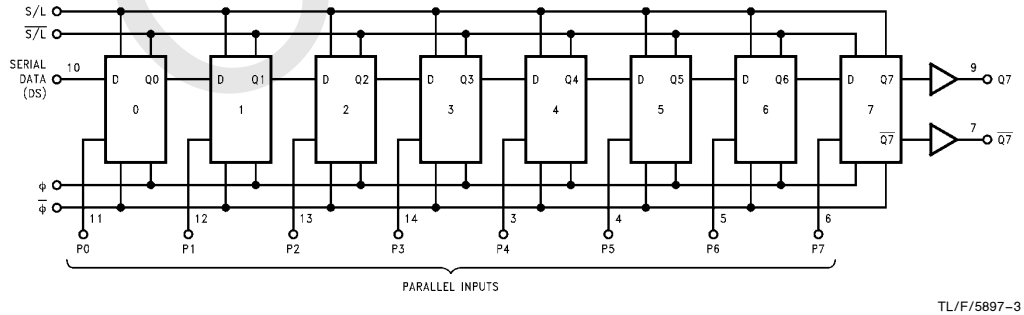


TL/F/5897–2

Order Number MM54C165* or MM74C165*

*Please look into Section 8, Appendix D for availability of various package types.

Top View



TL/F/5897–3

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C165	−55°C to +125°C
MM74C165	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Absolute Maximum V_{CC}	18V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA 74C V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA 74C V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = 0V	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = 0V	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_S	Serial Input Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	25 15		ns ns
t_H	Serial Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_S	Parallel Input Set-Up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_H	Parallel Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		70 30	200 100	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		85 30	180 90	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.5 5	6 12		MHz MHz
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	10 5			μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		65		pF

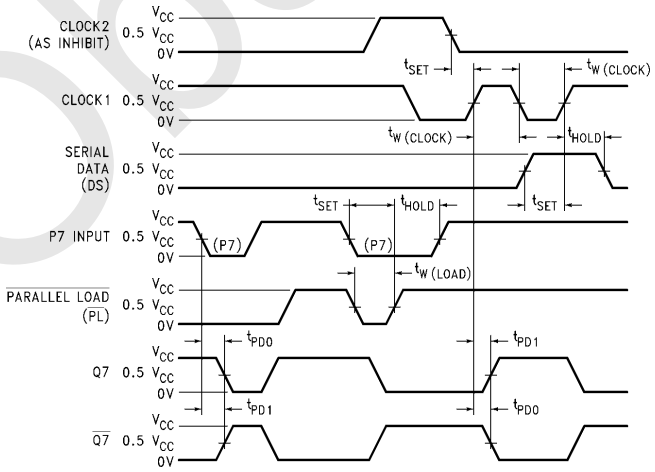
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveform



TL/F/5897–4

Note A: The remaining six data and the serial input are low.

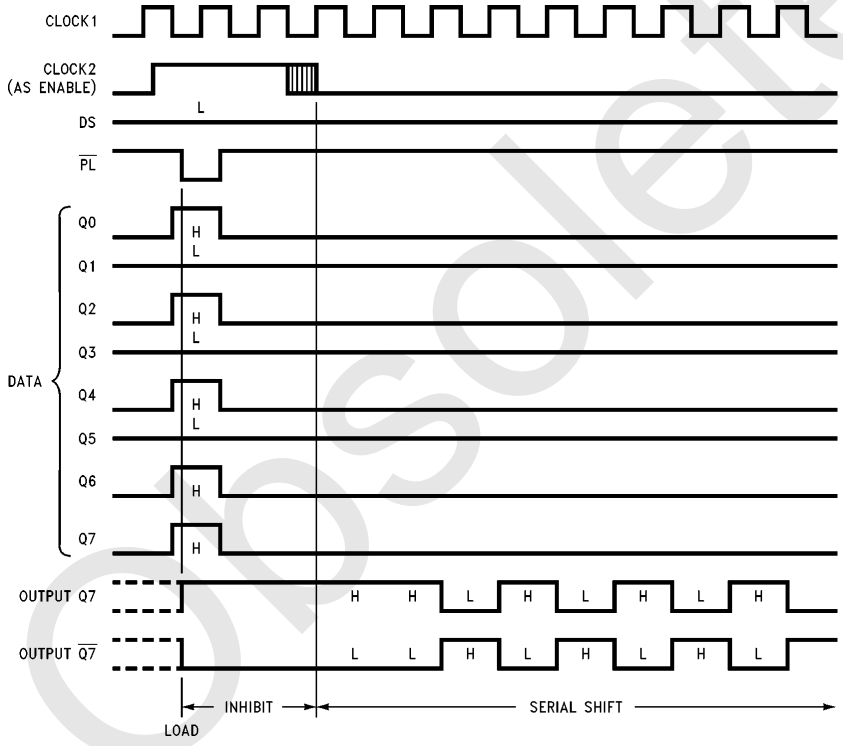
Note B: Prior to test, high level data is loaded into the P7 input.

Truth Table

State	Inputs					Internal		Outputs	
	$\overline{PL}$	Clock1	Clock2 (as enable)	Ds	P0 thru P7	Q0	Q1	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	P0 . . . P7	P0	P1	P7	$\overline{P7}$
Enable	H	L	L	X	X	P0	P1	P7	$\overline{P7}$
Shift (with Ds)	H	↑	L	H	X	H	P0	P6	$\overline{P6}$
Shift (with Ds)	H	↑	L	L	X	L	H	P5	$\overline{P5}$
Hold (Disable)	H	↑	H	X	X	L	H	P5	$\overline{P5}$

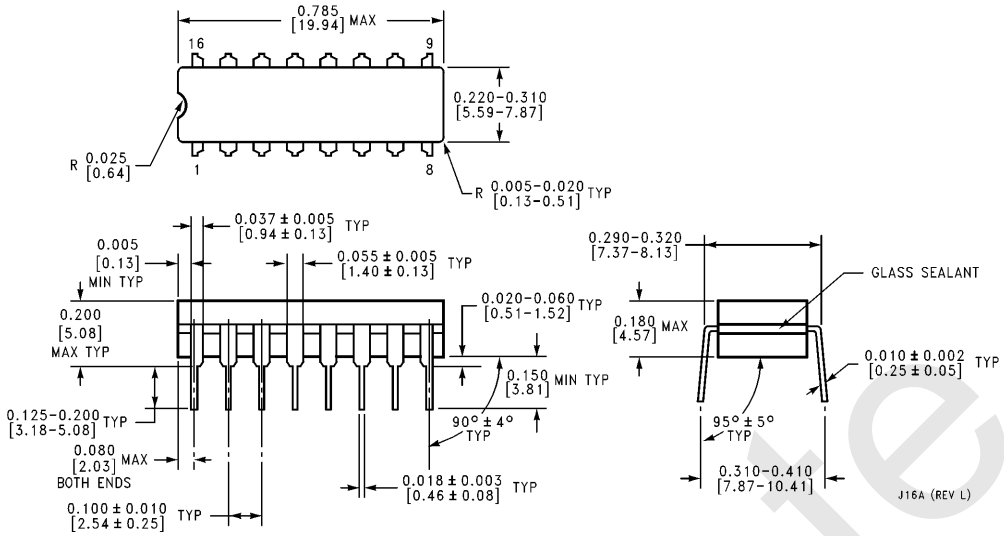
X = don't care
H = $V_{IN(1)}$
L = $V_{IN(0)}$
↑ = clock transition from $V_{IN(0)}$ to $V_{IN(1)}$
P0 thru P7 = data present (and loaded into) parallel inputs
Q0 thru Q6 = Internal flip-flop outputs

Logic Waveform



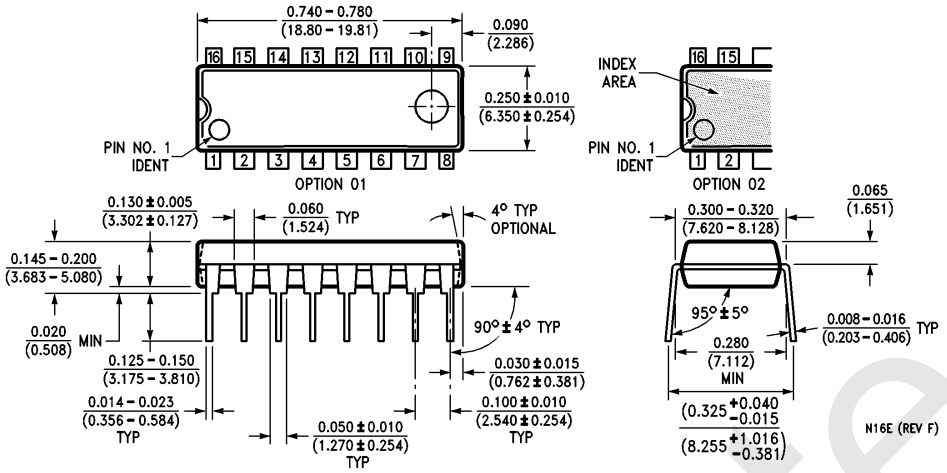
TL/F/5897–5

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C165J or MM74C165J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C165N or MM74C165N
NS Package Number N16E

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