National Semiconductor

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The four D-type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus-organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flops to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive-going transition.

Features

- Supply voltage range   3 V to 15 V
- Tenth power TTL compatible   Drive 2 LPTTL loads
- High noise immunity   0.45 V_{CC} (typ.)
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disable without gating the clock

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic Truth Table and Connection Diagrams
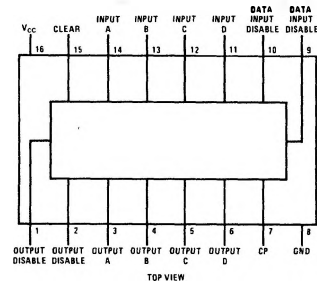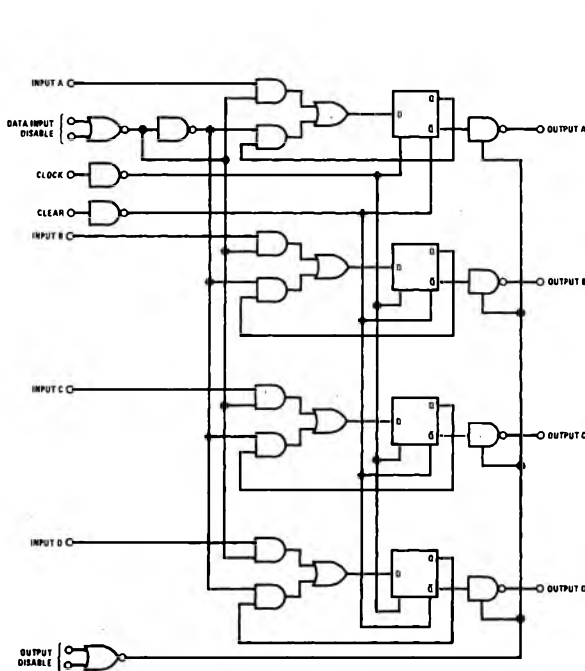
Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC} + 0.3$ V
Operating Temperature Range	
MM54C173	$-55°C$ to $+125°C$
MM74C173	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$ V	3.5			V
		$V_{CC} = 10$ V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$ V			1.5	V
		$V_{CC} = 10$ V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$ V	4.5			V
		$V_{CC} = 10$ V	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$ V,			0.5	V
		$V_{CC} = 10$ V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$ V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		-1.0	-0.005		μA
	Output Current in High Impedance State	$V_{CC} = 15$ V, $V_O = 15$ V		0.001	1.0	μA
		$V_{CC} = 15$ V, $V_O = 0$ V	-1.0	0.001		μA
I_{CC}	Supply Current	$V_{CC} = 15$ V		0.05	300	μA
Low Power TTL/CMOS Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5$ V	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75$ V	$V_{CC} - 1.5$			v
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5$ V			0.8	V
		74C $V_{CC} = 4.75$ V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = -360\mu$A	2.4			V
		74C $V_{CC} = 4.75$ V, $I_O = -360\mu$A	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = 360\mu$A			0.4	V
		74C $V_{CC} = 4.75$ V, $I_O = 360\mu$A			0.4	V
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $T_A = 25°C$		500		ns
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0$ V, $V_{IN(0)} = 0$ V, $T_A = 25°C$, $V_{OUT} = 0$ V	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10$ V, $V_{IN(0)} = 0$ V, $T_A = 25°C$, $V_{OUT} = 0$ V	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0$ V, $V_{IN(1)} = 5.0$ V, $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10$ V, $V_{IN(1)} = 10$ V, $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Output	$V_{CC} = 5.0\,V$		220	400	ns
		$V_{CC} = 10\,V$		80	200	ns
t_S	Input Data Set-up Time	$V_{CC} = 5.0\,V$		40	80	ns
		$V_{CC} = 10\,V$		15	30	ns
t_H	Input Data Hold Time	$V_{CC} = 5.0\,V$	0	0		ns
		$V_{CC} = 10\,V$			0	ns
t_S	Input Disable Set-up Time, $t_{S\ DISS}$	$V_{CC} = 5.0\,V$		100	200	ns
		$V_{CC} = 10\,V$		35	70	ns
t_H	Input Disable Hold Time, $t_{H\ DISS}$	$V_{CC} = 5.0\,V$		0	0	ns
		$V_{CC} = 10\,V$		0	0	ns
t_{1H}, t_{0H}	Delay from Output Disable to High Impedance State (from Logical "1" or Logical "0" Level)	$V_{CC} = 5.0\,V$, $R_L = 10\,k$		170	340	ns
		$V_{CC} = 10\,V$, $R_L = 10\,k$		70	140	ns
t_{H1}	Delay from Output Disable to Logical "1" Level (from High Impedance State)	$V_{CC} = 5.0\,V$		170	340	ns
		$V_{CC} = 10\,V$		70	140	ns
t_{H0}	Delay from Output Disable to Logical "0" Level (from High Impedance State)	$V_{CC} = 5.0\,V$		170	340	ns
		$V_{CC} = 10\,V$		70	140	ns
t_{pd0}, t_{pd1}	Propagation Delay from Clear to Output	$V_{CC} = 5.0\,V$		240	490	ns
		$V_{CC} = 10\,V$		90	180	ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$	3.0	4.0		MHz
		$V_{CC} = 10\,V$	7.0	12		MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$		150		ns
		$V_{CC} = 10\,V$		70		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$		10		μs
		$V_{CC} = 10\,V$		5.0		μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)				

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN–90.

Switching Time Waveforms