# MM54C192,MM54C193,MM74C192,MM74C193

***MM54C192 MM74C192 Synchronous 4-Bit Up/Down Decade Counter MM54C193 MM74C193 Synchronous 4-Bit Up/Down Binary Counter***


Literature Number: SNOS327A

National Semiconductor

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# MM54C192/MM74C192
# Synchronous 4-Bit Up/Down Decade Counter
# MM54C193/MM74C193
# Synchronous 4-Bit Up/Down Binary Counter

## General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters, while the MM54C193 and MM74C193 are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

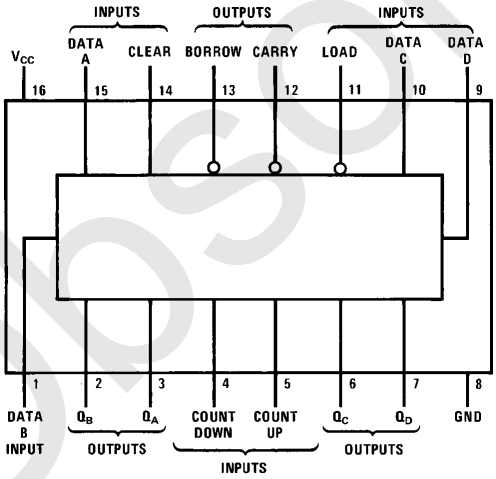
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

## Features

- High noise margin — 1V guaranteed
- Tenth power TTL compatible — Drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 $V_{CC}$ (typ.)

## Connection Diagram

**Dual-In-Line Package**

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**Top View**

**Order Number MM54C192, MM74C192, MM54C193 or MM74C193**



## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $-0.3V$ to $V_{CC} + 0.3V$ |
| Operating Temperature Range ($T_A$) | |
| MM54C154 | $-55°C$ to $+125°C$ |
| MM74C154 | $-40°C$ to $+85°C$ |
| Storage Temperature Range ($T_S$) | $-65°C$ to $+150°C$ |
| Maximum $V_{CC}$ Voltage | 18V |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3V to 15V |
| Lead Temperature ($T_A$) (Soldering, 10 sec.) | 260°C |

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 3.5<br>8.0 | | | V<br>V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | | 1.5<br>2.0 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5V$, $I_O = -10\ \mu A$<br>$V_{CC} = 10V$, $I_O = -10\ \mu A$ | 4.5<br>9.0 | | | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5V$, $I_O = 10\ \mu A$<br>$V_{CC} = 10V$, $I_O = 10\ \mu A$ | | | 0.5<br>1.0 | V<br>V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V$, $V_{IN} = 15V$ | | 0.005 | 1.0 | $\mu A$ |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V$, $V_{IN} = 0V$ | $-1.0$ | $-0.005$ | | $\mu A$ |
| $I_{CC}$ | Supply Current | $V_{CC} = 15V$ | | 0.05 | 300 | $\mu A$ |
| **CMOS TO LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$ | $V_{CC} - 1.5$<br>$V_{CC} - 1.5$ | | | V<br>V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$ | | | 0.8<br>0.8 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C $V_{CC} = 4.5V$, $I_O = -100\ \mu A$<br>74C $V_{CC} = 4.75V$, $I_O = -100\ \mu A$ | 2.4<br>2.4 | | | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C $V_{CC} = 4.5V$, $I_O = 360\ \mu A$<br>74C $V_{CC} = 4.75V$, $I_O = 360\ \mu A$ | | | 0.4<br>0.4 | V<br>V |
| **OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 5V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-1.75$ | | | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 10V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-8$ | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 5V$, $V_{IN(1)} = 5V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 1.75 | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 10V$, $V_{IN(1)} = 10V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 8 | | | mA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation Delay Time to Q from Count Up or Down | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 250<br>100 | 400<br>160 | ns<br>ns |
| $t_{pd}$ | Propagation Delay Time to Q Borrow from Count Down | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 120<br>50 | 200<br>80 | ns<br>ns |
| $t_{pd}$ | Propagation Delay Time to Carry from Count Up | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 120<br>50 | 200<br>80 | ns<br>ns |
| $t_S$ | Time Prior to Load that Data Must be Present | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 100<br>30 | 160<br>50 | ns<br>ns |
| $t_W$ | Minimum Clear Pulse Width | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 300<br>120 | 480<br>190 | ns<br>ns |
| $t_W$ | Minimum Load Pulse Width | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 100<br>40 | 160<br>65 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time to Q from Load | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 300<br>120 | 480<br>190 | ns<br>ns |
| $t_W$ | Minimum Count Pulse Width | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 120<br>35 | 200<br>80 | ns<br>ns |
| $f_{MAX}$ | Maximum Count Frequency | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 2.5<br>6 | 4<br>10 | | MHz<br>MHz |
| $t_r$, $t_f$ | Count Rise and Fall Time | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | | 15<br>5 | $\mu$s<br>$\mu$s |
| $C_{IN}$ | Input Capacitance | (Note 2) | | 5 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 3) | | 100 | | pF |

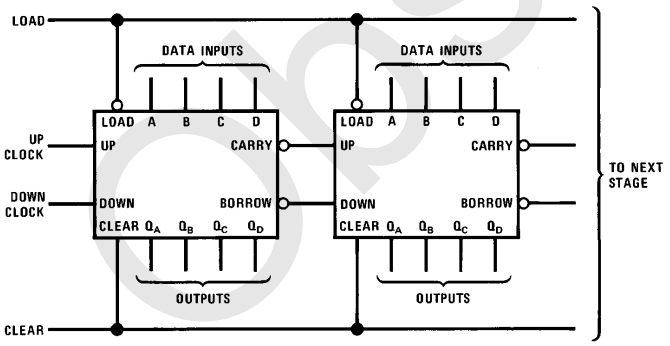
*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

## Cascading Packages

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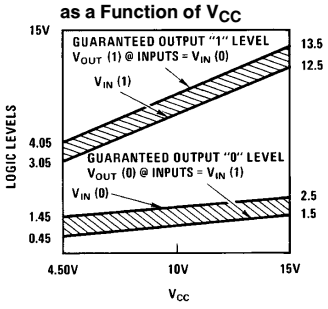
**Guaranteed Noise Margin as a Function of $V_{CC}$**

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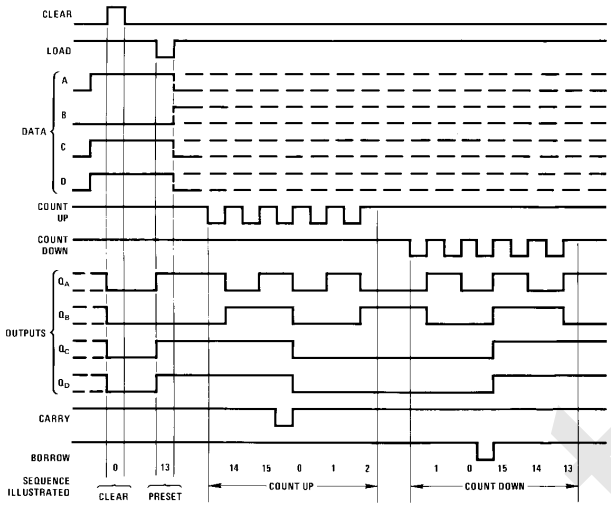
## Timing Diagrams

**MM54C192/MM74C192**

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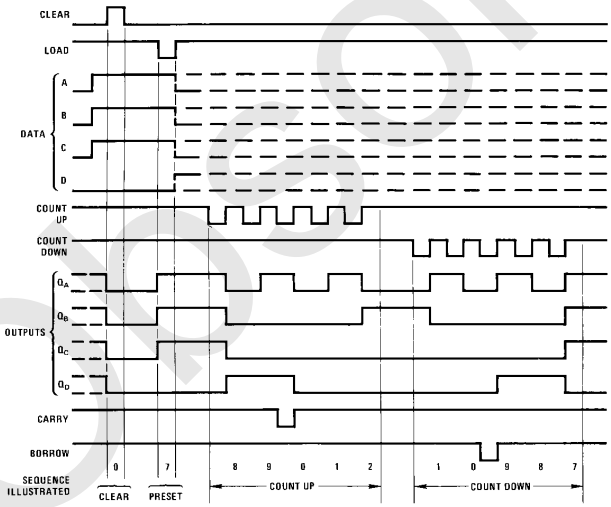
**Note 1:** Clear ouptuts to zero.

**Note 2:** Load (preset) to binary thirteen.

**Note 3:** Count up to fourteen, fifteen, carry, zero, one and two.

**Note 4:** Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

**MM54C193/MM74C193**

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**Note 1:** Clear ouptuts to zero.

**Note 2:** Load (preset) to BCD seven.

**Note 3:** Count up to eight, nine, carry, zero, one, and two.

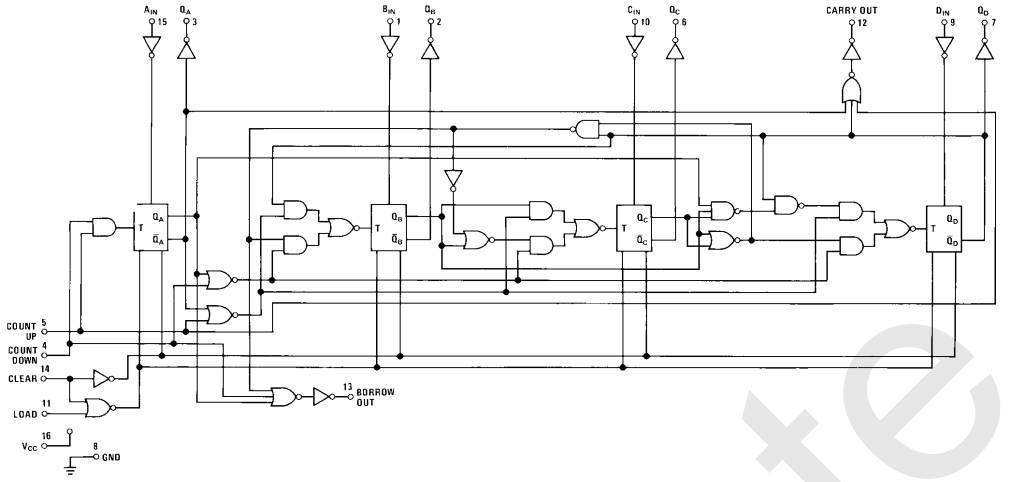
**Note 4:** Count down to one, zero, borrow, nine, eight, and seven.

**Note A:** Clear overrides load, data, and count inputs.

**Note B:** When counting up, count down input must be high; when counting down, count-up input must be high.

## Schematic Diagrams

**MM54C192 Synchronous 4-Bit Up/Down Decade Counter**

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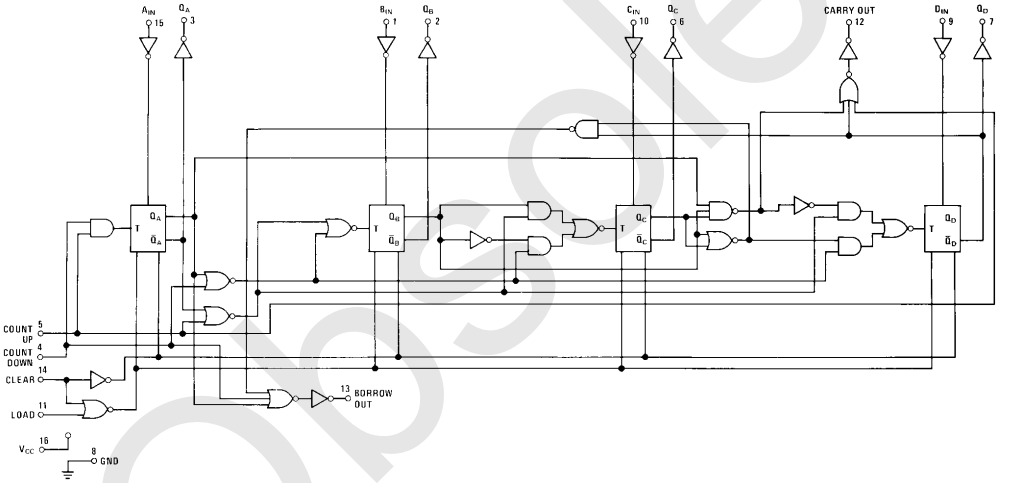
**MM54C193 Synchronous 4-Bit Up/Down Binary Counter**

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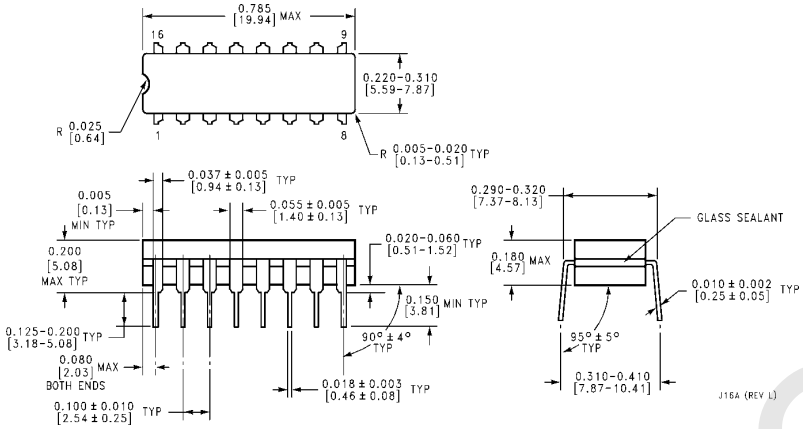
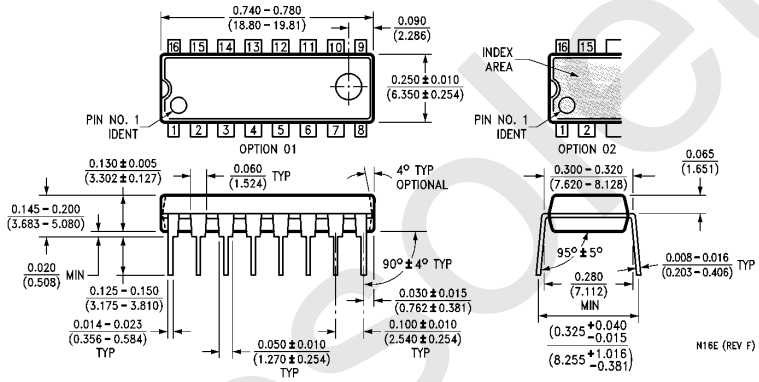
## Physical Dimensions inches (millimeters)




**Ceramic Dual-In-Line Package (J)**
**Order Number MM54C192J, MM74C192J, MM54C193J or MM74C193J**
**NS Package Number J16A**




**Molded Dual-In-Line Package (N)**
**Order Number MM54C192N, MM74C192N, MM54C193N or MM74C193N**
**NS Package Number N16E**



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