MM54C373,MM54C374,MM74C373,MM74C374

MM54C373 MM74C373 TRI-STATE(RM) Octal D-Type Latch MM54C374 MM74C374

TRI-STATE Octal D-Type Flip-Flop

Literature Number: SNOS333A

National Semiconductor

March 1988

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE outputs. These outputs have been specially designed to drive high capacitive loads, such as one might find when driving a bus, and to have a fan out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

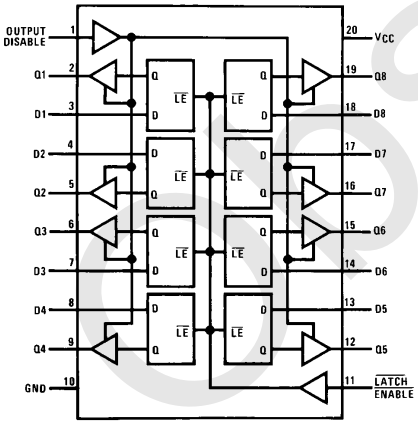
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300″ pin centers.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility — Fan out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/$\overline{\text{LATCH ENABLE}}$ and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300″ centers takes half the board space of a 24-pin package

Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package

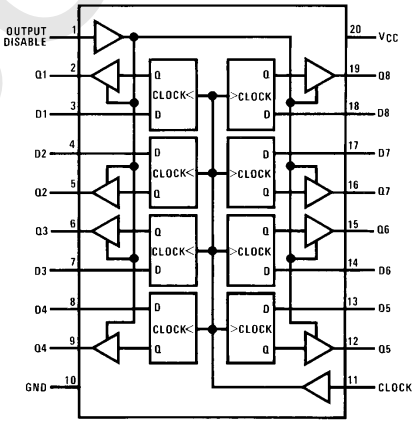


TL/F/5906–1

Top View

Order Number MM54C373 or MM74C373

MM54C374/MM74C374
Dual-In-Line Package



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Top View

Order Number MM54C374 or MM74C374

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	
MM54C373	−55°C to +125°C
MM74C373	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	TRI-STATE Leakage Current	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 54C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA 74C V_{CC} = 4.75V, I_O = −360 μA	V_{CC} − 0.4 V_{CC} − 0.4			V V
		54C V_{CC} = 4.5V, I_O = −1.6 mA 74C V_{CC} = 4.75V, I_O = −1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 1.6 mA 74C V_{CC} = 4.75V, I_O = 1.6 mA			0.4 0.4	V V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C (Note 4)	−12	−24		mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C (Note 4)	−24	−48		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC} T_A = 25°C (Note 4)	6	12		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C (Note 4)	24	48		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics*

MM54C373/MM74C373, $T_A = 25°C$, $C_L = 50$ pF, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output	$V_{CC} = 5V$, $C_L = 50$ pF		165	330	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		195	390	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		85	170	ns
t_{pd0}, t_{pd1}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$				
		$V_{CC} = 5V$, $C_L = 50$ pF		155	310	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		185	370	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		85	170	ns
$t_{SET\text{-}UP}$	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0$ ns				
		$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		35	70	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency	$V_{CC} = 5V$	3.5	6.7		MHz
		$V_{CC} = 10V$	4.5	9.0		MHz
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	V_{CC} 5V		75	150	ns
		$V_{CC} = 10V$		55	110	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	$V_{CC} = 5V$		NA		μs
		$V_{CC} = 10V$		NA		μs
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 5$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		110	220	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		70	140	ns
C_{LE}	Input Capacitance	$\overline{\text{LE}}$ Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		200		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* (Continued)

MM54C374/MM74C374, $T_A = 25°C$, $C_L = 50$ pF, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output	$V_{CC} = 5V$, $C_L = 50$ pF		150	300	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		180	360	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		80	160	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0$ ns				
		$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		35	70	ns
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		50	100	ns
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5V$	3.5	7.0		MHz
		$V_{CC} = 10V$	5	10		MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		110	220	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		70	140	ns
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5V$	15	>2000		μs
		$V_{CC} = 10V$	5	>2000		μs
C_{CLK}	Input Capacitance	CLOCK Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		250		pF

*AC Parameters are guaranteed by DC correlated testing.

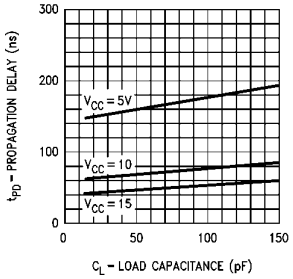
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

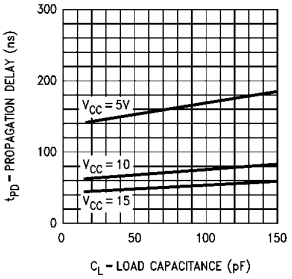
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25°C$

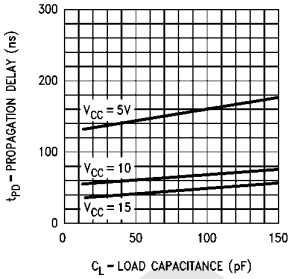
MM54C373/MM74C373 Propagation Delay, $\overline{\text{LATCH}}$ $\overline{\text{ENABLE}}$ to Output vs Load Capacitance



MM54C373/MM74C373 Propagation Delay, Data In to Output vs Load Capacitance

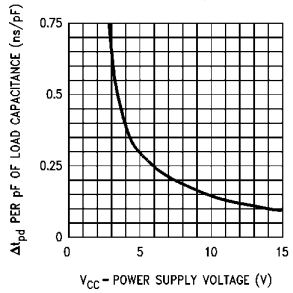


MM54C374/MM74C374 Propagation Delay, CLOCK to Output vs Load Capacitance

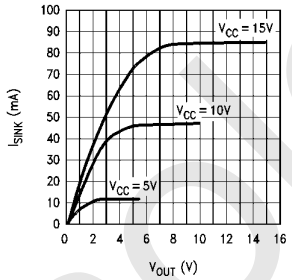


TL/F/5906–3

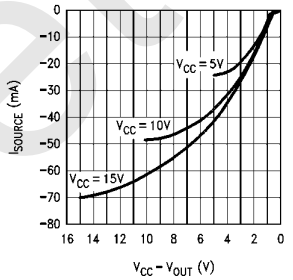
MM54C373/MM74C373, MM54C374/MM74C374 Change in Propagation Delay per pF of Load Capacitance (Δt_{PD}/pF) vs Power Supply Voltage



MM54C373/MM74C373, MM54C374/MM74C374 Output Sink Current vs V_{OUT}



MM54C373/MM74C373, MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



TL/F/5906–4

Truth Table

MM54C373/MM74C373

Output Disable	$\overline{\text{LATCH}}$ $\overline{\text{ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

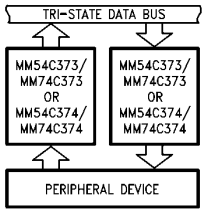
MM54C374/MM74C374

Output Disable	Clock	D	Q
L	⌐/	H	H
L	⌐/	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

L = Low logic level
H = High logic level
X = Irrelevant
⌐/ = Low to high logic level transition
Q = Preexisting output level
Hi-Z = High impedance output state

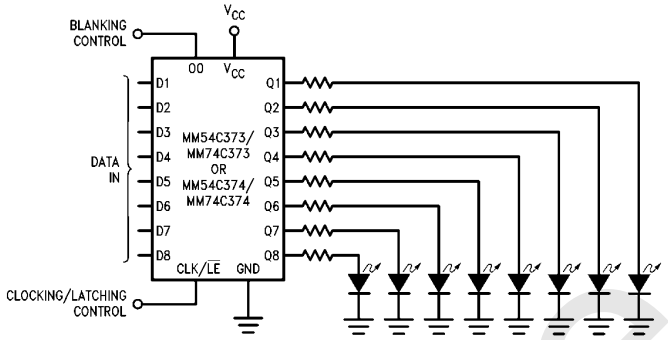
Typical Applications

Data Bus Interfacing Element



TL/F/5906–5

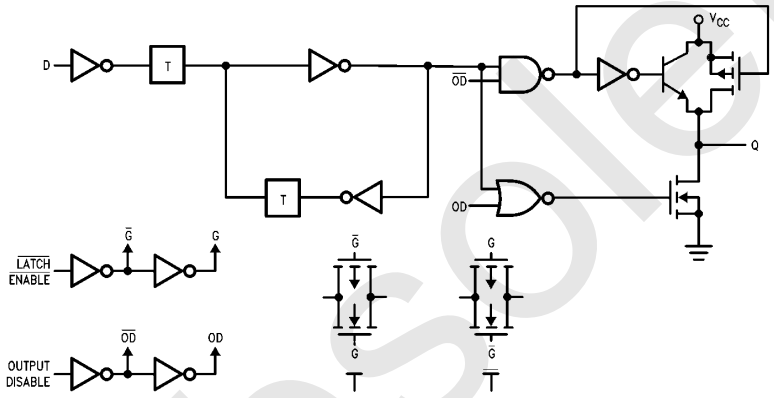
Simple, Latching, Octal, LED Indicator Driver with Blanking for Use as Data Display, Bus Monitor, μP Front Panel Display, Etc.



TL/F/5906–6

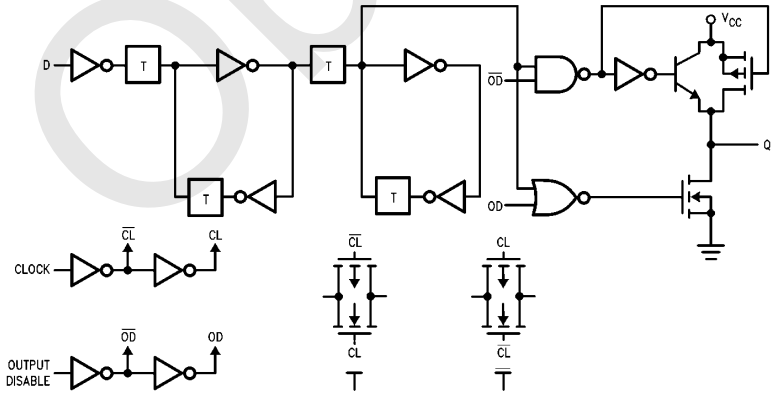
Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)



TL/F/5906–7

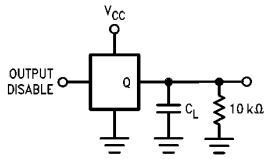
MM54C374/MM74C374 (1 of 8 Flip-Flops)



TL/F/5906–8

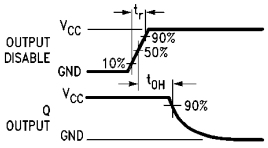
TRI-STATE Test Circuits and Switching Time Waveforms

t_{1H}, t_{H1}

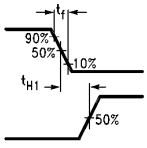


TL/F/5906–9

t_{1H}, C_L = 5 pF

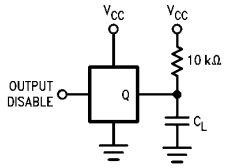


t_{H1}, C_L = 50 pF



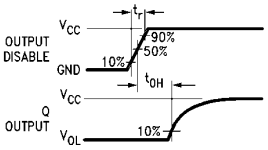
TL/F/5906–10

t_{0H}, t_{H0}

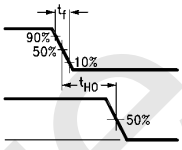


TL/F/5906–11

t_{0H}, C_L = 5 pF



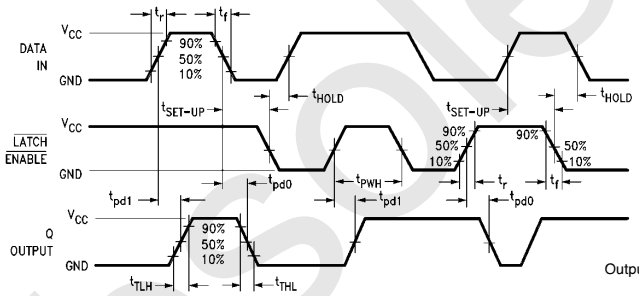
t_{H0}, C_L = 50 pF



TL/F/5906–12

Switching Time Waveforms

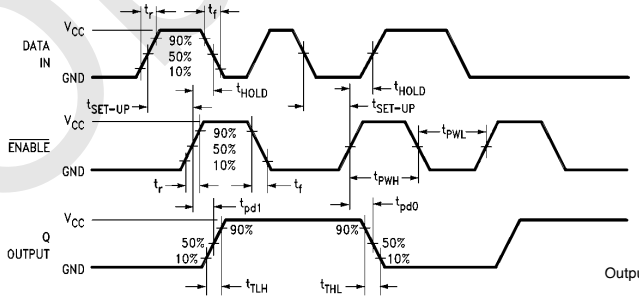
MM54C373/MM74C373



Output Disable = GND

TL/F/5906–13

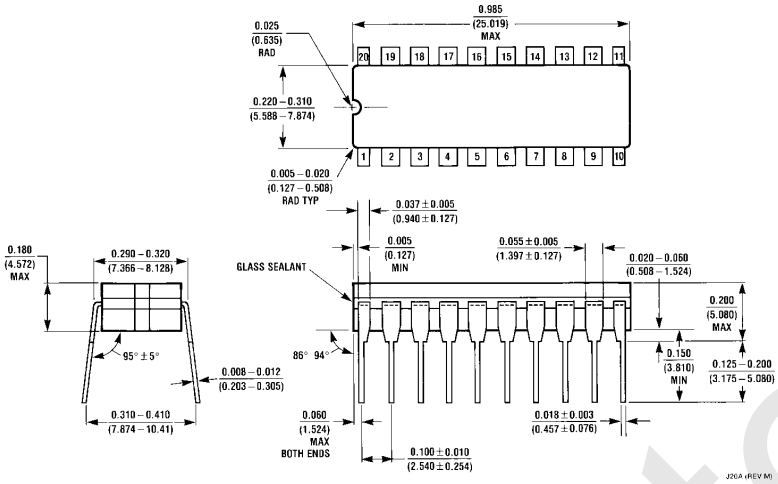
MM54C374/MM74C374



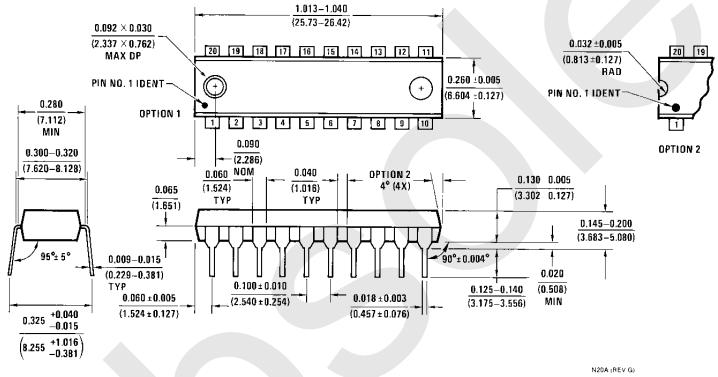
Output Disable = GND

TL/F/5906–14

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C373J, MM54C374J, MM74C373J or MM74C374J
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number MM54C373N, MM54C374N, MM74C373N or MM74C374N
NS Package Number N20A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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