PRELIMINARY

National Semiconductor

MM54C933/MM74C933 Address Bus Comparator

General Description

The MM54C933/MM74C933 Bus Comparator compares two binary words of up to 7 bits in length, and determines whether they are equal (bit for bit). Both enable (EN) inputs must be low to enable the comparison. The output, which is normally high, goes low when inputs A_0–A_6 and B_0–B_6 are equal.

The 'A' set of inputs is provided with latches which allow the inputs to flow through when ALE is high, and are latched when ALE is brought low.

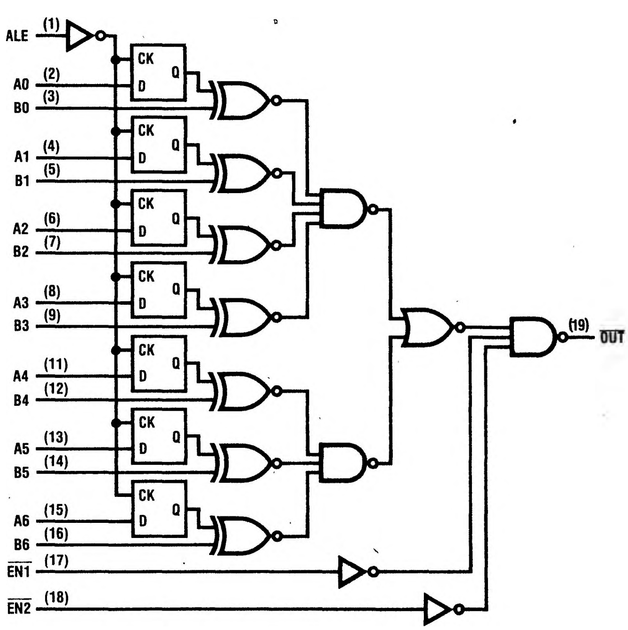
Features

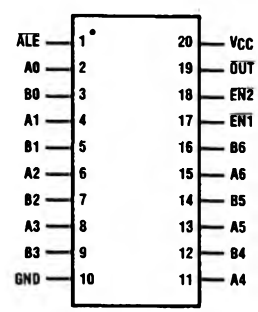
- Silicon Gate CMOS technology used for high speed
- Wide supply voltage range 3-6V
- 2 active low enables for cascading and control
- One set of latched inputs for easy interfacing to multiplexed μP busses
- Active low output compatible with memory and μP peripherals

Typical Applications

- Microprocessor Address/Data Bus decoders
- Equality detectors

Logic and Connection Diagrams





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C933	$-55°C$ to $+125°C$
MM74C933	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
V_{IH}	Input High Voltage	$V_{CC}=5.0V$, $V_{OUT}=0.5V$ or $4.5V$	3.5			V
V_{IL}	Input Low Voltage	$V_{CC}=5.0V$, $V_{OUT}=0.5V$ or $4.5V$			1.5	V
V_{OH}	Output High Voltage	$V_{CC}=5.0V$, $I_O=-1\mu A$ $V_{IN}=0V$ or $5.0V$	4.95			V
V_{OL}	Output Low Voltage	$V_{CC}=5.0V$, $I_O=1\mu A$ $V_{IN}=0V$ or $5.0V$			0.05	V
I_{OH}	Output High Current	$V_{CC}=5.0V$, $V_{IN}=0V$ or $5.0V$ $V_O=4.6V$	-2.0			mA
I_{OL}	Output Low Current	$V_{CC}=5.0V$, $V_{IN}=0V$ or $5.0V$ $V_O=0.4V$	$+2.0$			mA
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=6.0V$, $V_{IN}=V_{CC}$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=6.0V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LSTTL Interface (MM54C933: $V_{CC}=5.0V\pm10\%$, MM74C933: $V_{CC}=5.0V\pm5\%$)					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_O=0.4V$ or $V_{CC}-0.4$ $I_O=\pm10\mu A$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_O=0.4V$ or $V_{CC}-0.4$ $I_O=\pm10\mu A$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{IN}=4.0V$ or $1.0V$ $I_O=-2.0mA$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{IN}=4.0V$ or $1.0V$ $I_O=+2.0mA$			0.4	V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	16			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	16			mA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{PLH}, t_{PHL}	Propagation Delay A to $\overline{OUT}$	ALE = 5.0V, C_L = 15 pF		50		ns
		ALE = 5.0V, C_L = 100 pF		60		ns
t_{PLH}, t_{PHL}	Propagation Delay B to $\overline{OUT}$	C_L = 15 pF		40		ns
		C_L = 100 pF		50		ns
t_{PLH}, t_{PHL}	Propagation Delay $\overline{EN1}$ or $\overline{EN2}$ to $\overline{OUT}$	C_L = 15 pF		10		ns
		C_L = 100 pF		20		ns
t_{PLH}, t_{PHL}	Propagation Delay ALE to $\overline{OUT}$	C_L = 15 pF		30		ns
		C_L = 100 pF		40		ns
t_S	Time prior to ALE that A must be present			5.0		ns
t_H	Time after ALE that A must be present			5.0		ns
t_W	Minimum ALE Pulse Width			10		ns
t_T	Output Transition Time	C_L = 15 pF		10		ns
C_{IN}	Input Capacitance	(Note 2)		10		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines that no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Truth Tables

$\overline{EN1}$ or $\overline{EN2}$	A_N	B_N	$\overline{OUT}$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	X	X	1

ALE	Function
0	A_N Inputs Latched
1	A_N Inputs Flow-Through

Switching Time Waveforms