

# MM54C157,MM74C157

*MM54C157 MM74C157 Quad 2-Input Multiplexers*



Literature Number: SNOS321A

## MM54C157/MM74C157 Quad 2-Input Multiplexers

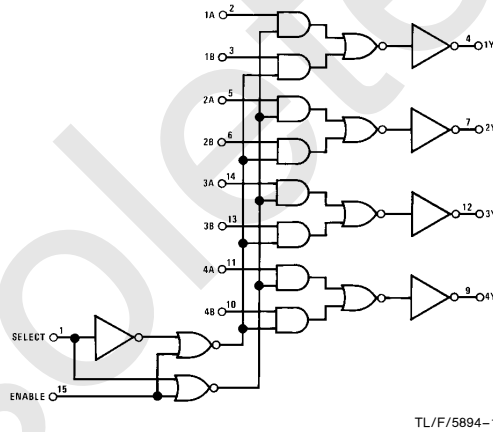
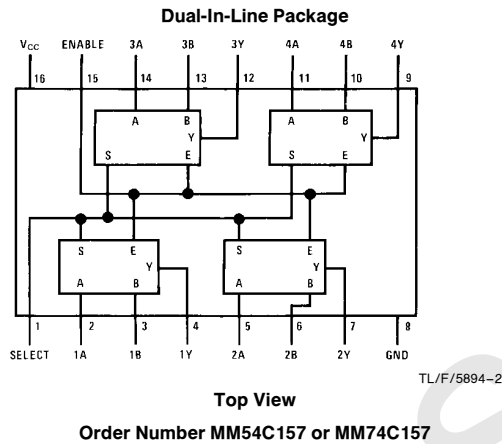
### General Description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

### Features

- Supply voltage range 3V to 15V
- High noise immunity 0.45 V<sub>CC</sub> (typ.)
- Low power 50 nW (typ.)
- Tenth power TTL compatible Drive 2 LPTTL loads

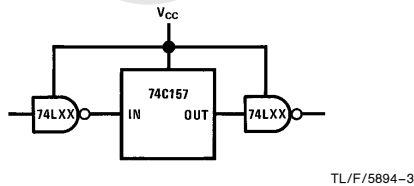
### Logic & Connection Diagrams



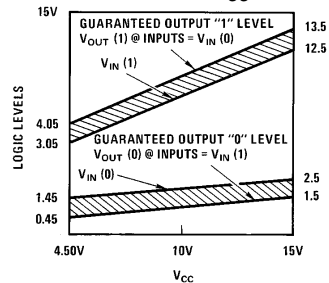
### Truth Table

Enable	Select	A	B	Output Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

### 74L Compatibility



### Guaranteed Noise Margin as a Function of V<sub>CC</sub>



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
MM54C157	-40°C to +85°C
MM74C157	

Storage Temperature Range	-65°C to +150°C
Maximum $V_{CC}$ Voltage	18V
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating $V_{CC}$ Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	260°C

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0	-0.005		$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	60	$\mu A$

## CMOS TO TENTH POWER INTERFACE

$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -360 \mu A$ 74C $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 360 \mu A$ 74C $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4 0.4	V V

## OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)

$I_{SOURCE}$	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75			mA
$I_{SOURCE}$	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8.0			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	1.75			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	8.0			mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**AC Electrical Characteristics\***  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0}$ , $t_{pd1}$	Propagation Delay from Data to Output	$V_{CC} = 5.0\text{V}$		150	250	ns
		$V_{CC} = 10\text{V}$		70	110	ns
$t_{pd0}$ , $t_{pd1}$	Propagation Delay from Select to Output	$V_{CC} = 5\text{V}$		180	300	ns
		$V_{CC} = 10\text{V}$		80	130	ns
$t_{pd0}$ , $t_{pd1}$	Propagation Delay from Enable to Output	$V_{CC} = 5\text{V}$		180	300	ns
		$V_{CC} = 10\text{V}$		80	130	ns
$C_{IN}$	Input Capacitance	(Note 2)		5		pF
$C_{PD}$	Power Dissipation Capacitance	(Note 3)		20		pF

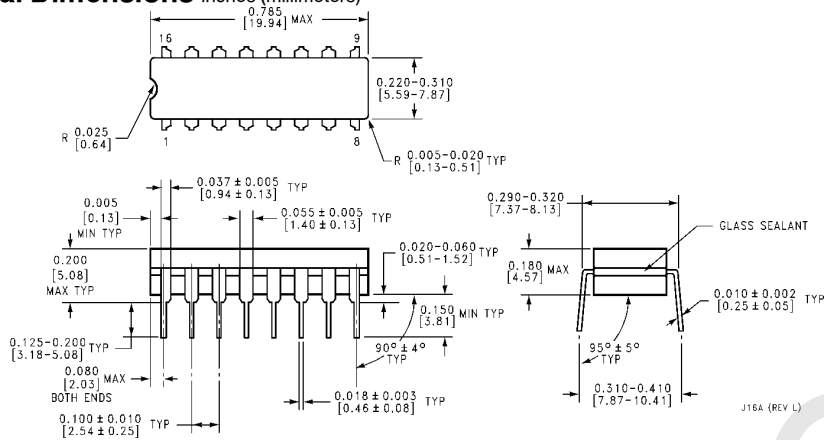
\*AC Parameters are guaranteed by DC correlated testing.

**Note 2:** Capacitance is guaranteed by periodic testing.

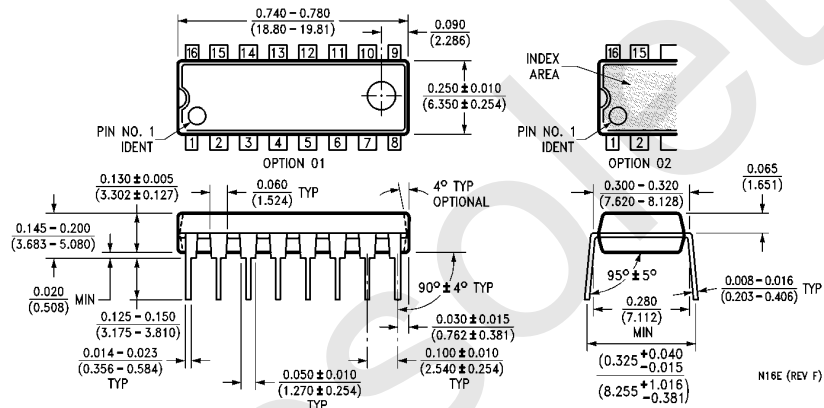
**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

Obsolete

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54C157J or MM74C157J**  
**NS Package Number J16A**



**Molded Dual-In-Line Package (N)**  
**Order Number MM54C157N or MM74C157N**  
**NS Package Number N16E**

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