National Semiconductor

MM54C165/MM74C165 Parallel-Load 8-bit Shift Register

General Description

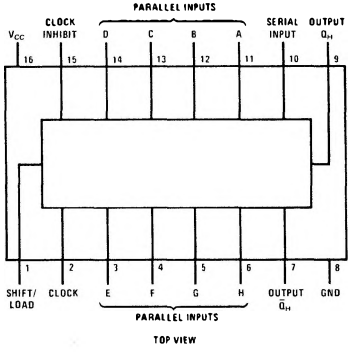
The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Features

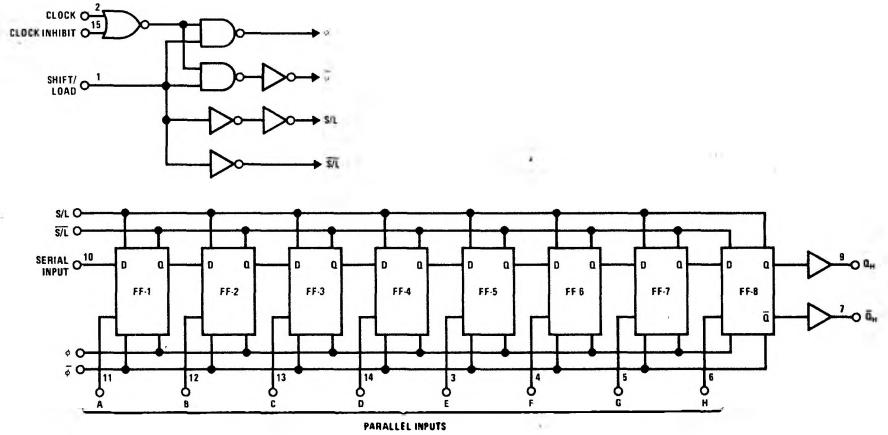
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Direct overriding load	
■ Gated clock inputs	
■ Fully static operation	

Connection Diagram



TOP VIEW

Block Diagrams



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC} + 0.3\,V$
Operating Temperature Range	
MM54C165	$-55°C$ to $+125°C$
MM74C165	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Absolute Maximum V_{CC}	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = -10\,\mu A$ $V_{CC} = 10\,V$, $I_O = -10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0\,V$, $I_O = +10\,\mu A$ $V_{CC} = 10\,V$, $I_O = +10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15\,V$, $V_{IN} = 0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15\,V$		0.05	300	μA
	CMOS to LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5\,V$ 74C $V_{CC} = 4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = -360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = -360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5\,V$, $I_O = 360\,\mu A$ 74C $V_{CC} = 4.75\,V$, $I_O = 360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10\,V$ $T_A = 25°C$, $V_{OUT} = 0\,V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10\,V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

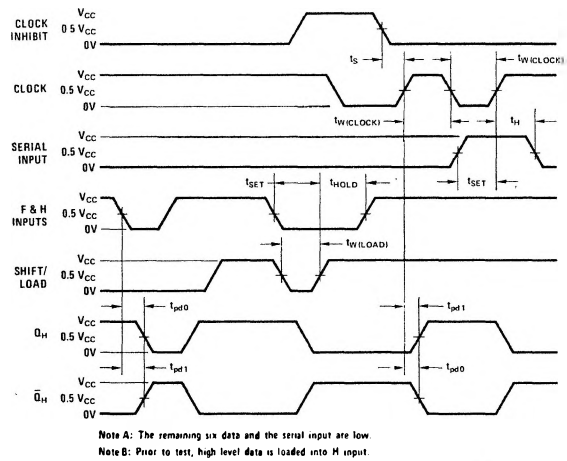
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_S	Serial Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	25 15		ns ns
t_H	Serial Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_S	Parallel Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_H	Parallel Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		70 30	200 100	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		85 30	180 90	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.5 5.0	6.0 12		MHz MHz
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	10 5.0			μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



Note A: The remaining six data and the serial input are low.

Note B: Prior to test, high level data is loaded into H input.

Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{BG}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$

X = irrelevant

↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$

a . . . h = the level at data inputs A thru H

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock

Logic Waveforms