



## MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

### General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of  $\overline{CE}_3$ . The TRI-STATE data output line, working in conjunction with  $\overline{CE}_1$  or  $\overline{CE}_2$  inputs, provides for easy memory expansion.

**Address Operation:** Address inputs must be stable  $t_{SA}$  prior to the positive to negative transition of  $\overline{CE}_3$ . It is therefore unnecessary to hold address information stable for more than  $t_{HA}$  after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the  $\overline{CE}_3$  must occur for the memory to be selected.

**Read Operation:** The data is read out by selecting the proper address and bringing  $\overline{CE}_3$  low and  $\overline{WE}$  high.

Holding either  $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  at a high level forces the output into TRI-STATE. When used in bus-organized systems,  $\overline{CE}_1$ , or  $\overline{CE}_2$ , a TRI-STATE control provides for fast access times by not totally disabling the chip.

**Write Operation:** Data is written into the memory with  $\overline{CE}_3$  low and  $\overline{WE}$  low. The state of  $\overline{CE}_1$  or  $\overline{CE}_2$  has no effect on the write cycle. The output assumes TRI-STATE with  $\overline{WE}$  low.

### Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45  $V_{CC}$  (typ.)
- TTL compatibility fan out of 1 driving standard TTL
- Low power 500 nW (typ.)
- Internal address register

See page 4-7  
for detailed  
specifications