Technical Data

MMM5062/D
Rev. 3, 9/2002

Quad-Band GSM GPRS
3.5 V Power Amplifier

MOTOROLA
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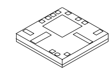
MMM5062



(Scale 1:1)

Package Information
Plastic Package
Case 1383
(Module, 7x7 mm)

Ordering Information

Device	Device Marking	Package
MMM5062	See Figure 30	Module

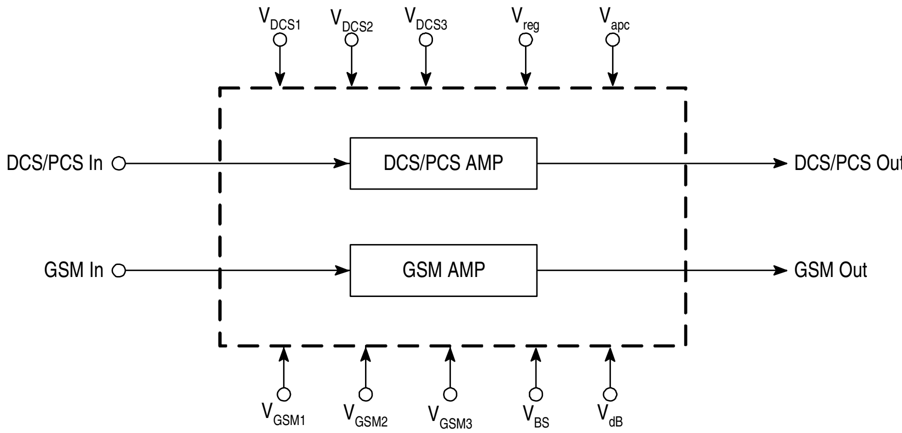
The MMM5062 is a quad-band single supply RF Power Amplifier for GSM850/GSM900/DCS1800/PCS1900 GPRS handheld radios. This fully integrated Power Amplifier uses a patented concept to realize the 50 Ω matching on-chip through integration of passives on the GaAs die. This allows module functionality in a very small 7 x 7 mm package and achieves best-in-class Power Amplifier performance and multi-band capability.

Applications:

- Quad-Band GSM850/900 DCS1800 and PCS1900
- Guaranteed for Class 10 GPRS

Features:

- Single Supply Enhancement Mode GaAs MESFET Technology
- Internal 50 Ω Input/Output Matching
- High Gain Three Stage Amplifier Design
- Typical 3.5 V Characteristics:
  - P_{out} = 35.5 dBm, PAE = 50% for GSM850
  - P_{out} = 35.2 dBm, PAE = 53% for GSM900
  - P_{out} = 33.8 dBm, PAE = 44% for DCS
  - P_{out} = 34 dBm, PAE = 43% for PCS
- Optimized and Guaranteed for Open-Loop Power Control Applications
- Small 7 x 7 mm Package



This device contains 26 active transistors.

Figure 1. Simplified Block Diagram

1 Electrical Specifications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	$V_{GSM1,2,3}$, $V_{DCS1,2,3}$, V_{dB}	6.0	V
RF Input Power	GSM IN, DCS/PCS IN	10	dBm
RF Output Power GSM Section DCS/PCS Section	 GSM OUT DCS/PCS OUT	 38 36	dBm
Operating Case Temperature Range	T_C	-35 to 100	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Die Temperature	T_J	150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤150 V and Machine Model (MM) ≤50 V. Additional ESD data available upon request.
3. Meets Moisture Sensitivity Level (MSL) 3. See Figure 30 on page 19 for additional details.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{GSM1,2,3}$, $V_{DCS1,2,3}$	2.7	-	5.5	V
Bias Supply Voltage	V_{dB}	2.7	-	5.5	V
Regulated Voltage	V_{REG}	2.5	2.8	3.0	V
Power Control Voltage	V_{apc}	0	1.8	2.8	V
Band Select	V_{BS}	0	2.8	3.0	V
Input Power GSM850/900	GSM IN	-1.0	-	8.0	dBm
Input Power DCS/PCS	DCS/PCS IN	2.0	-	10	dBm

Table 3. Control Requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Current for V_{reg} @ 2.8 V	I_{reg}	-	7.7	10	mA
Band Select Low Band Enable Voltage High Band Enable Voltage	V_{BS}	 2.2 0	 2.8 -	 - 0.3	V
Current for V_{BS} = 2.8 V	I_{BS}	-	0.76	1.0	mA

Table 4. Electrical Characteristics

(Peak measurement at 25% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GSM 850 Section(P_{in} = -1.0 dBm, $V_{GSM1,2,3}$ = 3.5 V pulsed, V_{dB} = 3.5 V, V_{REG} = V_{BS}= 2.8 V, V_{ramp} = 1.8 V pulsed)					
Frequency Range	BW	824	-	849	MHz
Output Power	P_{out}	34.5	35.5	-	dBm
Power Added Efficiency	PAE	42	50	-	%
Output Power @ Low Voltage ($V_{GSM1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	P_{out}	33	33.8	-	dBm
Power Added Efficiency @ Low Voltage ($V_{GSM1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	PAE	43	51	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		 - -	 -35 -60	 -30 -45	dBc
Second Harmonic Leakage at DCS Output		-	-25	-15	dBm

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Return Loss	$\|S_{11}\|$	-	13	-	dB
Output Power Isolation (V_{ramp} = 0 V, $V_{GSM1,2,3}$ = 0 V)	P_{off}	-	-45	-40	dBm
Noise Power in Rx Band @ P_{in} = -1.0 dBm (100 kHz measurement bandwidth) @ f_o + 20 MHz f_o = 849 MHz	NP	-	-83	-	dBm
Noise Power in Rx Band @ P_{in} = 6.0 dBm (100 kHz measurement bandwidth) @ f_o + 20 MHz f_o = 849 MHz	NP	-	-86	-82	dBm
Stability-Spurious Output (P_{out} = 5.0 to 35 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress (P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			
GSM 900 Section(P_{in} = -1.0 dBm, $V_{GSM1,2,3}$ = 3.5 V pulsed, V_{dB} = 3.5 V, V_{REG} = V_{BS}= 2.8 V, V_{ramp} = 1.8 V pulsed)					
Frequency Range	BW	880	-	915	MHz
Output Power	P_{out}	34.2	35.2	-	dBm
Power Added Efficiency	PAE	48	53	-	%
Output Power @ Low Voltage ($V_{GSM1,2,3}$ = 2.8 V pulsed, V_{dB} = 2.8 V)	P_{out}	32.5	33.4	-	dBm
Power Added Efficiency @ Low Voltage ($V_{GSM1,2,3}$ = 2.8 V pulsed, V_{dB} = 2.8 V)	PAE	48	54	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		 - -	 -37 -60	 -33 -45	dBc
Second Harmonic Leakage at DCS Output (Crosstalk isolation)		-	-28	-15	dBm
Input Return Loss	$\|S_{11}\|$	-	10	-	dB
Output Power Isolation (V_{ramp} = 0 V, $V_{GSM1,2,3}$ = 0 V)	P_{off}	-	-45	-40	dBm
Noise Power in Rx Band @ P_{in} = -1.0 dBm (100 kHz measurement bandwidth) @ f_o + 10 MHz (f_o = 915 MHz) @ f_o + 20 MHz (f_o = 915 MHz)	NP	 - -	 -80 -81	 - -	dBm
Noise Power in Rx Band @ P_{in} = 6.0 dBm (100 kHz measurement bandwidth) @ f_o + 10 MHz (f_o = 915 MHz) @ f_o + 20 MHz (f_o = 915 MHz)	NP	 - -	 -84 -86	 -77 -81	dBm

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Stability-Spurious Output (P_{out} = 5.0 to 35 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress (P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			
DCS Section(P_{in} = 2.0 dBm, $V_{DCS1,2,3}$ = 3.5 V pulsed, V_{dB} = 3.5 V, V_{REG} = 2.8 V, V_{ramp} = 1.8 V pulsed, V_{BS} = 0 V)					
Frequency Range	BW	1710	-	1785	MHz
Output Power	P_{out}	32.5	33.8	-	dBm
Power Added Efficiency	PAE	38	44	-	%
Output Power @ Low Voltage ($V_{DCS1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{DCS1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	PAE	38	45	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		 - -	 -65 -50	 -45 -45	dBc
Input Return Loss	$\|S_{11}\|$	-	9.0	-	dB
Output Power Isolation (V_{ramp} = 0 V, $V_{DCS1,2,3}$ = 0 V)	P_{off}	-	-40	-35	dBm
Noise Power in Rx Band @ P_{in} = 2.0 dBm @ f_o + 20 MHz (f_o = 1785 MHz) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output (P_{out} = 0 to 33 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress (P_{out} = 0 to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			
PCS Section(P_{in} = 3.0 dBm, $V_{DCS1,2,3}$ = 3.5 V pulsed, V_{dB} = 3.5 V, V_{REG} = 2.8 V, V_{ramp} = 1.8 V pulsed, V_{BS} = 0 V)					
Frequency Range	BW	1850	-	1910	MHz
Output Power	P_{out}	32.5	34	-	dBm
Power Added Efficiency	PAE	37	43	-	%
Output Power @ Low Voltage ($V_{DCS1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{DCS1,2,3}$ = 2.8 V pulsed, V_{dB}= 2.8 V)	PAE	37	43	-	%

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Harmonic Output $2f_o$ $\geq 3f_o$		 - -	 -65 -50	 -45 -45	dBc
Input Return Loss	$\lvert S_{11} \rvert$	-	5.0	-	dB
Output Power Isolation (V_{ramp} = 0 V, $V_{DCS1,2,3}$ = 0 V)	P_{off}	-	-35	-32	dBm
Noise Power in Rx Band @ P_{in} = 3.0 dBm @ f_o + 20 MHz (f_o = 1910 MHz) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output (P_{out} = 0 to 33 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress (P_{out} = 0 to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

2 Typical Performance Characteristics

2.1 GSM850

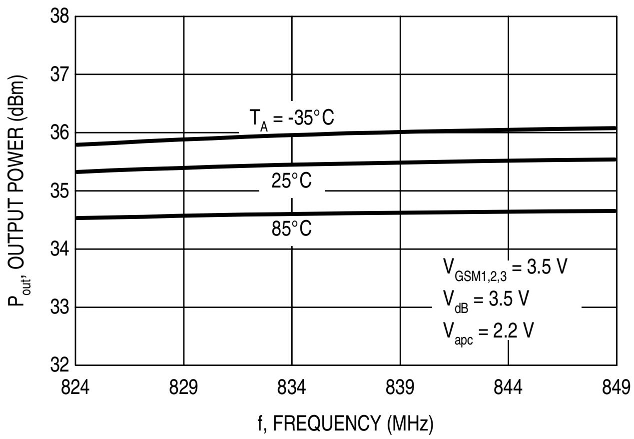


Figure 2. Output Power versus Frequency

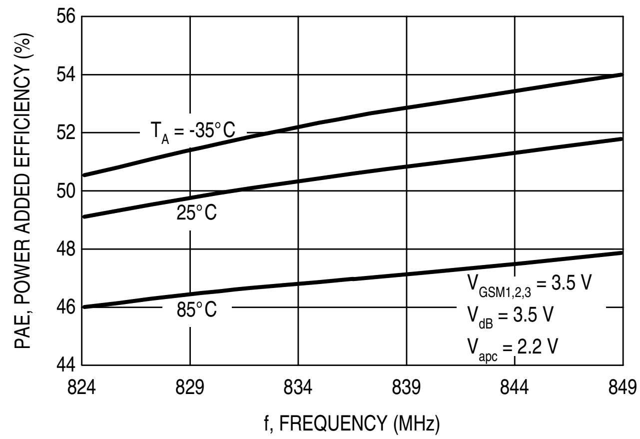


Figure 3. Power Added Efficiency versus Frequency

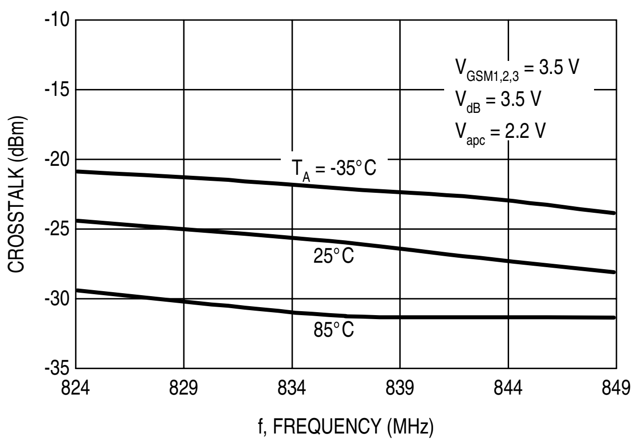


Figure 4. Crosstalk versus Frequency

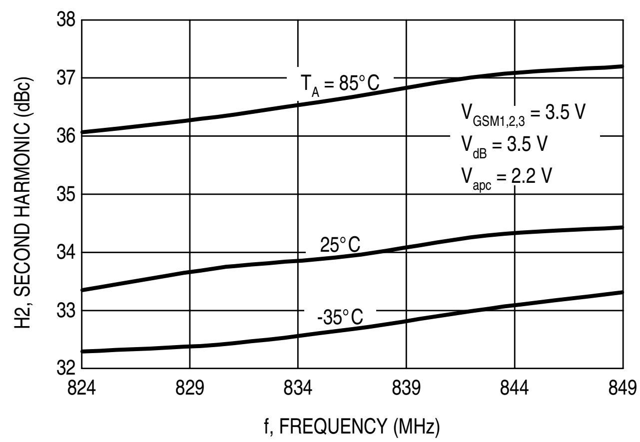


Figure 5. Second Harmonic Output versus Frequency

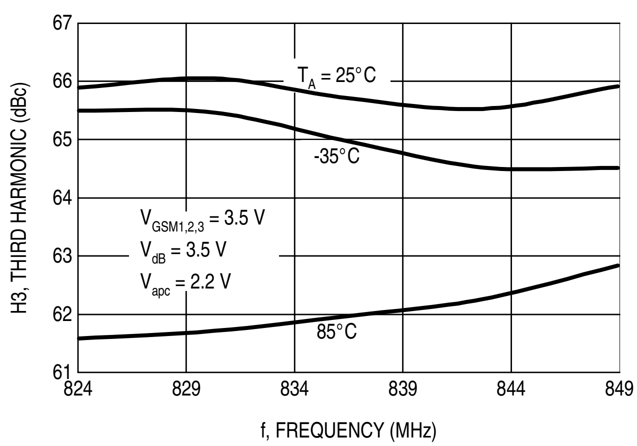


Figure 6. Third Harmonic Outputversus Frequency

2.2 GSM900

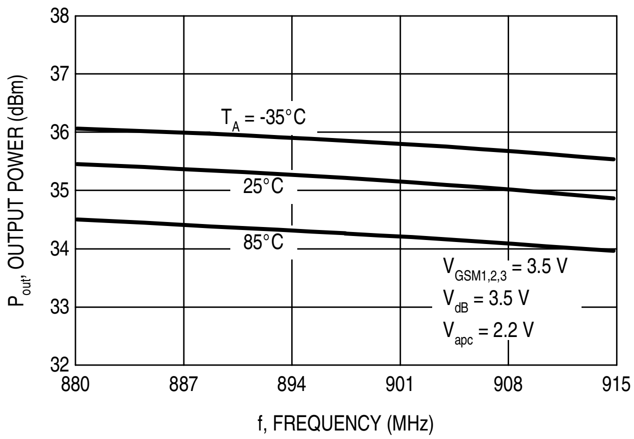


Figure 7. Output Power versus Frequency

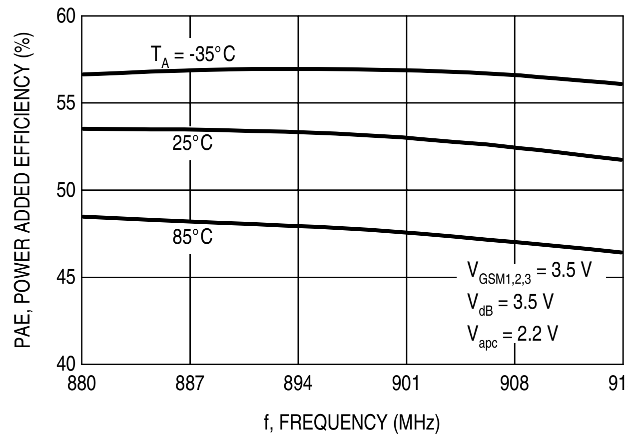


Figure 8. Power Added Efficiency versus Frequency

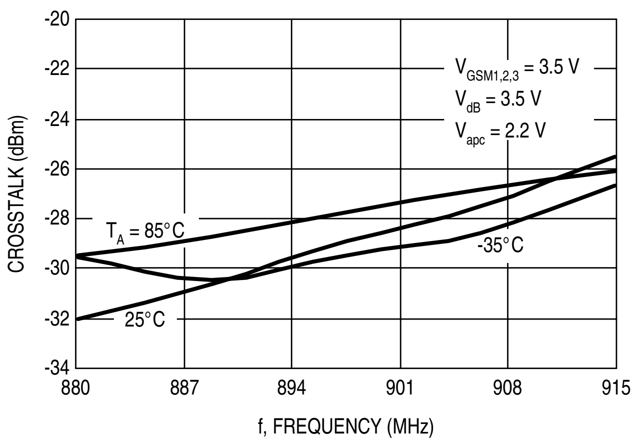


Figure 9. Crosstalk versus Frequency

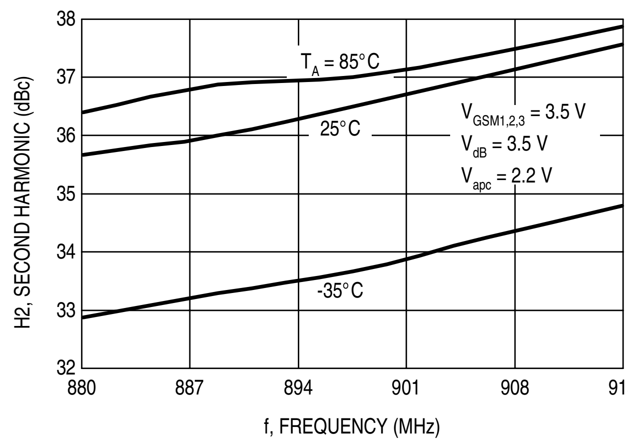


Figure 10. Second Harmonic Output versus Frequency

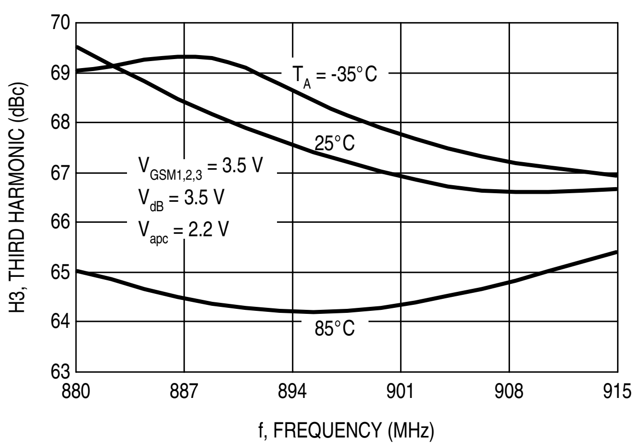


Figure 11. Third Harmonic Output versus Frequency

2.3 DCS

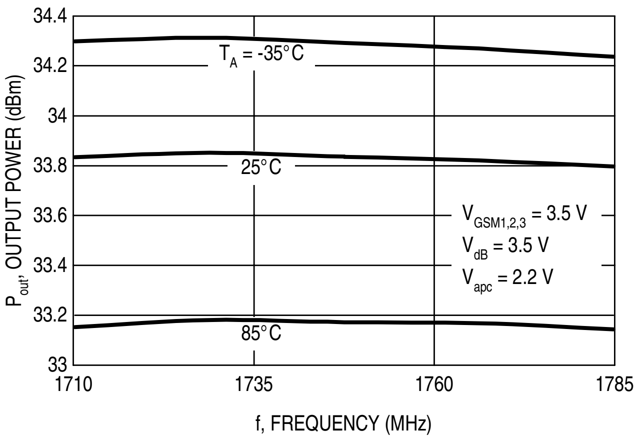


Figure 12. Output Power versus Frequency

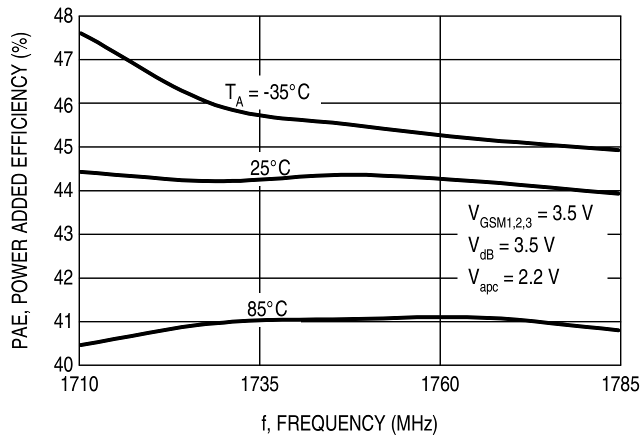


Figure 13. Power Added Efficiency versus Frequency

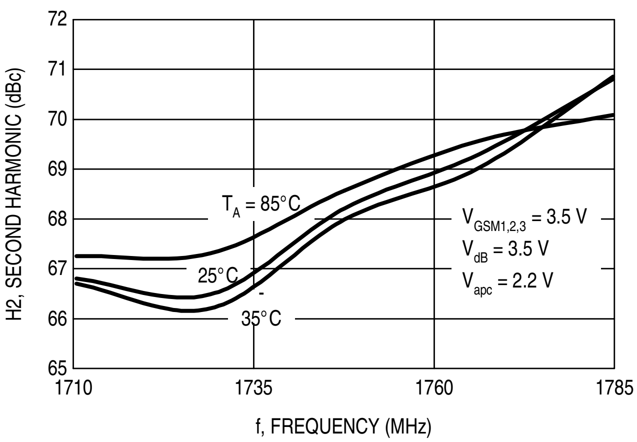


Figure 14. Second Harmonic Output versus Frequency

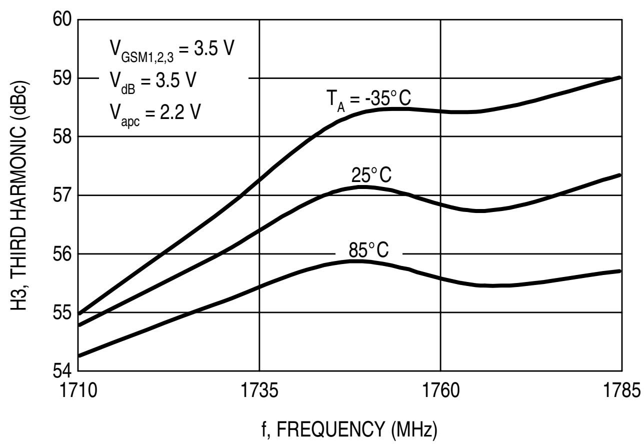


Figure 15. Third Harmonic Output versus Frequency

2.4 PCS

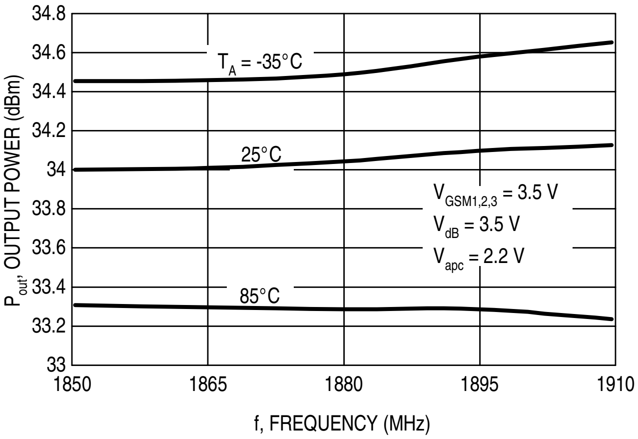


Figure 16. Output Power versus Frequency

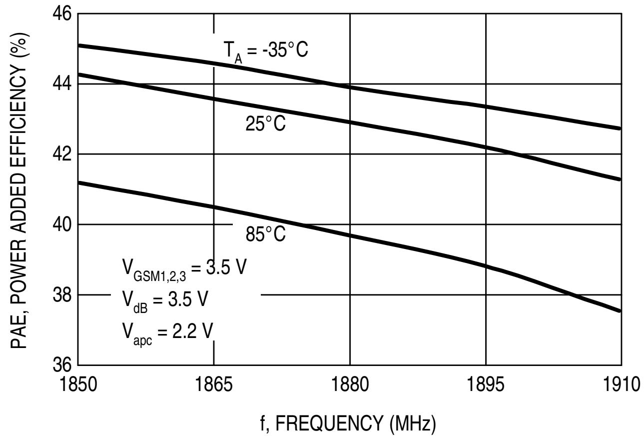


Figure 17. Power Added Efficiency versus Frequency

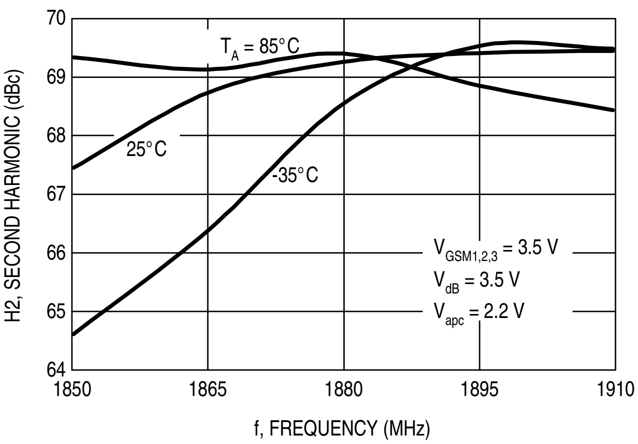


Figure 18. Second Harmonic Output versus Frequency

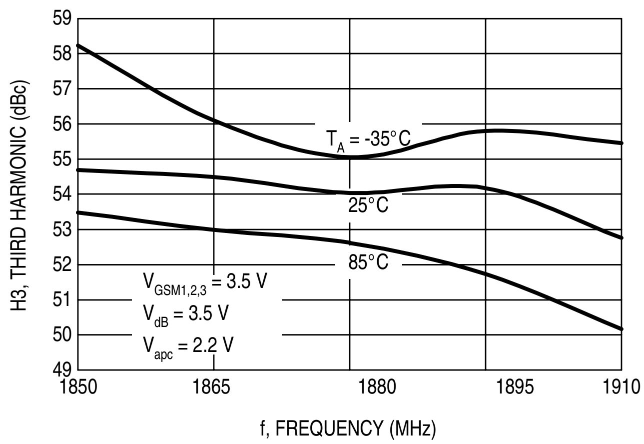
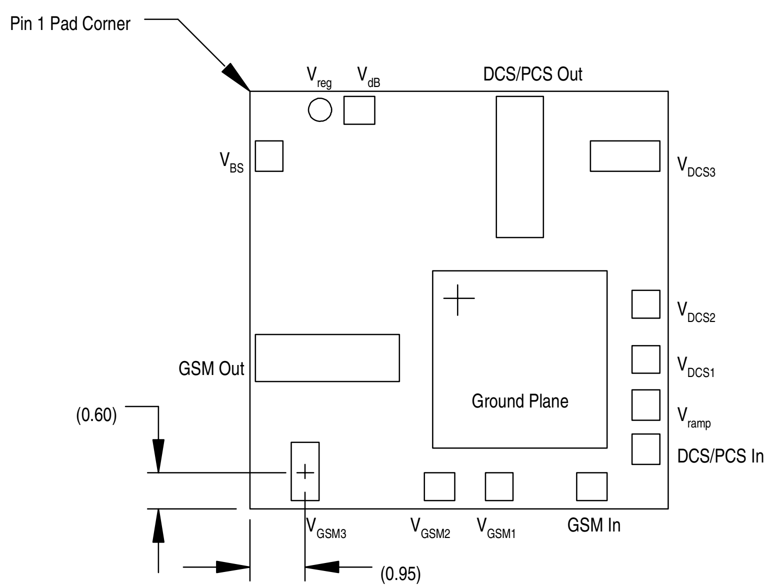


Figure 19. Third Harmonic Output versus Frequency

3 Pin Descriptions and Connections

Table 5. Pin Function Description

Pin	Symbol	Description
1	V_{reg}	Regulated dc voltage for bias circuit
2	V_{dB}	DC supply voltage for active bias circuits connected to the battery
3	DCS/PCS Out	DCS/PCS RF output
4	V_{DCS3}	DCS/PCS DC supply voltage for 3rd stage
5	V_{DCS2}	DCS/PCS DC supply voltage for 2nd stage
6	V_{DCS1}	DCS/PCS DC supply voltage for 1st stage
7	V_{apc}	Power control for both line-ups (V_{apc} = 0 V, $P_{out} = P_{off}$, V_{apc} = 1.8 V, $P_{out} = P_{max}$)
8	DCS/PCS In	DCS/PCS RF input
9	GSM In	GSM850/GSM900 RF input
10	V_{GSM1}	GSM850/GSM900 DC supply voltage for 1st stage
11	V_{GSM2}	GSM850/GSM900 DC supply voltage for 2nd stage
12	V_{GSM3}	GSM850/GSM900 DC supply voltage for 3rd stage
13	GSM Out	GSM850/GSM900 RF output
14	V_{BS}	Band selection between GSM850/GSM900 and DCS/PCS



NOTE: For optimum performance V_{GSM1} and V_{GSM2}, as well as V_{DCS1} and V_{DCS2}, must be strapped together on the application demobard.

Figure 20. Pin Connections
(Bottom View)

4 Application Information

4.1 Power Control Considerations

The MMM5062 is designed for open loop (drain control) applications. A PMOS FET is used to switch the MMM5062 drain and vary the supply voltage from 0 to the battery voltage setting (V_{bat}). The simplified concept schematic (see Figure 27) describes the application circuit used to control the device through the drain voltage.

A drain control provides a linear transfer function which is repeatable versus control voltage (see Figure 21).

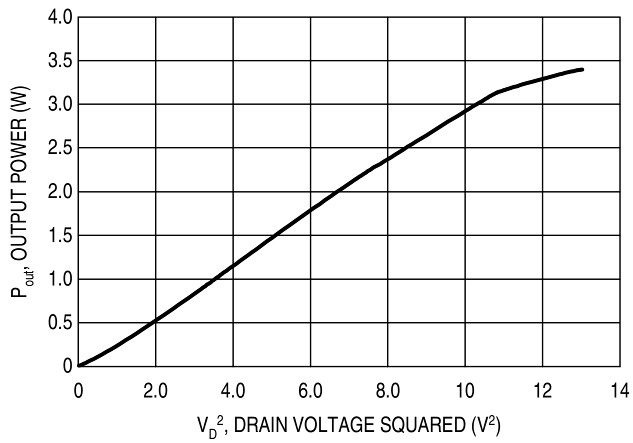


Figure 21. Output Power versus Drain Voltage

4.2 GSM Second Harmonic (H2) Trap Circuitry

When transmitting in GSM saturated mode, the second harmonic is naturally present at the RF output of the PA and reaches the antenna after additional filtering in the front-end. ETSI specifies that harmonic level cannot exceed -36 dBm. In order to improve H2 rejection in low Band (GSM850/GSM900), an H2 trap has been developed. The topology is based on a Low Pass π Cell Filter (see Figure 22) where the first shunt capacitor is actually part of the PA output match.

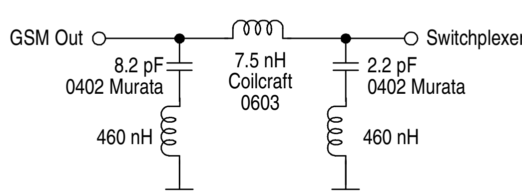
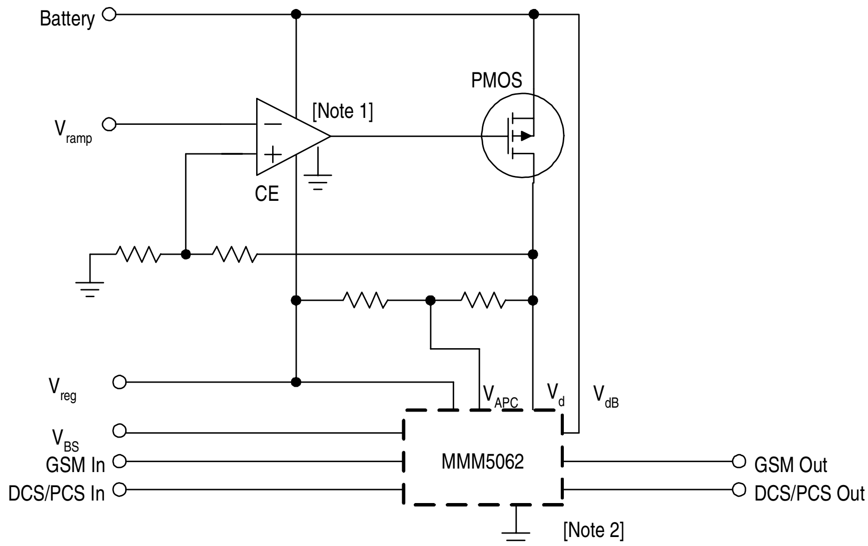


Figure 22. Low Pass Filter

This circuit reduces H2 level by 7 to 8 dB with low in-band insertion losses (mainly due to the series inductor). Moreover, this structure can be used to match Power amplifier module output to the switchplexer.

4.3 Application Schematics and Printed Circuit Boards



NOTES: 1. Op/Amp is either external (with an enable pin CE) or in an ASIC.
2. The MMM5062 requires 4 to 6 RF/LF decoupling capacitors (not shown).

Figure 23. Open Loop Control Application Schematic

Figure 23 represents the complete Power Amplifier implementation including the MMM5062 Amplifier Module and the Control Circuitry. This functionality is realized with two separate printed circuit boards; the PA Evaluation Circuit with schematic shown in Figure 26 and PCB Layout shown in Figure 28, and the Power Amplifier Control Loop with schematic shown in Figure 27 and PCB Layout shown in Figure 29.

The PA Evaluation Circuit is straightfoward and, due to the MMM5062's high level of integration, requires only a few passive components around the package. These components are mainly de-coupling capacitors.

The Power Amplifier Control Loop is based on an operational amplifier driving a PMOS transistor. The PMOS device functions as a linear drain voltage regulator controlled by $V_{ramp}$with a typical gain of 2 which is set through the resistive divider R4 and R5 as shown in Figure 27. To control output power through the drain, V_{apc} must be indexed to the drain voltage to prevent the PA Section from drawing excessive current especially at low output power. Nevertheless, V_{apc} should stay above 0.8 V to provide sufficient gain for the line-up. Figure 24 describes the application circuit used to control V_{apc} through the drain voltage. It uses V_{reg} to pre-position V_{apc} at 0.9 V and add a voltage which is dependent on the drain Voltage.

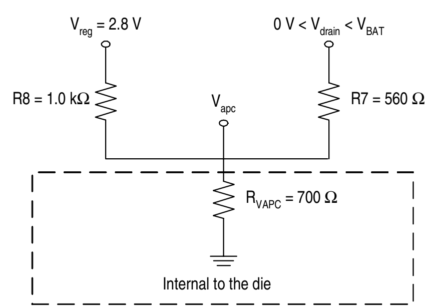


Figure 24.

R8 and R_{Vapc} set V_{apc} at 0.9 V while R7 sets the V_{apc} slope. V_{apc} versus V_{drain} is shown in the Figure 25.

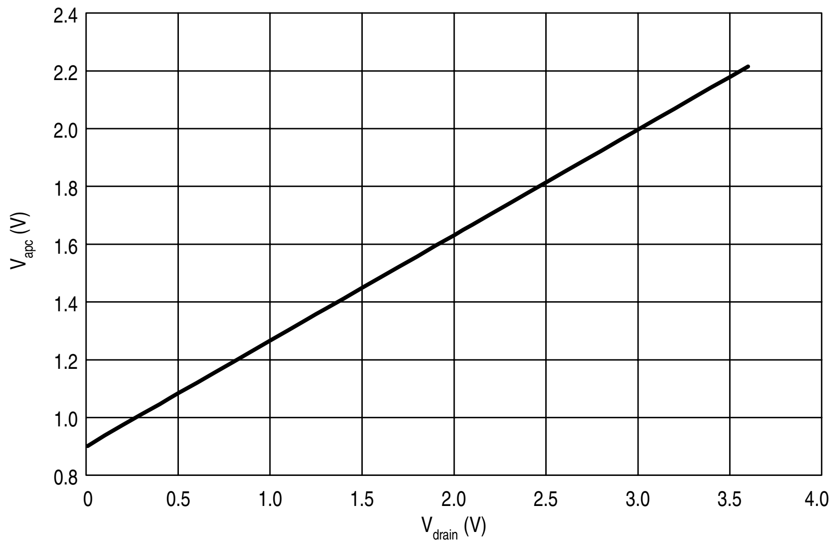


Figure 25. V_{apc} versus V_{drain}

It is possible that the Power Control DAC output voltage can be in the 200 mV to 2.0 V range. This raises a concern for the MMM5062 ramp control voltage (V_{ramp}) which must start at 0 V to get enough output power dynamic range. To overcome this limitation, a resistor (R6 in Figure 27) is used to set an additional offset (200 mV with R6 = 39 kΩ). This residual voltage is then subtracted the DAC output voltage through the differential Operational Amplifier.

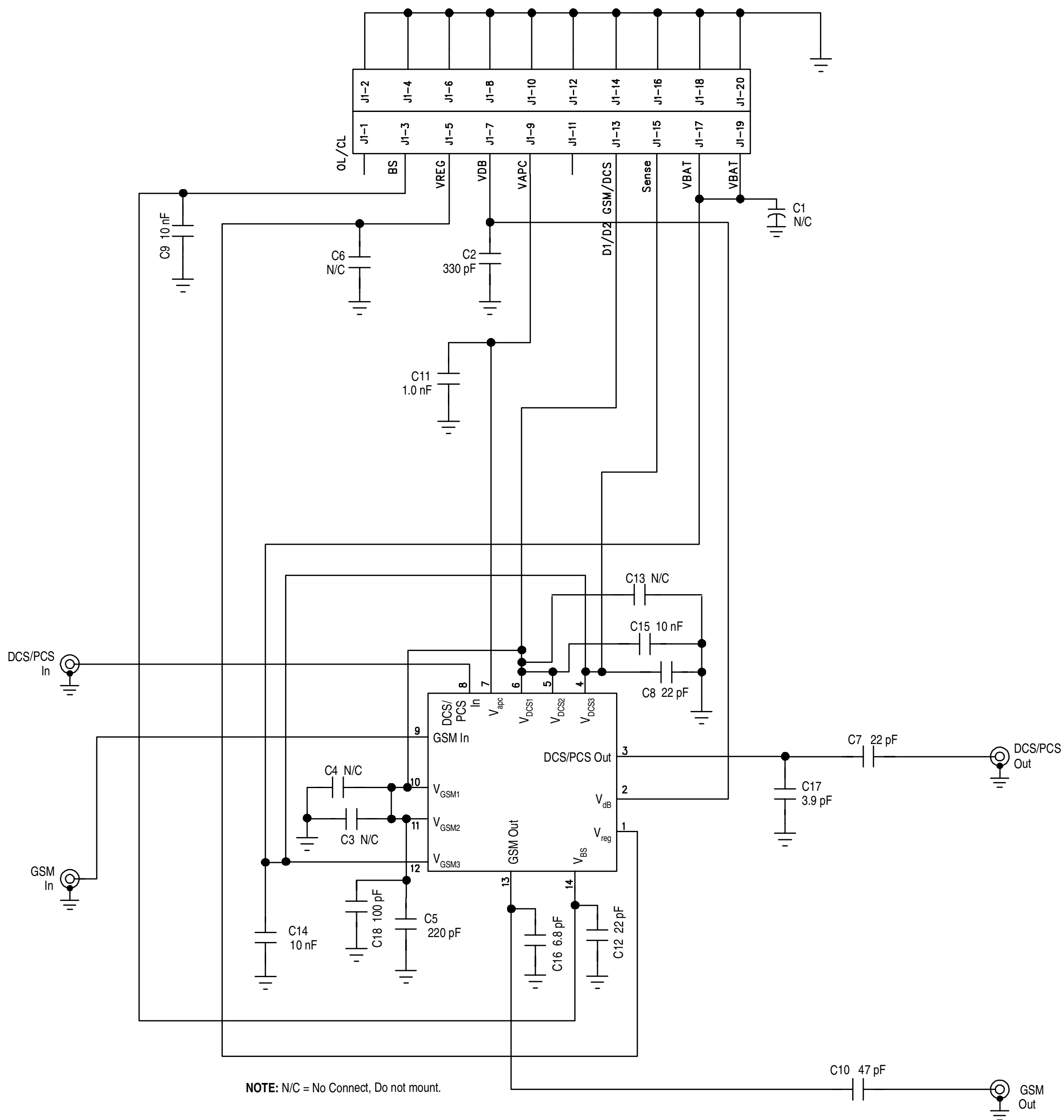


Figure 26. PA Evaluation Circuit

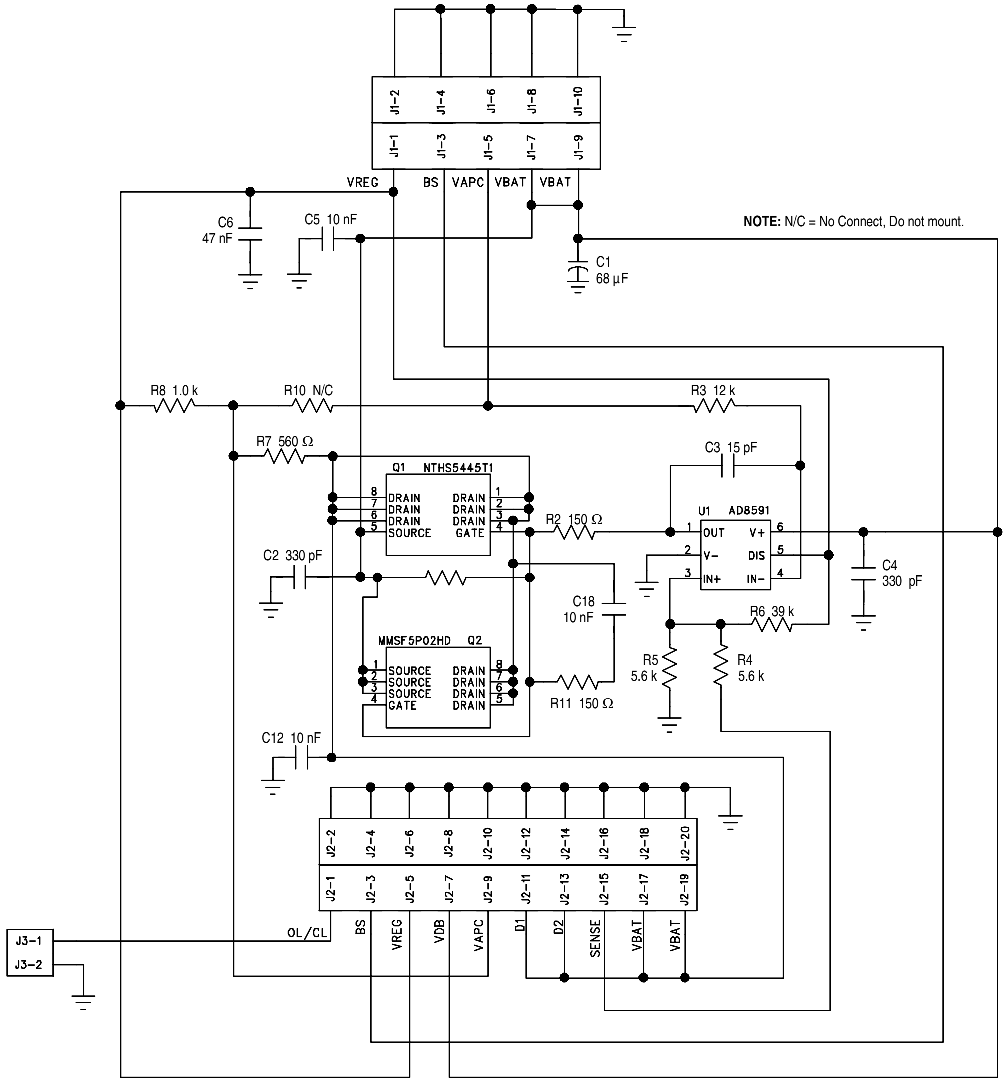


Figure 27. Power Amplifier Control Loop

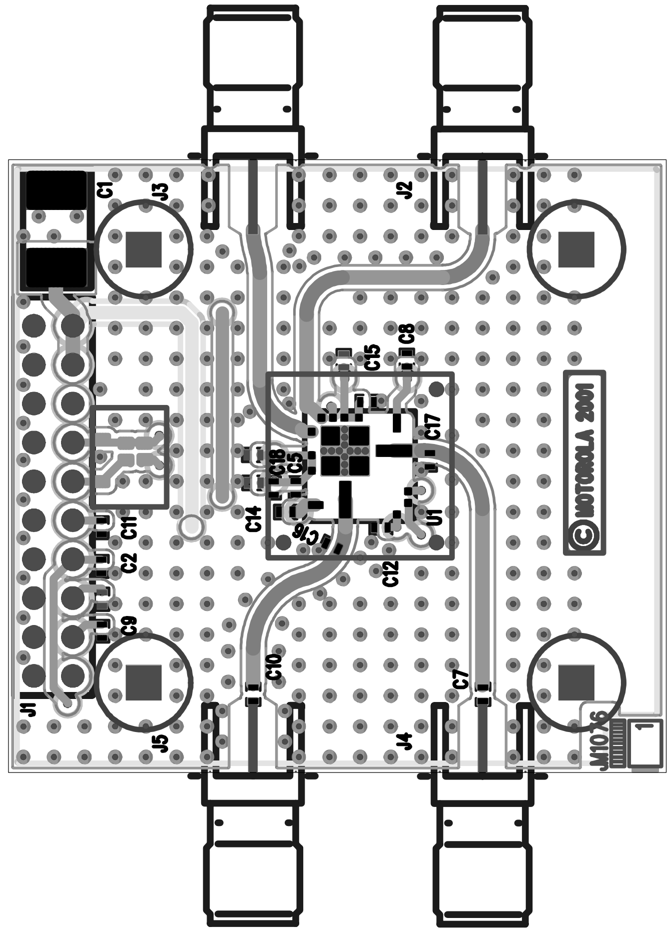


Figure 28. PA Evaluation Circuit PCB

Table 6. PA Evaluation Circuit PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1, C3, C4, C6, C13	N/C - Do not mount		
C2	330 pF	GRM36COG330J50	Murata
C5	220 pF	GRM36X7R221K50	Murata
C7, C8, C12	22 pF	GRM36COG220J50	Murata
C9, C14, C15	10 nF	GRM36X7R103K25	Murata
C10	47 pF	GRM36COG470J50	Murata
C11	1.0 nF	GRM36X7R102K25	Murata
C16	6.8 pF	GRM36COG6R8J50	Murata
C17	3.9 pF	GRM36COG3R9J50	Murata
C18	100 nF	GRM36X7R104K25	Murata
J2, J3, J4, J5	50 Ω	142-0711-821	Johnson

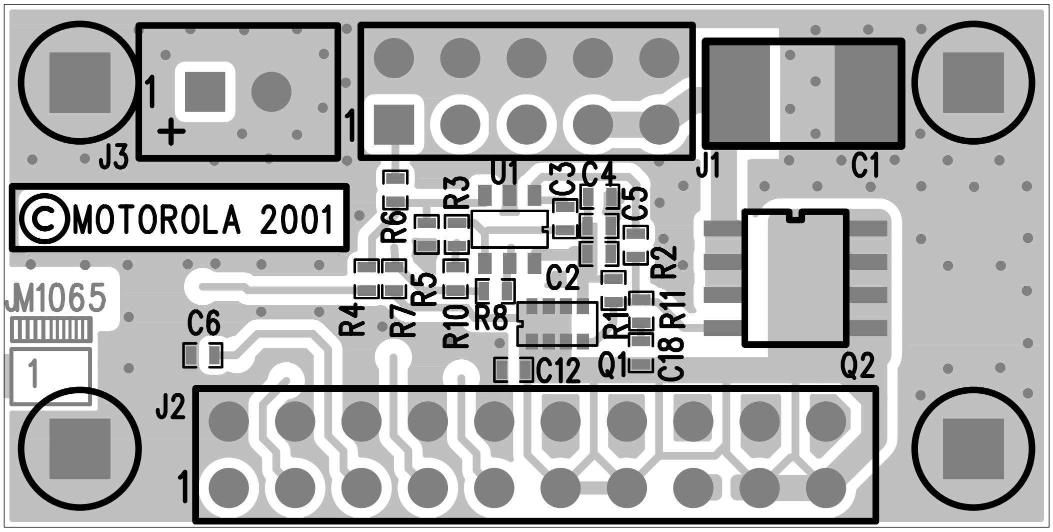


Figure 29. Power Amplifier Control Loop PCB

Table 7. Power Amplifier Control Loop PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1	68 µF	293D685X9020C	Sprague
C2	330 pF	GRM36COG330J50	Murata
C3	15 pF	GRM36COG150J50	Murata
C4	330 pF	GRM36x7R331K50	Murata
C5, C12, C18	10 nF	GRM36X7R103K25	Murata
C6	47 nF	GRM36X7R473K10	Murata
J1, J2, J3	DC connector		
Q1	Power MOSFET	NTHS5445T	ON Semiconductor
Q2	N/C - Do not mount		
R1, R8	1.0 k	CRG0402 5% 1 kO	NEOHM
R2	150 Ω	CRG0402 5% 150 O	NEOHM
R3	12 k	CRG0402 5% 12 kO	NEOHM
R4, R5	5.6 k	CRG0402 5% 5.6 kO	NEOHM
R6, R10	N/C - Do not mount		
R7	560 Ω	CRG0402 5% 560 O	NEOHM
R11	100 Ω	CRG0402 5% 100 O	NEOHM
U1	CMOS Op Amp	AD8591	Analog Devices

5 Packaging Information

Shipping, Packaging and Marking Information

Tape Width: 16.0 mm
Tape Pitch 12 mm (part to part)
Reel Diameter: 330 mm (13 in)
Component Orientation: Parts are to be orientated with pin 1 side closest to the tape's round sprocket holes on the tape's trailing edge.

Dry Pack: This device meets Moisture Sensitiviy Level (MSL) 3. Parts will be shipped in Dry Pack. Parts must be stored at 30°C and 60% relative humidity with time out of dry pack not to exceed 168 hours.

In the event that parts are not handled or stored within these limits, one of the following dry out procedures must be completed prior to reflow:

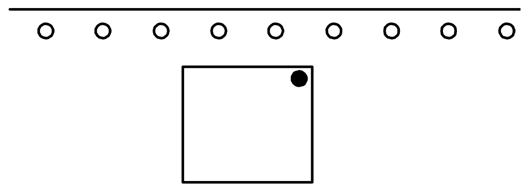
1) 40°C Dry Out: Bake devices at 40°C $\leq T_A \leq$ 45°C, 5% Relative Humidity for at least 192 hours.

2) Room Temperature Dry Out: Store devices at less than 20% Relative Humidity for at least 500 hours.

Marking:

1st line:	Motorola Logo
2nd Line:	Partnumber coded on 7 characters
3rd Line:	Wafer lot number (coded on 6 characters) followed by wafer number (coded on 3 digits)
4th Line:	Assy site code (on 1 or 2 characters), followed by Wafer Lot Number (coded on 1 or 2 characters), followed by Year (on 2 digits) and Workweek (on 2 digits).

Marking
(Top View)



Tape & Reel Orientation
(Top View)

Figure 30. Packaging Information

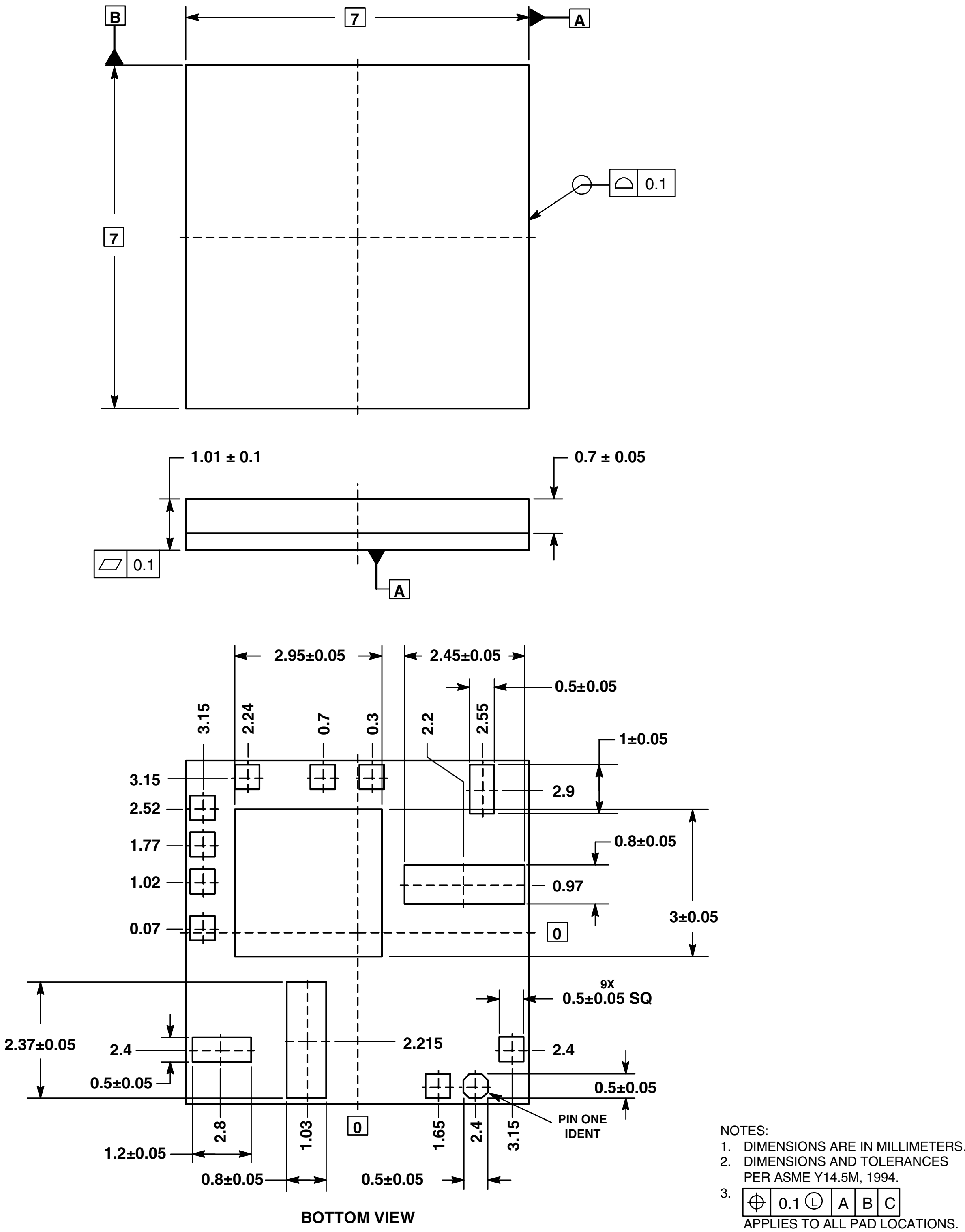


Figure 31. Outline Dimensions for 7x7 mm Module
(Case 1383-02, Issue A)

NOTES

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