

# □ MN102H460B

<b>Type</b>	MN102H460B	
<b>ROM (x8-bit)</b>	External	
<b>RAM (x8-bit)</b>	4 K	
<b>Package</b>	LQFP128-P-1818C *Lead-free, TQFP128-P-1414B *Lead-free	
<b>Minimum Instruction Execution Time</b>	With main clock operated	50 ns (at 3.0 V to 3.6 V, 40 MHz) 100 ns (at 2.0 V to 3.6 V, 20 MHz)
<b>Interrupts</b>	<ul style="list-style-type: none"> <li>• RST pin • Watchdog • NMI pin • Timer counter 4 to 15 • Timer counter 16, 17, 21</li> <li>• Timer counter 16 to 20 compare capture A • Timer counter 16 to 20 compare capture B</li> <li>• Timer counter 21 capture A • Timer counter 21 capture B • Timer counter 21 capture D</li> <li>• Timer counter 21 compare E • Timer counter 21 compare F • ATC ch.0 to 3 transfer finish</li> <li>• External 0 to 7 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • <math>\overline{KI}</math> pin (OR)</li> <li>• A/D conversion finish</li> </ul>	
<b>Timer Counter</b>	<p>Timer counter 0 : 8-bit × 1 (prescalers) Clock source ..... 1/2 of system clock frequency; timer counter 1 output</p> <p>Timer counter 1 : 8-bit × 1 (prescalers) Clock source ..... 1/2 of system clock frequency; timer counter 0 output</p> <p>Timer counter 2, 3 : 8-bit × 1 (UART baud rate generator) Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output</p> <p>Timer counter 4 : 8-bit × 1 (timer output, A/D conversion start up) Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source ..... underflow of timer counter 4</p> <p>Timer counter 5, 9 : 8-bit × 1 (UART baud rate generator) Clock source ..... 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output Interrupt source ..... underflow of timer counter 5, 9</p> <p>Timer counter 6, 10, 11 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output Interrupt source ..... underflow of timer counter 6, 10, 11</p> <p>Timer counter 7 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output Interrupt source ..... underflow of timer counter 7</p> <p>Timer counter 8 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source ..... underflow of timer counter 8</p> <p>Timer counter 12 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock frequency; external clock input with edge; timer counter 0 output; timer counter 1 output Interrupt source ..... underflow of timer counter 12</p> <p>Timer counter 13 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output Interrupt source ..... underflow of timer counter 13</p> <p>Timer counter 14 : 8-bit × 1 (timer output) Clock source ..... 1/2 of system clock; external clock input with edge; timer counter 0 output Interrupt source ..... underflow of timer counter 14</p>	

<b>Timer Counter (Continue)</b>	<p>Timer counter 15 : 8-bit × 1 (timer output)            Clock source ..... 1/2 of system clock frequency; external clock input with edge; timer counter 0 output            Interrupt source ..... underflow of timer counter 15</p> <p><b>Connectable</b> timer counter 0 to 3, 4 to 7, 8 to 11, 12 to 15</p> <p>Timer counter 16, 17 : 16-bit × 1            (timer output, event count, input capture, output compare, PWM output, 2-phase encorder input)            Clock source ..... 1/2 of system clock frequency; external clock input (with edge, timer counter 17 only); timer counter 0 output; timer counter 1 output (timer counter 16 only)            Interrupt source ..... coincidence with compare capture A or at capture;            coincidence with compare capture B or at capture;            underflow of timer counter 16, 17</p> <p>Timer counter 18, 19, 20: 16-bit × 1            (timer output, event count, input capture, output compare, PWM output, 2-phase encorder input)            Clock source ..... 1/2 of system clock frequency; external clock input; timer counter 0 output;            timer counter 1 output            Interrupt source ..... coincidence with compare capture A or at capture;            coincidence with compare capture B or at capture;            underflow of timer counter 18, 19, 20</p> <p>Timer counter 21 : 24-bit × 1 (servo control)            Clock source ..... 1/2 of system clock frequency; timer counter 1 output            Interrupt source ..... when capturing to capture A;            when capturing to capture B;            when capturing to capture D;            when coinciding to compare E;            when coinciding to compare F</p>
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<b>Serial Interface</b>	<p>Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)            Clock source ..... 1/8 of timer counter 2; 1/8, 1/2 of timer counter 5; external clock</p> <p>Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)            Clock source ..... 1/8 of timer counter 3; 1/8, 1/2 of timer counter 9; external clock</p> <p>UART × 4 (common use with serial 0 to 3)</p> <p>I<sup>2</sup>C × 2 (common use with serial 1, 3; single master)</p>
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<b>I/O Pins</b>	<b>I/O</b>	55	<ul style="list-style-type: none"> <li>• Common use : 55 (use of full address, address data separate 16-bit mode)</li> <li>• Common use : 72 (use of address 16-bit, address data multiplex 16-bit mode)</li> </ul>
	<b>Input</b>	8	<ul style="list-style-type: none"> <li>• Common use : 8</li> </ul>

<b>A/D Inputs</b>	10-bit × 12-ch. (maximum input is 16) (with S/H)
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<b>PWM</b>	16-bit × 5-ch. (timer counter 16 to 20)
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<b>ICR</b>	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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<b>OCR</b>	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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<b>Notes</b>	Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable
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See the next page for electrical characteristics, pin assignment and support tool.

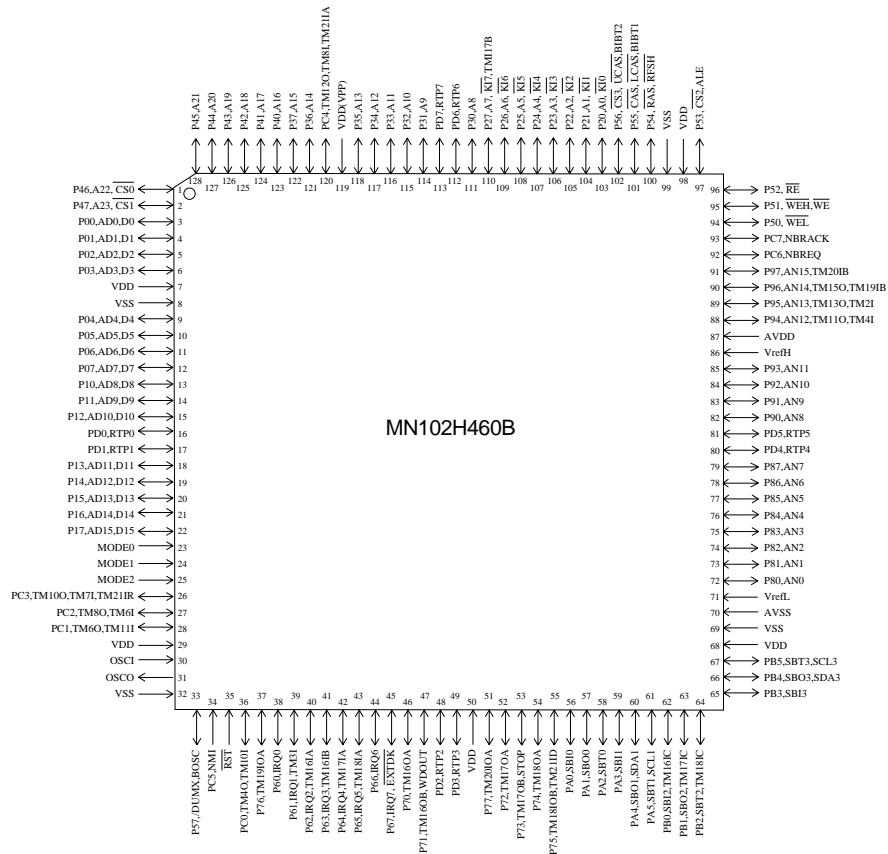
## Electrical Characteristics

### Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 40 MHz, VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 40 MHz, VDD = 3.3 V, output open			25	mA

(Ta = -20°C to +70°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

## Pin Assignment



LQFP128-P-1818C \*Lead-free

TQFP128-P-1414B \*Lead-free

## Support Tool

### ■ In-circuit Emulator

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PX-ICE102H46-LQFP128-P-1818C

PX-ICE102H46-TQFP128-P-1414B

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Minimum instruction execution time    57.1 ns (at 30 MHz)

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