❑ MN103000

Type	MN103000
Command RAM (×64-bit)	16 K-byte
Data RAM (×32-bit)	16 K-byte
Package **(Conventional Package)**	QFP160-P-2828F *Lead-free (QFP160-P-2828B)
Minimum Instruction Execution Time	17 ns (at 3.3 V to lerance = ± 5%, 60 MHz)
Interrupts	• RESET • IRQ × 8 • NMI • Timer × 28 • SIF × 4 • DMAC × 4 • WDT • A/D • System error
Timer Counter	Timer counter 0 to 3: 32-bit × 1 (interval timer, event count, timer output, interrupt, clock source for serial I/F, A/D conversion trigger) Clock Source ····· IOCLK; external clock input; underflow of timer counter Interrupt Source ····· underflow of timer counter 0, 1, 2, 3 Timer counter 4 to 7: 32-bit × 1 (interval timer, event count, timer output, interrupt, clock source for serial I/F) Clock source ····· IOCLK; external clock input; underflow of timer counter Interrupt source ····· underflow of timer counter 4, 5, 6, 7 *: Configuration of each of timer counters 0 to 3 and timer counters 4 to 7 can be changed to 8-, 16- and 24-bit timer counters. Timer counter 8: 16-bit × 1 (interval timer, event count, toggle output (2 lines), PWM output, one-shot output, input capture (2 lines), interrupt, DMA start, generation of timer synchronous output timing) Clock source ····· IOCLK; external clock input; underflow of timer counter Interrupt source ····· overflow of timer counter 8; coincidence with compare capture (2 lines) or at capture Timer counter 9: 16-bit × 1 (interval timer, event count, toggle output (2 lines), PWM output, high-speed PWM output, one-shot output, input capture (2 lines), interrupt, DMA start, generation of timer synchronous output timing) Clock source ····· IOCLK; external clock input; underflow of timer counter Interrupt source ····· overflow of timer counter 9; coincidence with compare capture (2 lines) or at capture Timer counter 10: 16-bit × 1 (interval timer, event count, toggle output (3 lines), PWM output (2 lines), one-shot output, input capture (3 lines), interrupt, DMA start, 2-phase encode) Clock source ····· IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source ····· overflow of timer counter 10; underflow of timer counter 10; coincidence with compare capture (3 lines) or at capture Timer counter 11: 16-bit × 1 (interval timer, event count, toggle output (4 lines), PWM output, inter-offset 3-phase PWM output, one-shot output, input capture (4 lines), interrupt, DMA start, 2-phase encode) Clock source ····· IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source ····· overflow of timer counter 11; underflow of timer counter 11; coincidence with compare capture (4 lines) or at capture Timer counter 12: 16-bit × 1 (interval timer, event count, toggle output (4 lines), PWM output (3 lines), one-shot output, input capture (4 lines), interrupt, 2-phase encode) Clock source ····· IOCLK; external clock input; 2-phase encode; underflow of timer counter Interrupt source ····· overflow of timer counter 12; underflow of timer counter 12; coincidence with compare capture (4 lines) or at capture

Timer Counter (continue)	Watchdog timer: 16-bit to 25-bit × 1		
Serial Interface	Serial 0, 1: 7-bit, 8-bit × 2 (clock synchronous mode, start-stop synchronous mode, I²C mode) Clock source: ····· (clock synchronous mode, start-stop synchronous mode) IOCLK; underflow of timer counter; external clock (I²C mode) IOCLK; underflow of timer counter		
I/O Pins	**I/O**	51	• Common use
	Output	25	• Common use
	Input	13	• Common use
A/D Inputs	10-bit × 8-ch.		
PWM	16-bit × 5-ch.		
ICR	16-bit × 15-ch. (common with OCR)		
OCR	16-bit × 15-ch. (common with ICR)		
Timer Synchronous Output	4-bit (synchronous output) × 2-ch.		
DMAC	4-ch.		

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	VDD , PVDD , AVDD = 3.3 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			250	mA
Supply current at SLEEP	IDD2	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			50	mA
Supply current at HALT	IDD3	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , fosc = 15.0 MHz FRQS pin = Hi level Output open			5	mA
Supply current at stopping	IDD4	VDD , PVDD , AVDD = 3.465 V VI = VDD or VSS , Fosc = Oscillation stopped Output open			300	µA

(Ta = –20°C to +70°C)

See the next page for electrical characteristics (continue), pin assignment and support tool.

Electrical Characteristics (Continue)

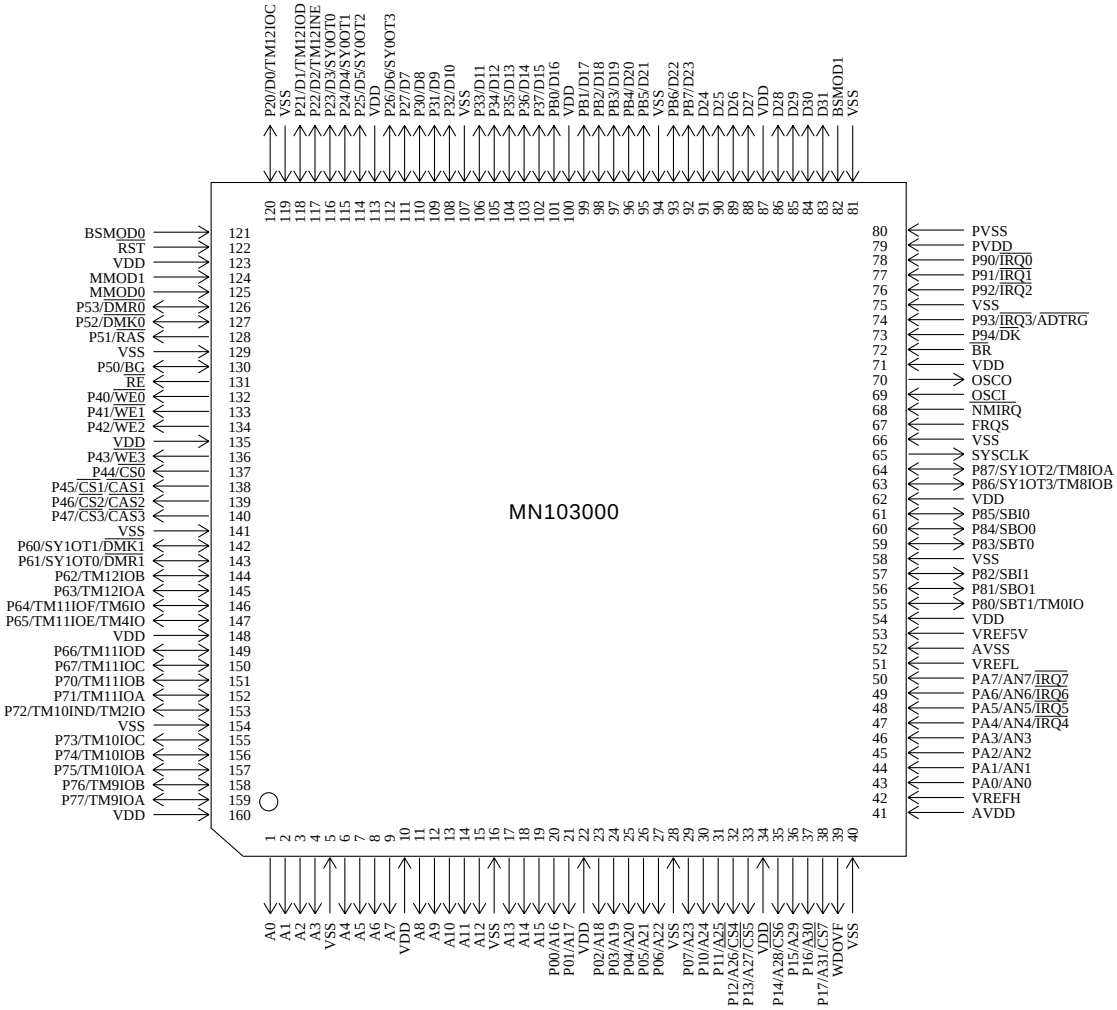
A/D conversion performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute error		VREF+ = 3.3 V, VREF– = 0.0 V A/D conversion clock = 5 MHz			± 7	LSB
A/D conversion relative error					± 5	LSB
A/D conversion time			2.8			µs

(Ta = –20°C to +70°C, AVDD = 3.3 V, AVSS = 0.0 V)

Pin Assignment

( ) : Conventional Package



QFP160-P-2828F *Lead-free

(QFP160-P-2828B)

Support Tool

In-circuit Emulator	PX-ICE103000-QFP160-P-2828B
On-board Development Tools	CSIDE-MN10300 (Computex Co., Ltd, product)

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