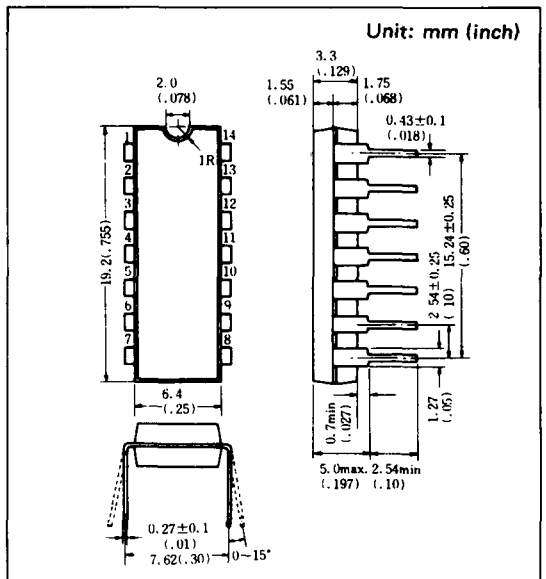
MN3004

512-STAGE LOW NOISE BBD

■ General Description

The MN3004 is a 512-stage high performance low noise BBD that provides a 85dB of signal to noise ratio (S/N) by increasing a capacity of capacitors with the same chip area, which is enabled by the improvement of silicon materials and process. There are many features for this device such as low insertion loss and no back gate bias voltage V_{BB}, etc.

The MN3004 can delay analog signal of the audio band in the range of 2.56ms ~ 25.6ms by adjusting a clock frequency.



14-Lead Dual-In-Line Plastic Package

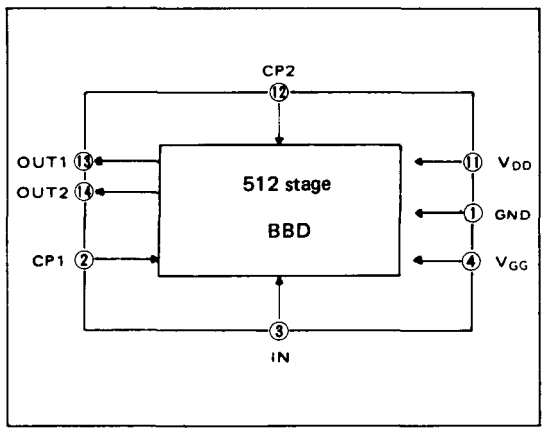
■ Features

- Variable delay of audio signal: 2.56ms ~ 25.6ms
- Clock component cancellation capability.
- Low insertion loss: L_j = 1/5dB typ.
- Wide dynamic range: S/N ≃ 85dB typ.
- Wide frequency response: $f_j \leqq 0.3 \times f_{cp}$
- Clock frequency range: 10 ~ 100KHz
- Low noise: V_{no} = 0.21mVrms max.
- Low distortion: THD = 0.4% typ.

■ Applications

- Variable playback speed of tape recorder.
- Reverberation and echo effects of audio equipments such as stereo.
- Tremolo, vibrato and chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems.
- Others.

■ Block Diagram



■ Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	2.56~25.6	ms
Total Harmonic Distortion	THD	0.4	%
Signal to Noise Ratio	S/N	85	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18～+0.3	V
Output Voltage	V_O	−18～+0.3	V
Operating Temperature	Topr	−20～+60	℃
Storage Temperature	Tstg	−55～+125	℃

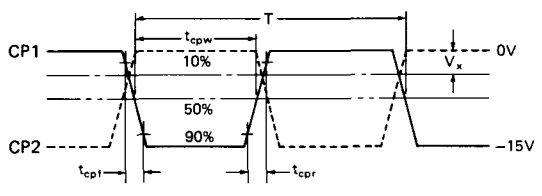
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				350	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{cpw}				0.5T*2	
Clock Rise Time *1	t_{cpr}				500	ns
Clock Fall Time *1	t_{cpf}				500	ns
Clock Cross Point	V_X		0		−3	V
Input DC Bias	V_{Bias}		−5		−10	V

■ Electrical Characteristics (Ta = 25°C, V_{DD} = V_{CPL} = −5V, V_{CPH} = 0V, V_{GG} = −14V, R_L = KΩ)

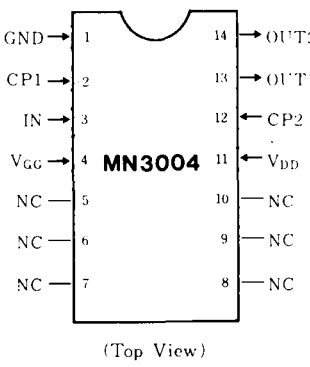
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		2.56		25.6	ms
Input Signal Frequency	f_i	f_{CP} = 40kHz, V_i = 1.8Vrms, 3dB down (0 dB at f_i = 1kHz)	12			kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i = 1 kHz, THD≦2.5%	1.8			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz, V_i =1.8Vrms	−4	1.5	4	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i = 1 kHz, V_i = 1 Vrms		0.4	2.5	%
Noise Voltage	Vno	f_{CP} = 100kHz Weighted by "A" curve			0.21	mVrms
Signal to Noise Ratio	S/N			85		dB

*1 Clock Pulse Wavefroms



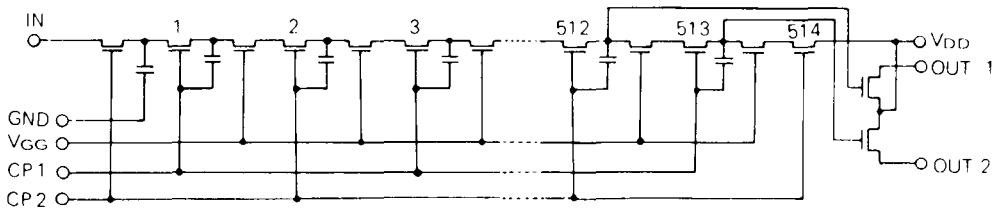
*2 T = 1/fcp (Clock Period)

■ Terminal Assignments



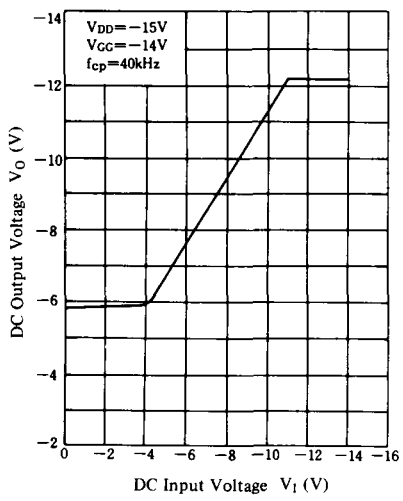
(Top View)

■ Circuit Diagram

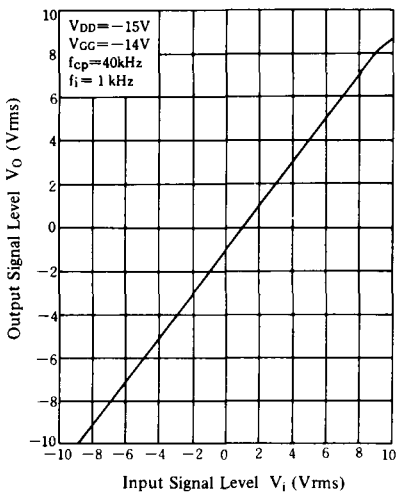


■ Typical Electrical Characteristic Curves

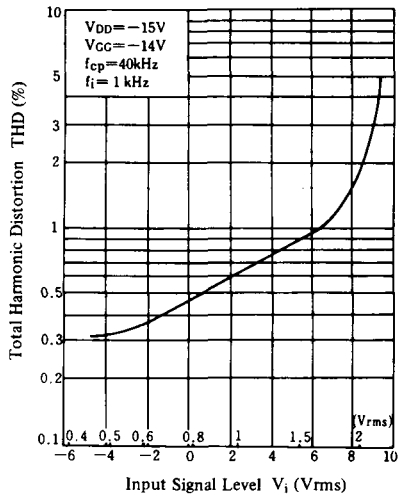
$V_O—V_I$



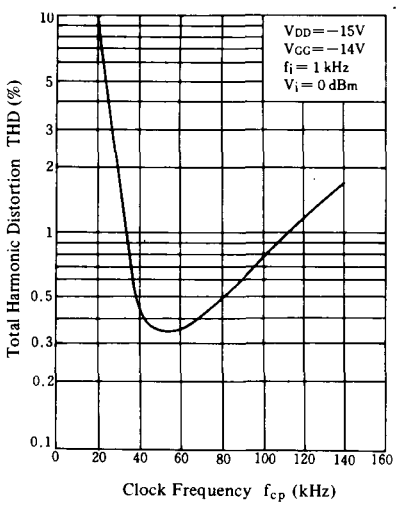
$V_O—V_i$



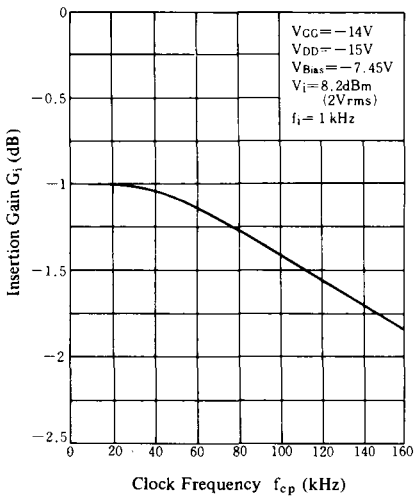
THD—V_i



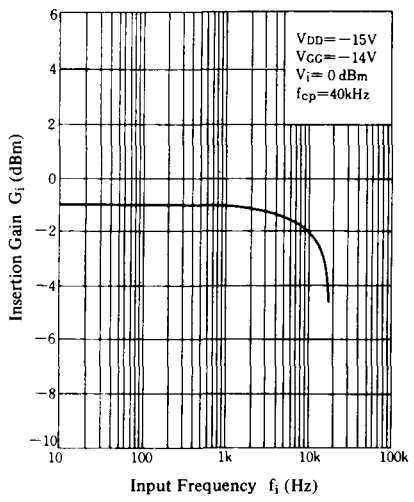
THD—fcp



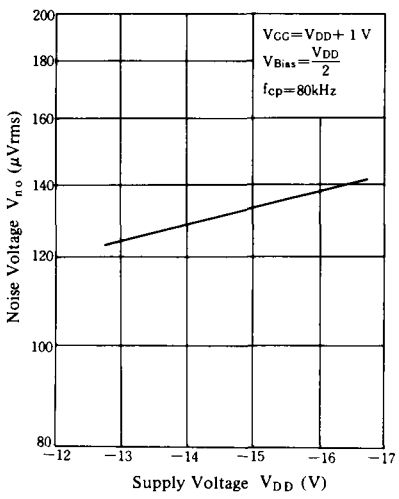
$G_i—f_{cp}$



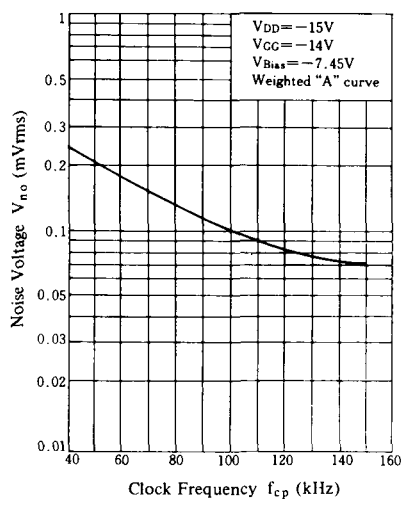
$G_i—f_i$



$V_{no}—V_{DD}$

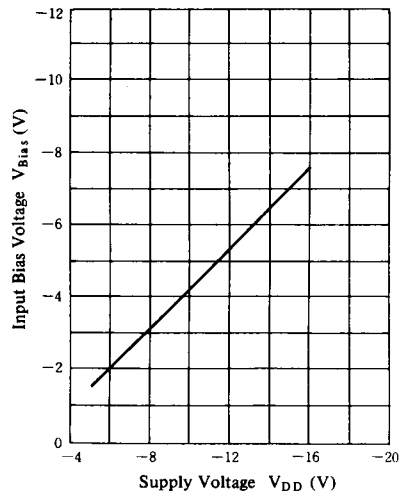


$V_{no}—f_{cp}$

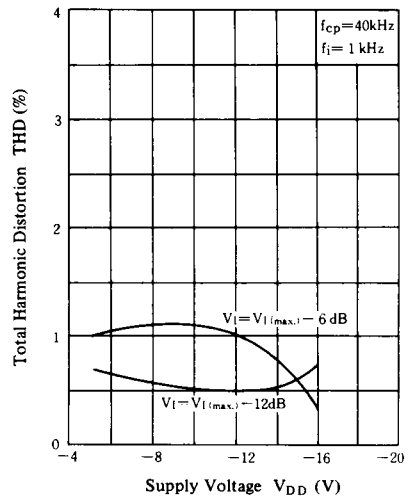


■ Supply Voltage Characteristics

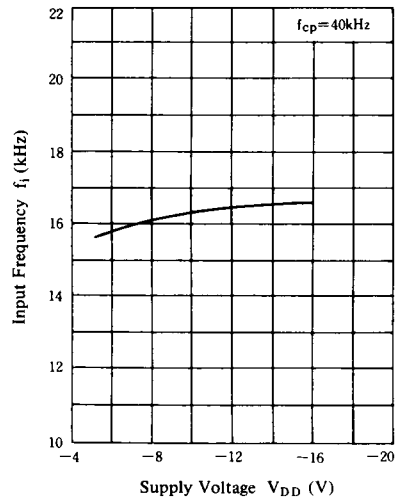
V_{Bias}—V_{DD}



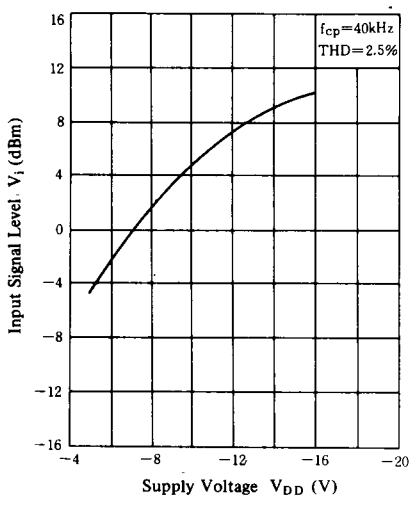
THD—V_{DD}



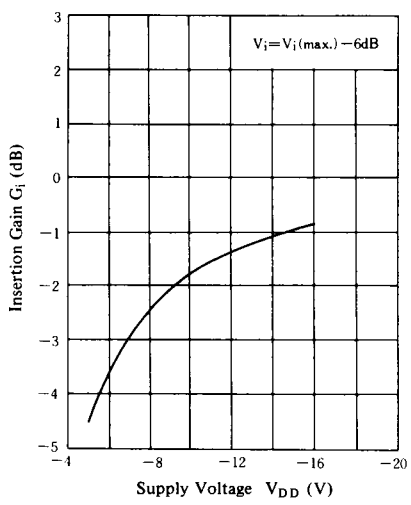
f_i—V_{DD}



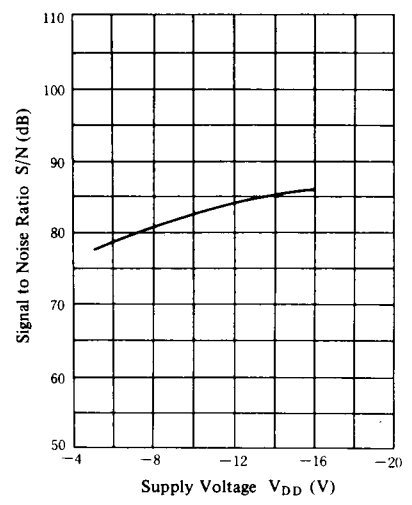
V_i—V_{DD}



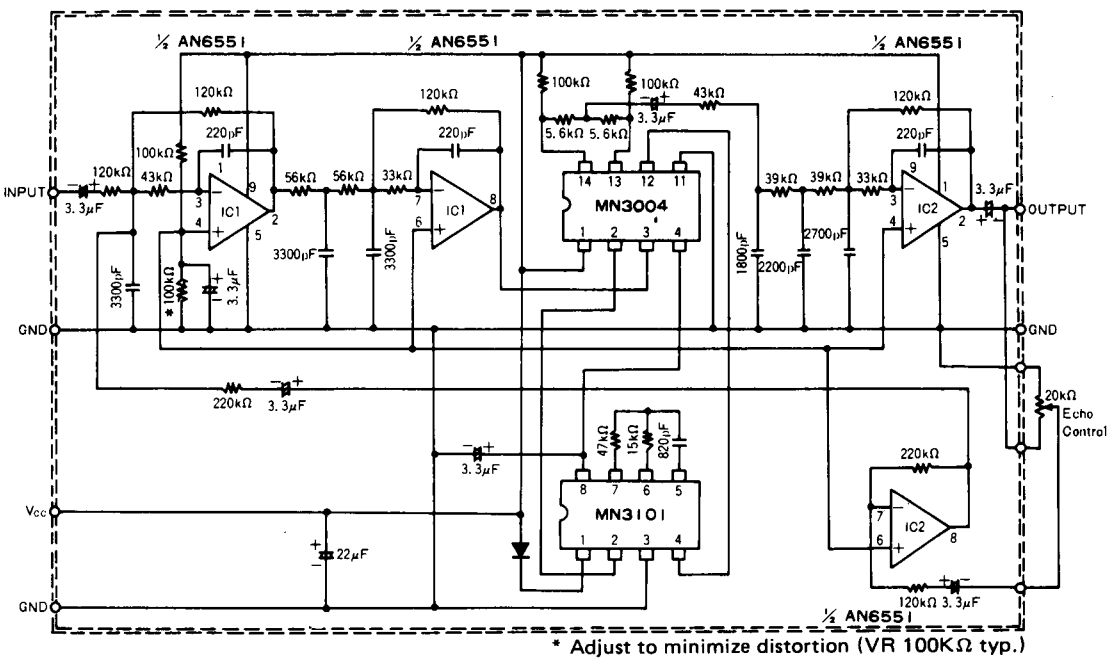
G_i—V_{DD}



S/N—V_{DD}



■ Application Circuit



* Adjust to minimize distortion (VR 100KΩ typ.)

Echo Effect Generation Circuit (Signal Delay Over 10msec.)